AN15154

How to Implement a 10BASE-T1S Network on MCX A577

Rev. 1.0 — 18 November 2026 Application note

Document information

Information	Content
Keywords	AN15154, MCX A5, 10BASE-T1S, TJF1410
Abstract	This application note describes how to build a 10BASE-T1S network using the NXP MCX A577 microcontroller.

1 Overview

This application note describes how to build a 10BASE-T1S multidrop Ethernet network using the NXP MCX A577 microcontroller. It explains the on-chip networking building blocks of the device. It also identifies the required external components, and provides the technical background required to design, configure, and bring up a 10BASE-T1S mixing segment.

The MCX A5 family devices are scalable microcontrollers within the MCX A Series. Optimized for connected industrial and secure edge applications, the MCX A577 combines a 240 MHz Arm Cortex-M33 core with up to 2 MB of flash memory and 640 kB SRAM. The device also provides advanced connectivity, rich analog integration, versatile serial interfaces, and enhanced security capabilities.

The device integrates a 10/100 Mbit/s Ethernet MAC and a 10BASE-T1S digital PHY. This integration simplifies industrial networking because both the MAC and the 10BASE-T1S digital PHY are integrated on the die. The only external component required to complete a physical 10BASE-T1S node is a Physical Medium Dependent (PMD) transceiver that complies with the Single-Pair Ethernet OPEN Alliance TC14 3-pin PMD interface.

NXP provides the TJF1410 PMD transceiver for exactly this purpose. The TJF1410 is a cost-effective 10BASE-T1S PMD transceiver that complies with IEEE 802.3cg and OPEN Alliance TC14 standards. It is supplied in a compact HVSON8 package measuring 3 mm x 3 mm. Its key features include:

- An OPEN Alliance TC14 3-pin interface for connection to the host digital PHY
- Support for 10BASE-T1S multidrop networks with up to 32 nodes and a total cable length of up to 100 m
- High Electromagnetic Compatibility (EMC) performance
- OPEN Alliance TC10-to-TC14 wake-up support
- TC14 advanced diagnostics capabilities, including topology discovery
- Compatibility with Power-over-Data-Line (PoDL) implementations

In addition to the on-chip 10BASE-T1S digital PHY, the ENET MAC can also connect to an external Ethernet PHY through the MII/RMII interface. This application note focuses on implementing a 10BASE-T1S network on the MCX A577. In this configuration, the ENET MAC connects to the integrated 10BASE-T1S digital PHY. The digital PHY drives the external TJF1410 PMD transceiver through the OPEN Alliance TC14 3-pin interface.

Figure 1 shows a conceptual block diagram of this configuration.

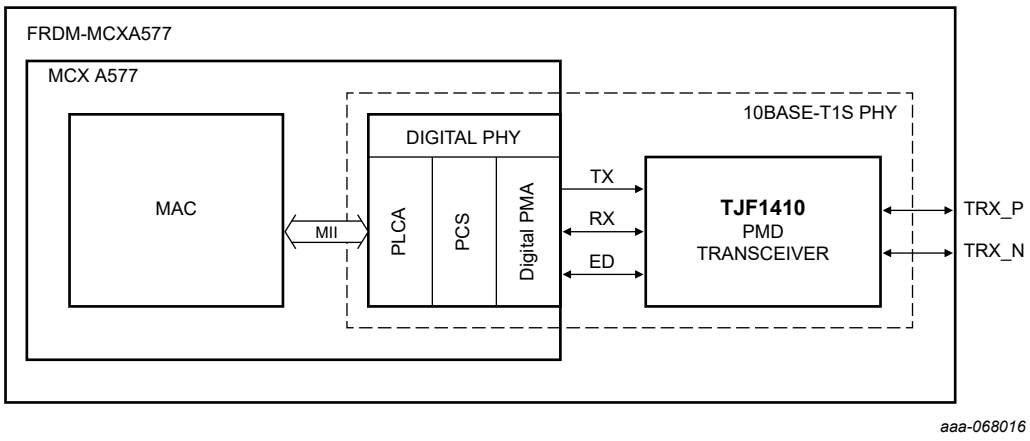


Figure 1. 10BASE-T1S network system block diagram

The combination of the MCX A577 and a TJF1410 PMD transceiver enables the implementation of an IEEE 802.3cg-compliant 10BASE-T1S multidrop Ethernet node.

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2 Ethernet MAC (ENET)

The MCX A577 integrates one instance of the Ethernet Media Access Controller (MAC) module, ENET0. This Ethernet interface is full-featured, supports 10 Mbit/s or 100 Mbit/s operation, and uses Direct Memory Access (DMA) hardware acceleration to optimize performance. It enables a host to transmit and receive Ethernet data in compliance with the IEEE 802.3-2008 standard.

The ENET controller can connect either to the on-chip 10BASE-T1S digital Physical Layer Device (PHY) or to an external Ethernet PHY. The SYSCON ENET_CTRL register controls the connection used by the ENET controller.

The ENET is an Advanced High-performance Bus (AHB) manager connected to the AHB multilayer matrix. It can access the internal SRAM used to store Ethernet frame data and control and status information. Automatic frame transmission and reception with Scatter-Gather DMA offloads many operations from the CPU.

The ENET module includes the following key features:

- Ethernet operation at 10 Mbit/s and 100 Mbit/s, compliant with IEEE 802.3-2008.
- Scatter-Gather DMA support for automatic frame handling.
- IEEE 1588-2008 version 2 (v2) timestamping and advanced timestamp support driven by the external PHY clock.
- Power management with magic packet detection for wake-on-LAN.
- Support for both Media Independent Interface (MII) and Reduced Media Independent Interface (RMII) (v1.2) PHY interfaces.
- MDIO management interface that supports Clause 22 and Clause 45 for managing and configuring the PHY.
- Internet Protocol (IP) checksum offloading for Transmission Control Protocol (TCP), User Datagram Protocol (UDP), and Internet Control Message Protocol (ICMP) payloads encapsulated over IP.
- Both full-duplex and half-duplex operation, including Carrier Sense Multiple Access with Collision Detection (CSMA/CD) for half-duplex.
- IEEE 802.3x pause frames support and Priority Flow Control (PFC) for full-duplex and backpressure for half-duplex.
- Automatic transmission of zero-quanta pause frames when the flow-control input is deasserted during full-duplex operation.

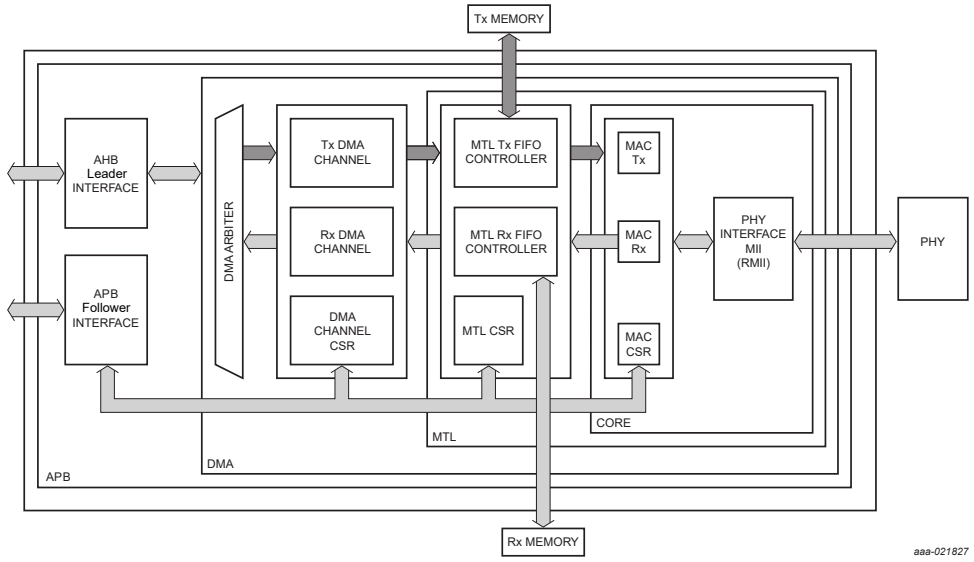


Figure 2. Ethernet MAC block diagram

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3 10BASE-T1S digital PHY (TENBASET_PHY)

The MCX A577 integrates a 10BASE-T1S digital PHY IP named TENBASET_PHY. It is a digital module that provides the Physical Medium Attachment (PMA) and Physical Coding Sublayer (PCS) building blocks. It also includes a Physical Layer Collision Avoidance (PLCA) Reconciliation Sublayer building block compliant with the IEEE 802.3cg 10BASE-T1S Ethernet Physical Layer standard. To form a complete IEEE-compliant PHY, an external PMD transceiver that supports the OPEN Alliance TC14 PMD transceiver interface must be attached to the TENBASET_PHY.

The TENBASET_PHY includes the following features:

- Support for 10BASE-T1S multidrop operation.
- An OPEN Alliance TC14 3-pin PMD interface for connecting to an external PMD transceiver.
- Internal PCS and external PMD loopback modes.
- A mode controller that supports low-power and PMD configuration modes.
- Local and remote wake-up detection and generation of Wake-Up Patterns (WUP) in compliance with the OPEN Alliance TC14/TC10 specification.
- Two interrupt outputs for reporting functional and safety-related events.
- An integrated Serial Management Interface (SMI) controller for accessing the PMD control and status registers through the 3-pin interface.
- Built-in Self-Test (BIST) for the external PMD transceiver.
- Diagnostic function for monitoring PLCA operation, pin faults, and PMD status.
- Debug outputs for monitoring internal signals.

The TENBASET_PHY does not support the following optional IEEE 802.3 features:

- The full-duplex long-range variant defined in Clause 146
- The full-duplex point-to-point variant defined in Clause 147
- Auto-Negotiation as defined in Clause 98
- The heartbeat function

Figure 3 shows the TENBASET_PHY block diagram.

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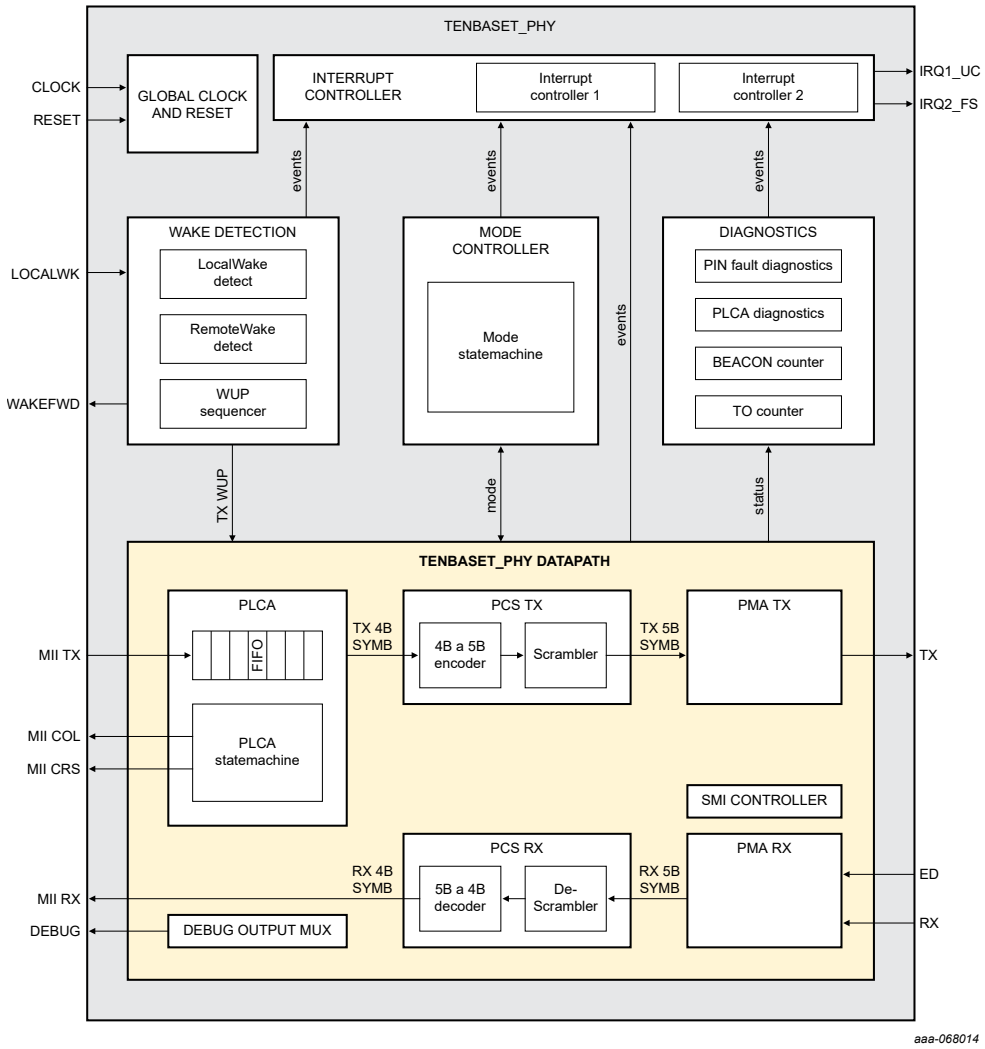


Figure 3. TENBASET_PHY block diagram

4 TJF1410 PMD transceiver

The TJF1410 is an NXP 10BASE-T1S PMD transceiver, which complies with the OPEN Alliance Technical Committee 14 (TC14) specifications. It is suitable for 10 Mbit/s industrial Ethernet applications. The TJF1410 communicates through the OPEN Alliance TC14 3-pin interface with a host Microcontroller Unit (MCU) or switch that provides the 10BASE-T1S digital PHY, such as the MCX A577.

Together, the MCX A577 (with its integrated ENET MAC and 10BASE-T1S digital PHY) and the TJF1410 form a complete, cost-effective 10BASE-T1S node.

The TJF1410 is a cost-effective solution for 10BASE-T1S connectivity and comes in a compact, low-footprint HVSON8 (3 mm x 3 mm) package. It ensures high signal quality even in challenging electromagnetic compatibility environments while maintaining a low quiescent current consumption.

The TJF1410 PMD transceiver includes the following features:

- 10BASE-T1S PMD transceiver compliant with IEEE 802.3cg and OPEN Alliance TC14 specifications.
- OPEN Alliance TC14 3-pin interface for connecting to a host MCU or switch that provides the 10BASE-T1S digital PHY.

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- Best-in-class EMC performance.
- Low quiescent current consumption.
- OPEN Alliance TC10 to TC14 wake-up support; a wake signal over the Ethernet data line.
- OPEN Alliance TC14 advanced diagnostics, including topology discovery.
- Compatibility with a PoDL implementation.
- Low-footprint HVSON8 measuring 3 mm x 3 mm package.

In an MCX A577-based 10BASE-T1S node, the TJF1410 connects to the device on-chip 10BASE-T1S digital PHY through the OPEN Alliance TC14 three-pin interface. This interface consists of the TX, RX, and ED signals.

The MCX A577 digital PHY controls the operating mode of the TJF1410 to keep the two devices in consistent operating states. For example, the digital PHY and the PMD transceiver can enter low-power mode together. The integrated Serial Management Interface (SMI) controller of the digital PHY accesses the TJF1410 control and status registers through the same 3-pin interface when the digital PHY is in `TXCCONFIG` mode.

Because the TJF1410 complies with all OPEN Alliance TC14 conformance test specifications, it supports TC10-to-TC14 wake-up functionality and TC14 advanced diagnostic capabilities. Together, the MCX A577 and TJF1410 support standards-compliant 10BASE-T1S multidrop networking with a reduced external component count.

5 Hardware

This section describes the hardware platform used to implement a 10BASE-T1S network with the MCX A577. The implementation is based on the NXP FRDM-MCXA577 board.

The FRDM-MCXA577 is a design and evaluation platform built around the MCX A577 microcontroller. The board is compatible with Arduino (Arduino UNO R3) headers, the NXP FRDM-Touch shield, Mikroe click boards, and Pmod modules. It supports development tools, such as the NXP MCUXpresso IDE, IAR Embedded Workbench, and Arm Keil MDK. An onboard MCU-Link debug probe (based on the NXP LPC55S16 MCU) provides debug and VCOM port capabilities.

The MCX A577 integrates both the Ethernet MAC and the 10BASE-T1S digital PHY on-chip. The only external device required to complete a physical 10BASE-T1S node is an OPEN Alliance TC14-compliant PMD transceiver. The TJF1410A PMD transceiver is already placed on the board and wired to the MCU. As a result, the FRDM-MCXA577 can support a 10BASE-T1S network out of the box without requiring extra transceiver hardware or board rework.

The MCX A577 has a single Ethernet MAC module. To offer flexibility, the FRDM-MCXA577 board also includes a LAN8741 Ethernet PHY that supports 10/100 Mbit/s Ethernet through the RJ45 connector J19. However, the on-chip 10BASE-T1S PHY and the external LAN8741 PHY cannot be used at the same time, because both must connect to the same ENET MAC.

The SYSCON ENET_CTRL register selects the PHY connection used by the ENET MAC. For 10BASE-T1S operation, configure this register to connect the ENET MAC to the integrated 10BASE-T1S digital PHY. Figure 4 shows the FRDM-MCXA577 board and identifies the primary components and connector used for 10BASE-T1S operation.

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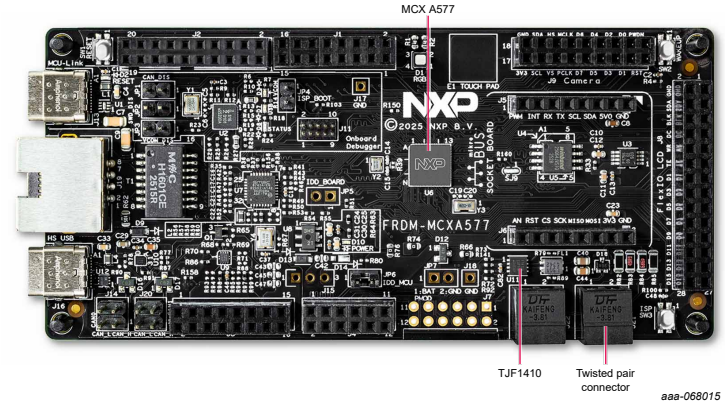


Figure 4. FRDM-MCXA577 board

The single-pair 10BASE-T1S cable connects to the board through two identical connectors, **J21** and **J22**. These two connectors are provided to support 10BASE-T1S multidrop operation. A leaf node at the end of the bus uses only one of the two connectors, with proper bus termination applied at the ends of the segment.

6 Software

This section describes the software resources available in the FRDM-MCXA577 SDK (version 26.06.00) for exercising the on-chip 10BASE-T1S Ethernet interface. Two groups of examples are relevant:

- The bare ENET driver examples are located in `boards/frdmmcxa577/driver_examples/enet/`
- The Lightweight Internet Protocol (lwIP) TCP/IP stack examples are located in `boards/frdmmcxa577/lwip_examples/`

All of these examples can drive either the external 100BASE-TX PHY or the internal 10BASE-T1S digital PHY (T1S). The `BOARD_NETWORK_USE_TENBASET_PHY` macro selects the required PHY.

6.1 ENET Driver examples

The `driver_examples/enet` directory contains low-level examples that use the ENET peripheral driver directly without a TCP/IP stack. These examples demonstrate how to initialize the ENET MAC, transmit frames, and receive frames using different reception mechanisms.

Each transmit-and-receive example transmits 20 broadcast or Precision Time Protocol (PTP) frames and prints the number of frames received. The PTP example sends 20 PTP event frames and displays the corresponding hardware timestamps.

Table 1. ENET Driver examples

Example	Description
txrx_rxinterrupt	Uses the ENET functional (non-transactional) TX/RX Application Programming Interface (API). The interrupt Interrupt Request (IRQ) handler receives the frames.
txrx_rxpoll	Uses the ENET functional TX/RX API. Polling receives the frames. Prints the count and the MAC address of each received frame.
txrx_transfer_rxinterrupt	Uses the ENET transactional TX/RX API. The interrupt IRQ handler receives the frames.
txrx_transfer_rxpoll	Uses the ENET transactional TX/RX API. Polling receives the frames.

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Table 1. ENET Driver examples*...continued*

Example	Description
txrx_ptp1588_transfer	Demonstrates the IEEE 1588 PTP feature: It transmits 20 PTP event frames and shows the transmit/receive hardware timestamps.

6.1.1 Default PHY loopback mode

By default, the ENET driver examples are configured to run in PHY loopback. This configuration allows the demo to be self-tested on the bench without a link partner.

When `BOARD_NETWORK_USE_TENBASET_PHY` is set to 1, the example initializes the internal 10BASE-T1S PHY by calling the `PHY_Wrapped_Init` wrapper function in `hardware_init.c`. After completing the standard PHY initialization, the wrapper function enables PCS local loopback, as shown in the following code:

```
/* Wrapper for PHY init to enable loopback */
static status_t PHY_Wrapped_Init(phy_handle_t *handle,
                                 const phy_config_t *config)
{
    status_t result;

    /* Initialize PHY */
    result = PHY_TENBASET_Init(handle, config);
    if (result != kStatus_Success)
    {
        return result;
    }

    /* Enable PCS loopback */
    return PHY_EnableLoopback(handle, kPHY_LocalLoop,
                              kPHY_Speed10M, true);
}
```

In this mode, the PHY internally loops back every frame transmitted by the ENET MAC. Therefore, the example receives the same frames that it sends. This configuration is useful for an initial bring-up test because it does not require an external cable or link partner. However, the test does not exercise the real 10BASE-T1S bus.

6.1.2 Enabling a real 10BASE-T1S network

To test a real 10BASE-T1S network with another node on the same mixing segment, disable PHY loopback mode and select the integrated 10BASE-T1S digital PHY. Follow the steps below:

1. Select the integrated 10BASE-T1S digital PHY. Set the `BOARD_NETWORK_USE_TENBASET_PHY` macro to `1U`. This macro is defined in the `board.h` file of the example project. The default value is `0U`. Change the value to `1U`.

   ```
   #ifndef BOARD_NETWORK_USE_TENBASET_PHY
   #define BOARD_NETWORK_USE_TENBASET_PHY (0U)   /* change to (1U) */
   #endif
   ```

   When the macro is set to `1U`, `app.h` selects the 10BASE-T1S PHY operations (phy_ops, MII mode kENET_MiiMode). The `hardware_init.c` file then performs the following operations:
   - Configures the 10BASE-T1S clock
   - Resets the T1S block
   - Enables the T1S interrupt

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- Connects the ENET MAC to the integrated `TENBASET_PHY0` via SYSCON -> ENET_CTRL = SYSCON_ENET_CTRL_PHY_SEL(1) | SYSCON_ENET_CTRL_PHY_INTF(0)
- Enables PLCA with node ID 1 by default

2. Disable the PHY loopback mode. Change the fourth parameter of the `PHY_EnableLoopback` function to false.

```
PHY_EnableLoopback(handle, kPHY_LocalLoop, kPHY_Speed10M, false);
```

3. Set different node IDs for the boards in the `BOARD_InitHardware()` function. In the following test, node IDs 0 and 1 are assigned to the two boards.
4. Use a twisted-pair cable to connect the two FRDM-MCXA577 boards using J21 or J22.
5. Rebuild the example and download it to the board.

After these changes are applied, the demo transmits its frames over the physical 10BASE-T1S mixing segment. The receiving board prints only the frames received from the link partner, providing an end-to-end test of the network.

The following test uses the `enet_txrx_rxpoll` example. Modify the original Software Development Kit (SDK) example according to the steps above, and set the PLCA nodeID to 0 and 1 to the two FRDM-MCXA577 boards, respectively. Compile the project and download it to two FRDM-MCXA577 boards.

Power on both boards. Then, to restart the application, press the Reset button, SW1, on the node 0 board. The node 0 board transmits 20 broadcast frames to the node 1 board. The following console outputs show the results for node 0 and node 1.

Node0 console output:

```
MCUX SDK version: 2026.09.00

ENET example start.
Wait for PHY init...
Wait for PHY link up...

Transmission start now!
The 1-th frame transmitted success!
The 2-th frame transmitted success!
The 3-th frame transmitted success!
The 4-th frame transmitted success!
The 5-th frame transmitted success!
The 6-th frame transmitted success!
The 7-th frame transmitted success!
The 8-th frame transmitted success!
The 9-th frame transmitted success!
The 10-th frame transmitted success!
The 11-th frame transmitted success!
The 12-th frame transmitted success!
The 13-th frame transmitted success!
The 14-th frame transmitted success!
The 15-th frame transmitted success!
The 16-th frame transmitted success!
The 17-th frame transmitted success!
The 18-th frame transmitted success!
The 19-th frame transmitted success!
The 20-th frame transmitted success!
```

Node 1 console output:

```
One frame received. the length 1018
```


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```
Dest Address ff:ff:ff:ff:ff:ff Src Address 54:27:8d:87:17:0e
One frame received. the length 1018
Dest Address ff:ff:ff:ff:ff:ff Src Address 54:27:8d:87:17:0e
One frame received. the length 1018
Dest Address ff:ff:ff:ff:ff:ff Src Address 54:27:8d:87:17:0e
One frame received. the length 1018
Dest Address ff:ff:ff:ff:ff:ff Src Address 54:27:8d:87:17:0e
One frame received. the length 1018
Dest Address ff:ff:ff:ff:ff:ff Src Address 54:27:8d:87:17:0e
One frame received. the length 1018
Dest Address ff:ff:ff:ff:ff:ff Src Address 54:27:8d:87:17:0e
One frame received. the length 1018
Dest Address ff:ff:ff:ff:ff:ff Src Address 54:27:8d:87:17:0e
One frame received. the length 1018
Dest Address ff:ff:ff:ff:ff:ff Src Address 54:27:8d:87:17:0e
```

Figure 5 shows the 10BASE-T1S network setup using two FRDM-MCXA577 boards.

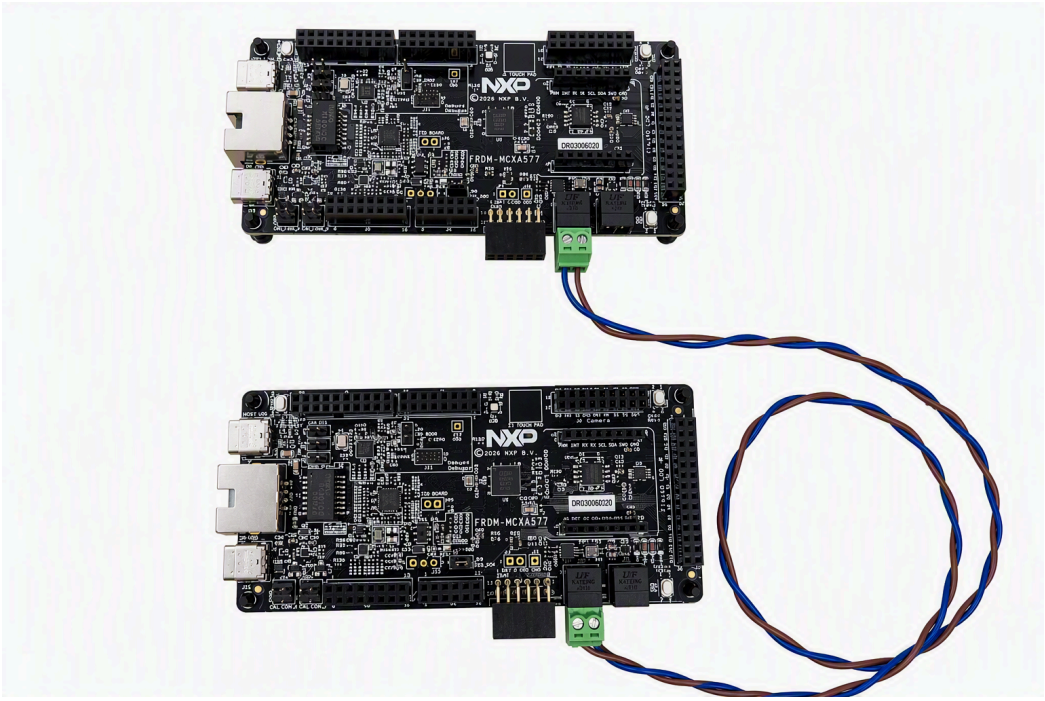


Figure 5. 10BASE-T1S network connectivity based on FRDM-MCXA577 boards

6.2 lwIP examples

The `lwip_examples` directory provides application-level examples that run on the lwIP TCP/IP stack. Most examples are supplied in two variants:

- A BareMetal version (bm)
- A FreeRTOS version (freertos)

Table 2. lwIP examples

Example	Variants	Description
lwip_ping	bm, freertos	ICMP ping demo. The example periodically sends ICMP echo requests

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Table 2. lwIP examples*...continued*

Example	Variants	Description
		to a PC and processes the replies. The board also replies to pings from the PC.
lwip_dhcp	bm, freertos	DHCP client demo. The example acquires an IP address from a DHCP server and prints the DHCP state transitions and link-state changes.
lwip_dhcp_usb	bm, freertos	DHCP (plus ping) demo running over the lwIP stack together with the USB stack.
lwip_iperf	bm	Throughput benchmark using the iperf protocol running on the lwIP stack.
lwip_ipv4_ipv6_echo	freertos	TCP and UDP echo servers supporting both IPv4 and IPv6.
lwip_mqtt	freertos	MQTT client that connects to an MQTT broker through an unsecured socket and obtains IP/DNS information through DHCP.
lwip_https_client	freertos	Downloads a webpage over an SSL/TLS connection using the HTTP GET method.
lwip_httpsrv	bm, freertos	HTTP server demo. A browser on the PC connects to the board, and the board serves a webpage.
lwip_httpssrv_mbedTLS	bm, freertos	HTTPS server built on lwIP together with the mbedTLS stack. The board serves pages over an encrypted HTTPS connection.

6.2.1 Selecting 10BASE-T1S for the lwIP examples

Like the ENET driver examples, the lwIP examples default to the external 100BASE-TX Ethernet interface through the RJ45 connector. To run these examples using the internal 10BASE-T1S PHY, set `BOARD_NETWORK_USE_TENBASET_PHY` to 1 in the example `board.h` and rebuild.

When `BOARD_NETWORK_USE_TENBASET_PHY` is set to `1`, the `hardware_init.c` file uses the same conditional initialization flow as the ENET driver examples. It configures the T1S clock, resets the T1S block, and connects the ENET MAC to the integrated 10BASE-T1S digital PHY.

Because the lwIP examples represent real network traffic, PHY loopback is not used. Instead, the board must be connected to a link partner.

For a PC-based 10BASE-T1S link, use a 10BASE-T1S network adapter instead of the RJ45 cable. Enable PLCA on the PC using the following parameters as documented in the example board README:

- Node ID: 0 (PLCA coordinator)
- Node count: 8
- TO timer: 32 BT
- Burst count: 0
- Burst timer: 128 BT

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By default, the FRDM-MCXA577 is configured with PLCA node ID 1 in `hardware_init.c`. Together, the PC coordinator (node ID 0) and the FRDM-MCXA577 board (node ID 1) form a PLCA-based 10BASE-T1S mixing segment.

Alternatively, another FRDM-MCXA577 board can be used as the second node. Change the PLCA node ID of the second board to `0`, then rebuild the project, and download it to the second board. To start the application, press the **RESET** button on the board.

7 Conclusion

This application note has shown how to build a 10BASE-T1S network using the MCX A577 and the FRDM-MCXA577 board. A key advantage of the MCX A577 is the integration of the Ethernet MAC and the 10BASE-T1S digital PHY on a single device. This eliminates the external PHY and its magnetics, saving board area and BOM cost, and requires only a PMD transceiver to reach the single-pair bus.

The FRDM-MCXA577 SDK provides ready-to-use examples, including the bare ENET driver examples for raw frame transmit/receive, and the lwIP examples for standard IP traffic. These examples enable developers to bring up a working 10BASE-T1S network, which makes the platform an excellent starting point for single-pair Ethernet designs.

8 Acronyms

Table 3 lists the acronyms used in this document.

Table 3. Acronyms

Term	Description
AHB	Advanced High-performance Bus
API	Application Programming Interface
APB	Advanced Peripheral Bus
BIST	Built-in Self-Test
CSR	Control and Status Register
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
DMA	Direct Memory Access
EMC	Electromagnetic Compatibility
FIFO	First In, First Out
ICMP	Internet Control Message Protocol
IP	Internet Protocol
IRQ	Interrupt Request
lwIP	Lightweight Internet Protocol
MAC	Media Access Controller
MCU	Microcontroller Unit
MII	Media Independent Interface
MTL	MAC Transfer Layer
OPEN	One-Pair Ethernet
PCS	Physical Coding Sublayer

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Table 3. Acronyms...*continued*

Term	Description
PFC	Priority Flow Control
PHY	Physical Layer Device
PLCA	Physical Layer Collision Avoidance
PMA	Physical Medium Attachment
PMD	Physical Medium Dependent
PoDL	Power-over-Data-Line
PTP	Precision Time Protocol
RMII	Reduced Media Independent Interface
SDK	Software Development Kit
SMI	Serial Management Interface
TC14	Technical Committee 14
TCP	Transmission Control Protocol
UDP	User Datagram Protocol
WUP	Wake-Up Patterns

9 Reference

The following is the list of the references used to supplement this document:

- *MCX A286, A287, A456, A457, A536, A537, A556, A557, A566, A567, and A577 Reference Manual* (MCXAP172M240F70RM)[1]
- *MCX A557/577 Datasheet* (MCXAP172M240F70)[1]

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11 Revision history

Table 4 summarizes the revisions to this document.

Table 4. Revision history

Document ID	Release date	Description
AN15154 v.1.0	18 November 2026	Initial public release

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