AN15136

Migration Guide from MCX A153 to MCX C162

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Document information

Information	Content
Keywords	AN15136, MCX A153, MCX C162, MCX C16, migration guide, cost-down, orderable part, pinout, ADC, OpAmp, FlexPWM
Abstract	This document provides customer-facing guidance for migrating an MCX A153 based design to MCX C162. It covers device selection, feature comparison, memory and clock migration, peripheral differences, hardware and pinout review, software migration, and validation recommendations.

1 Introduction

This document describes the migration considerations when moving from MCX A153 to MCX C162 microcontrollers. The migration direction is intended for products where customers want to reduce MCU cost, reduce external analog front-end components, or simplify a design while keeping a low-power Arm-based control platform.

MCX A153 is a higher-performance MCX A15 family device based on Arm Cortex-M33 at up to 96 MHz with 128 kB Flash, and 32 kB SRAM class resources. MCX C162 is an MCX C16 family device based on Arm Cortex-M23 at up to 72 MHz with 64 kB Flash, 12 kB SRAM, 153 CoreMark, precision analog, FlexPWM, and low-power operation. The devices are not considered drop-in replacements, so the migration must include both schematic and firmware review.

Migration positioning: MCX C162 is suitable when the application can fit into the smaller memory and CPU budget and does not require USB FS, I3C, or eQDC. The key MCX C162 advantage is the integrated analog subsystem, including 16-bit ADC, comparator with 8-bit DAC, and OpAmp/PGA.

2 Part number selection

Select the MCX C162 destination part by package, GPIO count, ADC channel requirement, production assembly preference, and PCB size. For an existing MCX A153 48-pin design, MCXC162VFT or MCXC162VLF must be evaluated first because they provide the highest GPIO counts in the MCX C162 family.

Table 1. MCXC162 orderable part options

Part number	Marking	Core speed (MHz)	Flash (kB)	SRAM (kB)	Pin count	Package
MCXC162VFG	MC7G	72	64	12	16	H-PQFN
MCXC162VFK	MC162K	72	64	12	24	H-PQFN
MCXC162VFM	MC162M	72	64	12	32	H-PQFN
MCXC162VFT	MC162T	72	64	12	48	H-PQFN
MCXC162VLF	MC162F	72	64	12	48	LQFP

Table 2. MCXC162 package-level pin resource summary

Destination part	Package/pin count	GPIO count	ADC input pins	Migration note
MCXC162VFG	H-PQFN16	15	4	Smallest package. Use only for limited I/O designs.
MCXC162VFK	H-PQFN24	23	6	H-PQFN24 is noted as not yet qualified in the data sheet.
MCXC162VFM	H-PQFN32	29	10	Balanced option for compact control designs.
MCXC162VFT	H-PQFN48	45	18	The closest package-class option when many GPIO and ADC channels are needed.
MCXC162VLF	LQFP48	43	16	Leaded package for easier probing

Table 2. MCXC162 package-level pin resource summary*...continued*

Destination part	Package/pin count	GPIO count	ADC input pins	Migration note
				and customer PCB assembly.

3 Feature comparison

3.1 High-level feature comparison

Table 3 summarizes the major system-level differences. The migration risks are primarily CPU performance reduction, memory reduction, and removal of MCX A153 features that are not present on MCX C162. The migration opportunity is the MCX C162 analog subsystem and low-cost entry-level positioning.

Table 3. High-level feature comparison between MCXA153 and MCXC162

Module	MCX A153	MCX C162	Migration impact
Core	Arm Cortex-M33, up to 96 MHz	Arm Cortex-M23, up to 72 MHz, 153 CoreMark	Measure CPU load, ISR latency, and control-loop timing.
Flash	128 kB class	64 kB Flash with ECC	Review map file, bootloader size, and NVM allocation.
RAM	32 kB class	12 kB RAM, configurable up to 8 kB with ECC	Reduce stacks, heap, DMA buffers, and sample buffers.
Clocking	FRO192M class clocking	FRO144M, FRO12M, FRO16K, OSC32K	Regenerate clock tree and all timed peripheral settings.
Connectivity	USB FS, I3C, LPI2C, LPSPI, LPUART	1x LPSPI, 1x LPI2C, up to 4x LPUART	USB and I3C functions need redesign or removal.
Motor control	FlexPWM and eQDC availability	1x FlexPWM, three submodules, six complementary outputs	PWM can migrate, but encoder/QDC logic must be redesigned.
Analog	ADC/CMP, no integrated Op Amp/PGA on MCX A153	16-bit ADC, CMP with 8-bit DAC, OpAmp with PGA	Opportunity to reduce external analog BOM.
Low power	58 µA/MHz Active, 6.47 µA power-down, 390 µA deep power-down	56 µA/MHz active, 2.91 µA power-down, 320 µA deep power-down typical conditions	Retest the current profile and wake-up time in the customer board.

3.2 Memory and clock migration

The memory and clock configuration must be rebuilt using the MCX C162 SDK and configuration tools. Do not reuse the MCX A153 linker file, startup file, vector table, or clock settings directly.

Table 4. Memory and clock migration checklist

Area	MCX A153 origin	MCX C162 destination	Required action
Program Flash	128 kB class	64 kB Flash, single-bank with ECC	Check `.text`, `.rodata`, boot metadata, data flash usage, and update reserve.
Data Flash	Customer implementation dependent	Up to 16 kB data flash, two 8 kB sectors	Recalculate EEPROM emulation layout and endurance budget.

Table 4. Memory and clock migration checklist*...continued*

Area	MCX A153 origin	MCX C162 destination	Required action
SRAM	32 kB class	12 kB RAM, all retainable down to Deep Power Down	Review `.data`, `.bss`, no-init, heap, and stack usage.
ECC	Flash and SRAM ECC options	Flash ECC plus up to 8 kB RAM with ECC	Reconfigure memory initialization and diagnostic tests.
Core clock	Up to 96 MHz	72 MHz maximum in standard drive mode	Recalculate timing constants and CPU margin.
FRO	FRO192M class source	FRO144M with 36/48/72/144 MHz selections, plus FRO12M and FRO16K	Regenerate clocks and validate communication/ PWM/ADC timing.
RTC clock	Application dependent	OSC32K supports an external 32.768 kHz crystal	Review XTAL_32K/EXTAL_ 32K pins and low-power current impact.

Recommended design gate: Before selecting MCX C162, ensure that the application image and all runtime data fit within 64 kB Flash and 12 kB RAM with margin. For customer designs using RTOS, large communication buffers, USB middleware, or signal-processing buffers, this is usually the first migration blocker.

4 Peripheral module migration

The following matrix classifies peripheral differences for firmware planning. A module marked as similar still requires instance, clock, trigger, DMA, interrupt, and pinmux review. A removed module must be removed from the firmware or replaced by an alternate implementation.

Table 5. Peripheral module migration matrix

Peripheral	MCX A153	MCX C162	Software driver comments
LPUART	Up to five LPUART depending on part/package	Up to 4x LPUART	Changed. Remap instances, pins, clock, IRQ, and DMA request.
LPI2C	1x LPI2C	1x LPI2C	Similar. Reconfigure pins and timing.
LPSPI	Up to 2x LPSPI	1x LPSPI	Changed. Check chip-select needs and peripheral clock.
USB FS	Supported	Not available	Removed. Replace USB bootloader, CDC, HID, or diagnostics path.
I3C	Supported	Not available	Removed. Use an I2C/SPI sensor alternative or keep MCXA153.
FlexPWM	1x FlexPWM, three submodules	1x FlexPWM, three submodules	Mostly portable. Recheck pinout, dead time, trigger, and fault logic.
eQDC/QDC	eQDC supported	Not available	Removed. Use timer capture/ GPIO decode or external decoder.

Table 5. Peripheral module migration matrix*...continued*

Peripheral	MCX A153	MCX C162	Software driver comments
CTimer	3x 32-bit timer class	Up to 2x 32-bit CTimer	Changed. Reassign compare/capture/PWM timer usage.
ADC	1x 16-bit ADC class	1x 16-bit ADC, up to 18 inputs, 2.4 Msps in 16-bit mode, 3 Msps in 12-bit mode	Changed. Remap channels, sample time, source impedance, FIFO, and calibration.
CMP	2x comparator class	1x high-speed comparator with eight input pins and 8-bit DAC	Changed. Remap threshold and comparator routing.
OpAmp/PGA	Not integrated	1x OpAmp with the PGA	Added. If gain, offset, bandwidth, and stability are validated, it can replace an external amplifier.
RTC	Not integrated	RTC with external XTAL support	Changed. Confirm low-power operation and crystal pins.

5 Hardware migration

5.1 Package and pinout migration

For the QFN32 package, MCXA153VFM and MCXC162VFM provide a highly compatible pinout for system pins and most GPIOs. Migration effort is associated mainly with peripheral function differences rather than PCB-level system circuitry changes.

Table 6 highlights the most important MCX C162 pins for a 48-pin migration review.

Table 6. Key MCXC162 pins for migration review, 48-pin package focus

Function group	MCXC162 signal/ pin name	H-PQFN48	LQFP48	Notes	Migration relevance
Reset	P1_29/RESET_B	5	3	Default ALT1 RESET_B	Preserve reset and programming entry.
ISP mode	P3_29/ISPMODE_N	25	25	Default ALT1 ISPMODE_N	Check bootstrap and manufacturing flow.
SWD/JTAG	P0_0/TMS/SWDIO	38	38	Default ALT1	Required for debug/ programming.
SWD/JTAG	P0_1/TCLK/ SWCLK	39	39	Default ALT1	Required for debug/ programming.
UART ISP	P0_2/LPUART0_ RXD	40	40	ISP UART_RXD	A common replacement for USB update flow.
UART ISP	P0_3/LPUART0_ TXD	41	41	ISP UART_TXD, CMP0_OUT ALT8	A common replacement for USB update flow.

Table 6. Key MCXC162 pins for migration review, 48-pin package focus*...continued*

Function group	MCXC162 signal/ pin name	H-PQFN48	LQFP48	Notes	Migration relevance
RTC clock	P1_30/XTAL_32K	6	4	Analog XTAL_32K	Required for external 32 kHz crystal.
RTC clock	P1_31/EXTAL_32K	7	5	ALT2 CLKIN, analog EXTAL_32K	Check crystal and clock input routing.
High-drive IO	P1_8/I2C_SDA capable	1	1	HD pad, ISP I2C_SDA	One of four 20 mA IO pins.
High-drive IO	P1_9/I2C_SCL capable	2	2	HD pad, ISP I2C_SCL	One of four 20 mA IO pins.
PWM high-drive	P3_1/PWM0_B0	35	34	HD pad	Useful for motor/ control output.
PWM high-drive	P3_0/PWM0_A0	36	35	HD pad	Useful for motor/ control output.
50 MHz IO	P1_0	45	45	MED + I2C_ FILT, ADC0_A16/ CMP0_IN3	High-speed IO and analog capable.
50 MHz IO	P1_1	46	46	MED + I2C_FILT, ADC0_A17	High-speed IO and analog capable.
50 MHz IO	P1_2	47	47	MED, ADC0_A18	High-speed IO and analog capable.
OpAmp/PGA	P2_12/OPAMP0_ INP0	16	15	ADC0_A5/ OPAMP0_INP0	OpAmp positive input.
OpAmp/PGA	P2_13/OPAMP0_ INN	17	16	OPAMP0_INN	OpAmp negative input.
OpAmp/PGA	P2_16/OPAMP0_ OUT	18	17	ADC0_A6/ OPAMP0_OUT/ CMP0_IN4P, ALT9	Configure ALT9 for OpAmp output path.
OpAmp/PGA	P2_17/OPAMP0_ INP1	19	18	OPAMP0_INP1	Alternative positive input.
Analog reference	P2_7/VREFI	15	14	ADC0_A7/ OPAMP0_EXT_ REF0	Reference or OpAmp external reference.
ADC/CMP	P2_2/ADC0_A4	12	11	ADC0_A4/CMP0_ IN0	ADC/comparator input.
PWM	P3_8/P3_9/P3_10/ P3_11	34/33/32/31	33/32/31/30	PWM0_A1/B1/A2/ B2	Other PWM output candidates.

Pinout migration rule: Do not migrate by package name only. Check reset, ISP, SWD, power, analog reference, ADC, OpAmp/PGA, PWM, UART, SPI, I2C, high-drive pins, and 50 MHz pins before schematic release.

5.2 Unused pin handling

Table 7. Recommended connection for unused MCXC162 pins

Pin type	Pin function	Data sheet recommendation	Migration note
Power	VDD	It must be powered	Required for the IO supply and internal modules.
Power	VDD_ANA	It must be powered	It must be at the same level as VDD and ramp together.
Reference	VREFH	Connect to VDD_ANA potential	Required for ADC reference behavior.
Reference	VREFL/VSS_ANA	Connect to VSS potential	Required for analog reference and ground.
Analog/non-GPIO	ADCn_x, EXTAL, XTAL	Float	Keep unused analog pins floating unless board-level constraints require otherwise.
GPIO/analog	Px/ADCn_x, Px/CMPn_INx	Float	Default analog input behavior must be considered.
Debug pins	JTAG_TCLK/TDI/TDO/TMS	Float by default	Disable unused debug pins in software if not needed; TCLK note recommends disabling for EMC.
GPIO/digital	Unused Px	Float	Default is disabled.

5.3 Analog front-end migration

For customers migrating from an MCX A153 design with external signal conditioning, MCX C162 can reduce external BOM by using the internal OpAmp/PGA together with the ADC and CMP. The analog path must still be electrically validated because source impedance, OpAmp output swing, ADC sampling time, gain error, offset, bandwidth, and settling time can directly affect measurement accuracy.

Table 8. Analog front-end migration checklist

Analog item	MCX C162 data point	Migration action	Validation evidence
ADC speed	Up to 2.4 Msps in 16-bit mode and 3 Msps in 12-bit mode in feature list	Set sample time and ADC clock based on source impedance.	ADC raw-code distribution, ENOB/SNR, gain/offset report.
ADC source resistance	External analog source resistance must be kept low; the operating table lists max RAS guidance	Review input RC filter and mux resistance.	Settling error at worst-case channel switching.
Comparator	One high-speed comparator, eight input pins, internal 8-bit DAC reference	Remap threshold and hysteresis configuration.	Threshold sweep and propagation delay test.
OpAmp	Input offset voltage is ±5 mV, output swing 0.2 V to VDD_ANA - 0.2 V, GBW high-speed typically 6 MHz	Check common-mode, output swing, and gain plan.	Gain, offset, bandwidth, and temperature test.
PGA	Gain accuracy is typically ±1 %. Bandwidth depends on gain	Select gain with bandwidth margin.	Step response and full-scale accuracy test.

6 Software migration

The recommended software migration is to create a clean MCX C162 SDK project and then port application-level code into the new project. This avoids hidden dependencies on MCX A153 startup code, vector tables, linker files, clock tree, removed peripherals, and peripheral instance numbers.

Table 9. Software migration checklist

Step	Migration task	Main risk	Recommended action
1	Create a clean MCX C162 SDK project	Wrong startup/linker/pinmux	Use target SDK and configuration tools.
2	Port board initialization	Clock and pin mismatch	Regenerate pins, clocks, peripherals, and power configuration.
3	Remove unsupported middleware	USB/I3C/eQDC dependency	Replace with UART/SPI/I2C alternatives or remove the feature.
4	Port peripheral drivers	Instance/channel differences	Update handles, IRQ names, DMA requests, triggers, and clocks.
5	Optimize memory	64 kB Flash/12 kB RAM budget	Review `.map` file, reduce buffers, tune stack/heap, remove dead code.
6	Benchmark timing	Lower core frequency and smaller CPU	Measure worst-case execution time and CPU load.
7	Validate analog	Gain/offset/noise changes	Run calibration and raw ADC code stability tests.
8	Regression test	Hidden behavior differences	Execute functional, low-power, production, and EMC-sensitive tests.

7 Validation recommendations

Do not release a migrated customer design based on compilation alone. The following evidence must be generated before production release:

- Build and memory report: Flash, RAM, heap, stack, and no-init region usage with margin.
- Timing report: worst-case ISR latency, PWM update, ADC trigger-to-result latency, and communication throughput.
- Analog report: ADC gain/offset/noise, OpAmp/PGA stability, comparator threshold accuracy, and temperature drift.
- Power report: active, sleep, deep-sleep, power-down, wake-up, reset, and brownout behavior.
- Manufacturing report: programming flow, debug access, serial number writing, calibration data, and board test coverage.
- System regression: full customer application behavior at voltage, temperature, and clock tolerance corners.

8 Recommended customer positioning

MCX C162 can be positioned as a cost-down migration target for MCX A153 designs when the application fits within 64 kB Flash and 12 kB RAM. It does not require USB FS, I3C, or eQDC, and benefits from integrated

analog resources. The migration must be positioned as a controlled redesign with schematic, pinout, firmware, and validation review, not as a drop-in replacement.

If the existing MCX A153 design uses USB for firmware update, large RAM buffers, encoder hardware decoding, complex middleware, or heavy real-time computation, MCX A153 must remain the preferred device unless those features are redesigned or removed.

9 Acronyms

Table 10 lists the acronyms used in this document.

Table 10. Acronyms

Acronym	Description
ADC	Analog-to-Digital Converter
BOM	Bill of Material
DMA	Direct Memory Access
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
FIFO	First In First Out
FRO	Free Running Oscillator
GPIO	General-Purpose Input/Output
HID	Human Interface Device
I3C	Improved Inter-Integrated Circuit
IO	Input/Output
IRQ	Interrupt Request
ISR	Interrupt Service Routine
JTAG	Joint Test Action Group
LPI2C	Low-Power Inter-Integrated Circuit
LPSPI	Low-Power Serial Peripheral Interface
LPUART	Low-Power Universal Asynchronous Receiver/Transmitter
MCU	MicroController Unit
NVM	Non-Volatile Memory
PCB	Printed-Circuit Board
PGA	Programmable Gain Amplifier
PWM	Pulse Width Modulation
RTC	Real-Time Clock
RTOS	Real-Time Operating System
SDK	Software Development Kit
SNR	Signal-to-Noise Ratio
SRAM	Static Random-Access Memory
SWD	Serial Wire Debug

10 References

- Migration Guide from MCXN to MCXA (AN14208)
- MCX C151/161/162 Data Sheet (MCXCP048M072F20)
- MCX A132/133/142/143/152/153 Data Sheet (MCXAP064M096F30)
- MCX A144/145/146/154/155/156 Data Sheet (MCXAP100M096F60)

11 Revision history

Table 11 summarizes the revisions to this document.

Table 11. Revision history

Document ID	Release date	Description
AN15136 v.1.0	10 September 2026	Initial public release

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