AN15030

External Hardware Design to Generate CP-PWM Signal Using SIGBRD-HPGP Board

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Document information

Information	Content
Keywords	AN15030, SIGBRD-HPGP board, MCX A154 MCU, electric vehicle (EV), EV charging signal board, sigboard, Home Plug GreenPHY, high-level communication, PLC, ISO 15118, AC charging, DC charging, PWM, control pilot (CP), LIN, LIN-CP
Abstract	This document describes the components required to design external hardware for generating Control Pilot PWM using the SIGBRD-HPGP board. The SIGBRD-HPGP board is an essential component in the EV charger implementation.

1 Introduction

The SIGBRD-HPGP board is an add-on development board used in EV charging solutions. The board has HomePlug GreenPHY (Lumissil CG5317) through SPI and Ethernet host connection interfaces for Control Pilot (CP) connection. In addition, this SIGBRD-HPGP board has an EV side CP-PWM detection circuit only.

This document describes the components required to design external hardware for generating CP-PWM using the SIGBRD-HPGP board. The SIGBRD-HPGP board is an essential component in the EV charger implementation. The SIGBRD-HPGP board also supports the other type of control pilot signal, named 'LIN-CP' for EV supply equipment (EVSE) or EV side of setups.

2 Required hardware

To provide complete the CP functionality, it is required to generate a control pilot signal and detect PWM high-level voltage. The CP signal swings between +12 V to -12 V.

SIGBRD-HPGP has a boost converter to generate +12 V from +5 V. Therefore, to generate -12 V, a charge pump inverter is required inside an external hardware.

To generate and detect CP-PWM, you need an additional circuit shown in Figure 1.

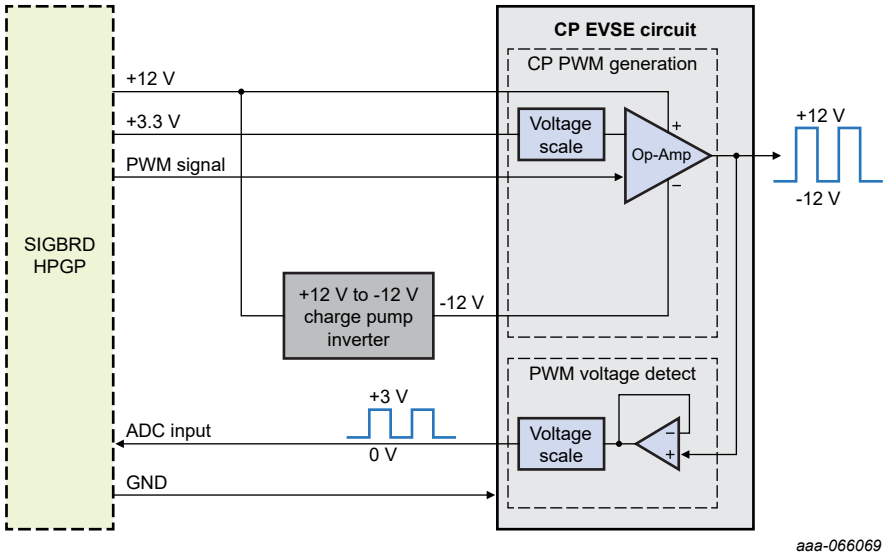

Figure 1. Required circuit

2.1 Charge pump inverter

The CP-PWM signal has a swing between +/-12 V. As the microcontroller MCXA154VFT generates a PWM of 3.3 V level, we need +12 V and -12 V to shift the level of the PWM.

SIGBRD-HPGP only generates +12 V by the boot converter. Therefore, the external charge pump inverted is needed to generate -12 V from +12 V.

Figure 2 shows generation of -12 V from +12 V.

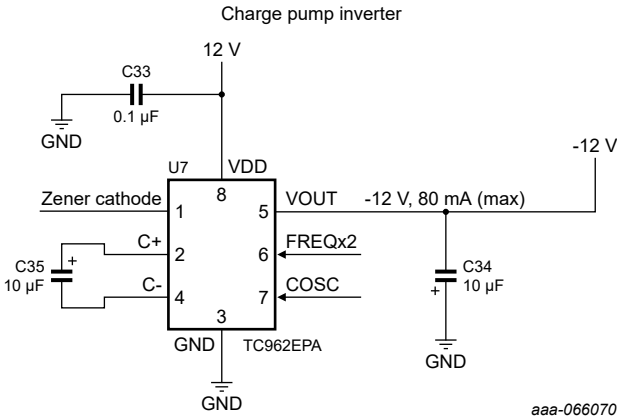

Figure 2. Charge pump inverter circuit

2.2 PWM generation and detection circuit

The CP circuit in the EVSE side has two parts:

- Generation of PWM, and
- Detection of PWM level

Figure 3 shows the generation and detection of CP-PWM signal.

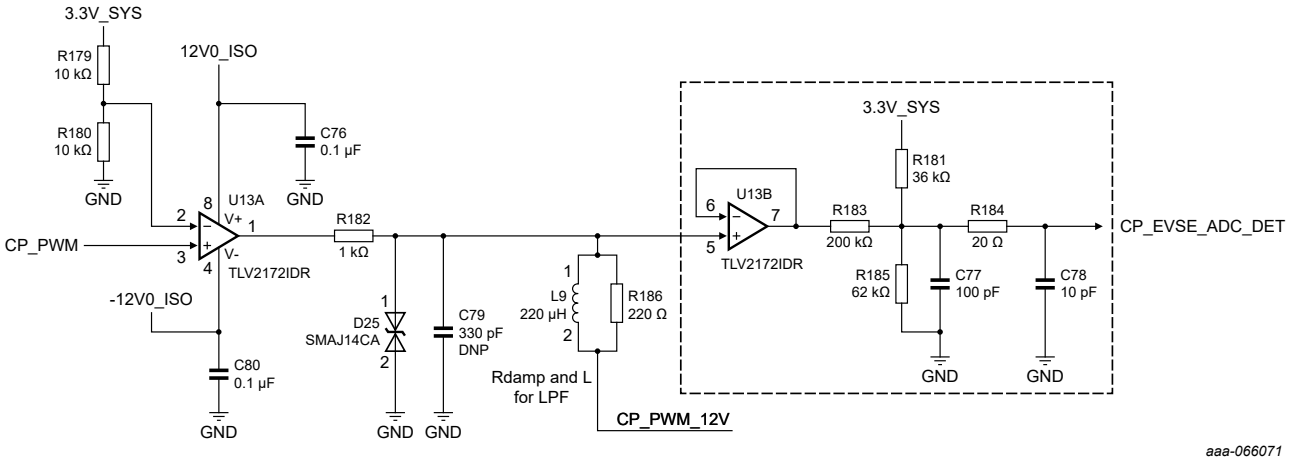

Figure 3. PWM generation and detection circuit

2.2.1 PWM generation circuit

The CP_PWM signal comes from SIGBRD-HPGP. This 3.3 V signal is then amplified to a -12 V to +12 V signal using an Operational Amplifier to generate CP_PWM_12V.

The core of the operation is the TLV2172 Operational Amplifier (U13A), which is configured here as a comparator. The U13A compares the incoming logic-level signal (CP_PWM) at the noninverting input, against a reference voltage created by the R179/R180 divider. The U13A is powered by the bipolar rails (+12V0_ISO and -12V0_ISO). Therefore, it amplifies the 0 V to 3.3 V input voltage into a full-swing ±12 V square wave.

To ensure signal integrity and circuit protection, the output passes through a TVS diode (D25), which clamps high-voltage transients to prevent damage from external surges.

The final stage is a damped low-pass filter formed by inductor L9 and resistor R186. This filter helps to smoothen the high-frequency transitions and manage impedance before the signal exits as CP_PWM_12V to communicate with the Electric Vehicle.

When the CP_PWM_12V signal is connected to an EV, the EV circuit drops the voltage to signal charging.

2.2.2 Detection circuit

In Figure 3, the circuit shown on the right is used to detect the voltage change in the CP_PWM_12V signal. The TLV2172 Operational Amplifier, configured as a voltage follower provides a high-impedance input. The voltage follower buffers the incoming signal without any distortion by the downstream components.

After buffering, the signal enters a biasing and scaling network. In this scaling network, the Resistors R183, R181, and R185 attenuate the voltage and shift it into a positive 0 V to 3.3 V range. This process ensures protecting the ADC from negative or overvoltage conditions.

Finally, the filtering stage consisting of C77, C78, and R184 cleans the signal. This filter circuit removes the high-frequency noise and stabilizes the output for precise digital sampling.

3 External Hardware connections with SIGBRD-HPGP

The external hardware requires 5 input/output connections and a ground shorting. These connections shown in Table 1 can be easily taken out from SIGBRD-HPGP from the jumpers and Arduino connectors.

Table 1. Input/output connection from SIGBRD-HPGP

Signal	Jumper header
+12 V	J40:2
+3.3 V	J29:2
CP_PWM	J31:1
CP_ADC	J31:4
GND	J2:14

Note: *The jumpers mentioned in Table 1 are not mandatory and the signals can be taken from the other jumpers/headers as per the design convenience.*

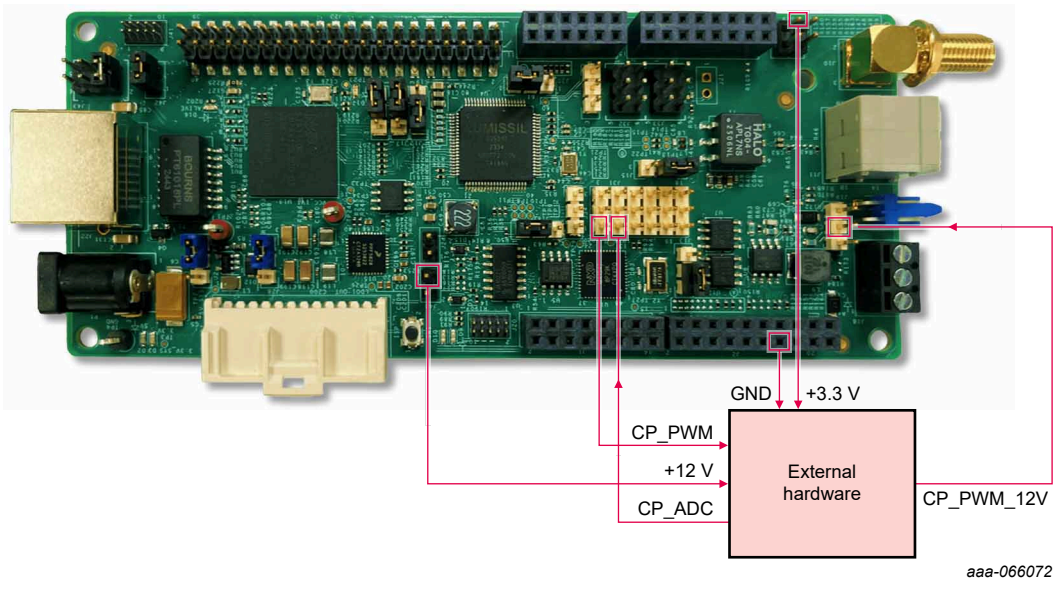

Figure 4. IO connections with external Hardware

4 Acronyms

Table 2 lists the acronyms used in this document.

Table 2. Acronyms

Acronym	Description
ADC	Analog-to-digital converter
CP	Control Pilot
ESP	Enhanced Serial Protocol
EV	Electric Vehicle
EVSE	Electric Vehicle Supply Equipment
GND	Ground
HPGP	Home Plug Green PHY
IP	Internet Protocol or Intellectual Property
IPsec	Internet Protocol Security
LIN	Local Interconnect Network
PWM	Pulse Width Modulation
RDB	Reference Design Board
SIB	Small cell IPsec Backhaul
SIGBRD	Signal Board
SPI	Serial Peripheral Interface
TAP	Test Access Port
TVS	Transient Voltage Suppression

5 Revision history

Table 3 summarizes the revisions to this document.

Table 3. Revision history

Document ID	Release date	Description
AN15030 v.1.0	27 May 2026	Initial public release

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Contents