AN14994

Continuous SRAM Address Usage on MCX A173 and MCX A174

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Document information

Information	Content
Keywords	AN14994, MCX, MCX A, MCX A173, MCX A174, SRAM address usage
Abstract	This application note explains the memory architecture, alias mechanism, REMAP behavior, available continuous address range, and provides step-by-step linker configuration examples for MCUXpresso (VS Code and IDE), IAR, and Keil.

1 Introduction

MCX A173 and MCX A174 devices support a continuous Static Random-Access Memory (SRAM) address space by using the SRAM X0 alias region. This feature enables multiple physically separated SRAM banks to appear as one linear memory region on the system bus, simplifying Direct Memory Access (DMA) operations and supporting applications that require large contiguous memory buffers, such as graphics or audio processing.

This application note explains the memory architecture, alias mechanism, REMAP behavior, available continuous address range, and provides step-by-step linker configuration examples for MCUXpresso (VS Code and IDE), IAR, and Keil.

2 Memory architecture overview

The MCX A series introduces a configurable continuous SRAM address space using the SRAM X0 alias region. Major advantages include:

- A single linear system RAM region simplifies buffer allocation.
- DMA engines benefit from continuous address mapping without manually breaking transfers by bank.
- Suitable for larger composite memory needs, such as graphics framebuffers or AI preprocessing buffers.

Note: *SRAM X0 alias does not provide more physical RAM. It maps to the same physical SRAM X0 (8 kB). Reading/writing to the alias region are equivalent to accesses on* `0x0400_0000-0x0400_1FFF`.

2.1 Memory map

Table 1 describes the memory map of MCX A174, which can be found in the attachment of Reference Manual.

For MCX A173, the address of SRAM X0 alias follows the end of SRAM B0, which offers a continuous address space with SRAM A0, A1, B0 (8 kB), 32 kB SRAM in total with continuous address.

Table 1. MCX A174 memory map

Start address (hex)	End address (hex)	Size (kB)	Description
Code bus memory			
04000000	04001FFF	8	SRAM X0 (Slave Port 0)
04002000	04003FFF	8	SRAM X1 (Slave Port 0)
System RAM			
20000000	20001FFF	8	SRAM A0 (Slave Port 3)
20002000	20003FFF	8	SRAM A1 (Slave Port 3)
20004000	20007FFF	16	SRAM B0 (Slave Port 4), only applied to MCX A174
20008000	2000BFFF	16	SRAM C0 (Slave Port 5), only applied to MCX A174
2000C000	**2000DFFF**	**8**	**SRAM X0 alias, only applied to MCX A174**

Table 2 describes the memory map of the MCX A173, which can be found in the attachment of Reference Manual.

For MCX A174, the address of SRAM X0 alias follows the end of SRAM C0, which offers a continuous address space with SRAM A0, A1, B0, C0, 58 kB SRAM in total with continuous address.

Table 2. MCX A173 memory map

Start address (hex)	End address (hex)	Size (kB)	Description
Code bus memory			
04000000	04001FFF	8	SRAM X0 (Slave Port 0)
04002000	04003FFF	8	SRAM X1 (Slave Port 0)
System RAM			
20000000	20001FFF	8	SRAM A0 (Slave Port 3)
20002000	20003FFF	8	SRAM A1 (Slave Port 3)
20004000	20005FFF	8	SRAM B0 (Slave Port 4), only applied to MCX A173
20006000	**20007FFF**	**8**	**SRAM X0 alias, only applied to MCX A173**

2.2 Memory architecture

Figure 1 describes the memory architecture of MCX A173 and MCX A174.

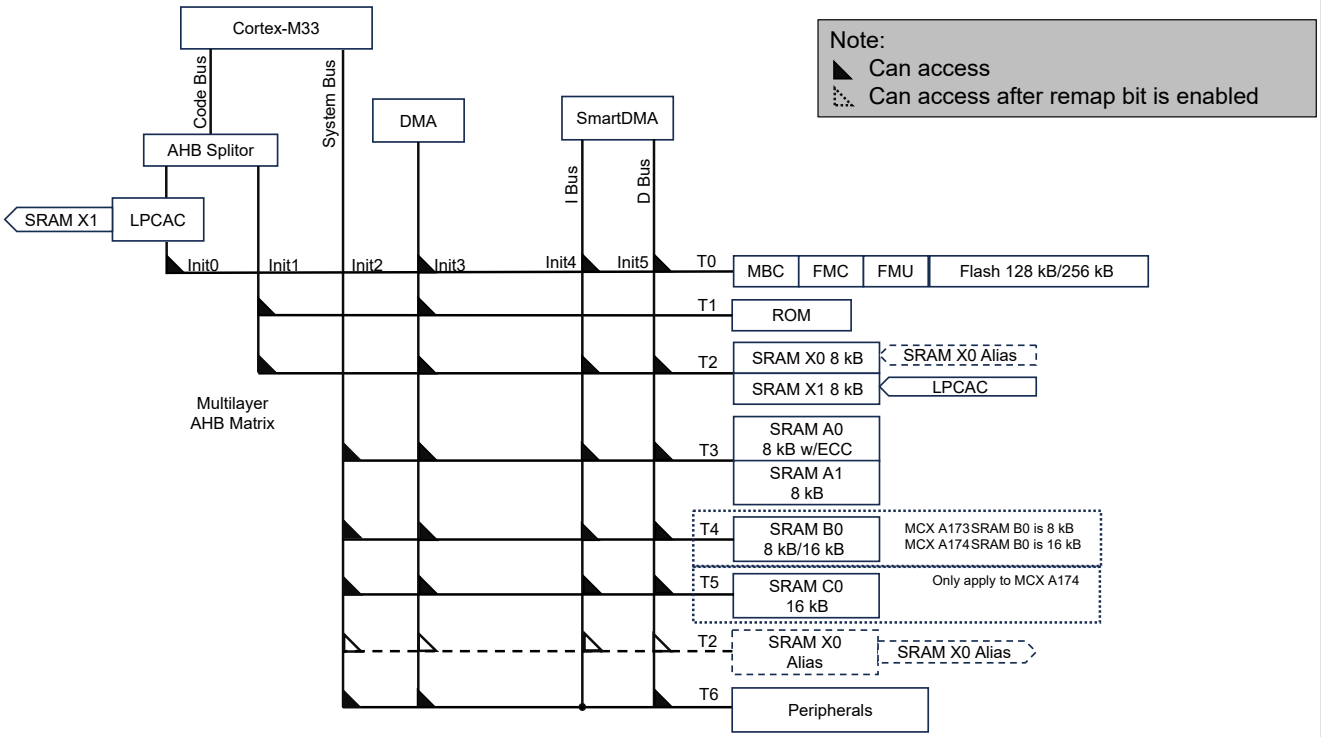

Figure 1. Memory architecture

The SRAM X0 alias region is set as Alias mode to `DMA0` and `CPU0_SBUS` by default (AHB Matrix Remap Control - REMAP register value is `0x01000104` after boot-up). The Cortex-M33 system bus and DMA can access up to 32 kB (MCX A173) or 58 kB (MCX A174) continuous address. MCX A173 and MCX A174 enabled the remap bit. Both SRAM X0 (`0x04000000`-`0x04001FFF`) and SRAM X0 alias (MCX A173: `0x20006000`-`0x20007FFF` or MCX A174: `0x2000C000`-`0x2000DFFF`) region can be accessed. When accessing the SRAM X0 alias address, the SRAM X0 alias address is translated into the corresponding SRAM X0 address, and then SRAM X0 is accessed.

To use SRAM X0 only through the code bus (`0x04000000` to `0x04001FFF`), disable the corresponding `CPU0_SBUS`, DMA, and SmartDMA bits of the AHB Matrix Remap Control (Remap) register in System Control

(SYSCON) module (set with 00b). For example, define SRAM X0 to Cortex-M33's code bus access only to get a better CPU performance.

Note: *Cortex-M33 accesses SRAM X0 alias region through the system bus, while accesses SRAM X0 region through the code bus.*

3 Configuration steps

Unlike the MCX A13x/14x/15x, there are no usage limitations on MCX A173 and MCX A174.

The following are the detailed steps of using SRAM X0 alias to the system bus with different IDEs.

3.1 MCUXpresso for Visual Studio Code

This section introduces how to modify the project code to implement continuous SRAM address in MCUXpresso IDE.

- For MCX A174, as shown in Figure 2:
  1. Modify the size of SRAM to include the SRAM X0 alias region.
  2. Modify the location and size of SRAMX to reserve SRAM X0 region to ensure the data security.
  3. Change the SRAM size from 0xC000 to 0xE000, including the SRAM X0 alias region.
  4. Remove the SRAM X0 region, which has been merged into the unified SRAM address space.

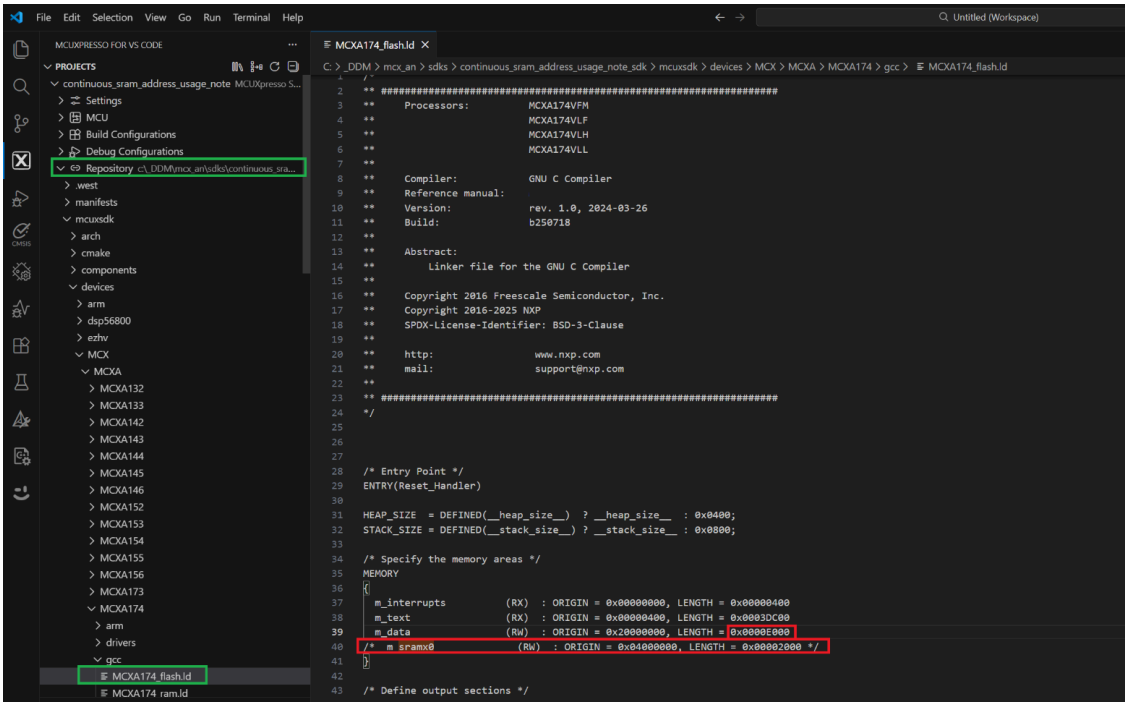

Figure 2. MCX A174 SRAM settings in MCUXpresso for VSC

- For MCX A173, as shown in Figure 3:
  1. Modify the size of SRAM to include the SRAM X0 alias region.
  2. Modify the location and size of SRAMX to reserve SRAM X0 region to ensure the data security.
  3. Increase the SRAM size from 0x6000 (or 0x4000) to 0x8000 by including the SRAM X0 alias region.
  4. Remove the SRAMX0 region, which has been merged into the unified SRAM address space.

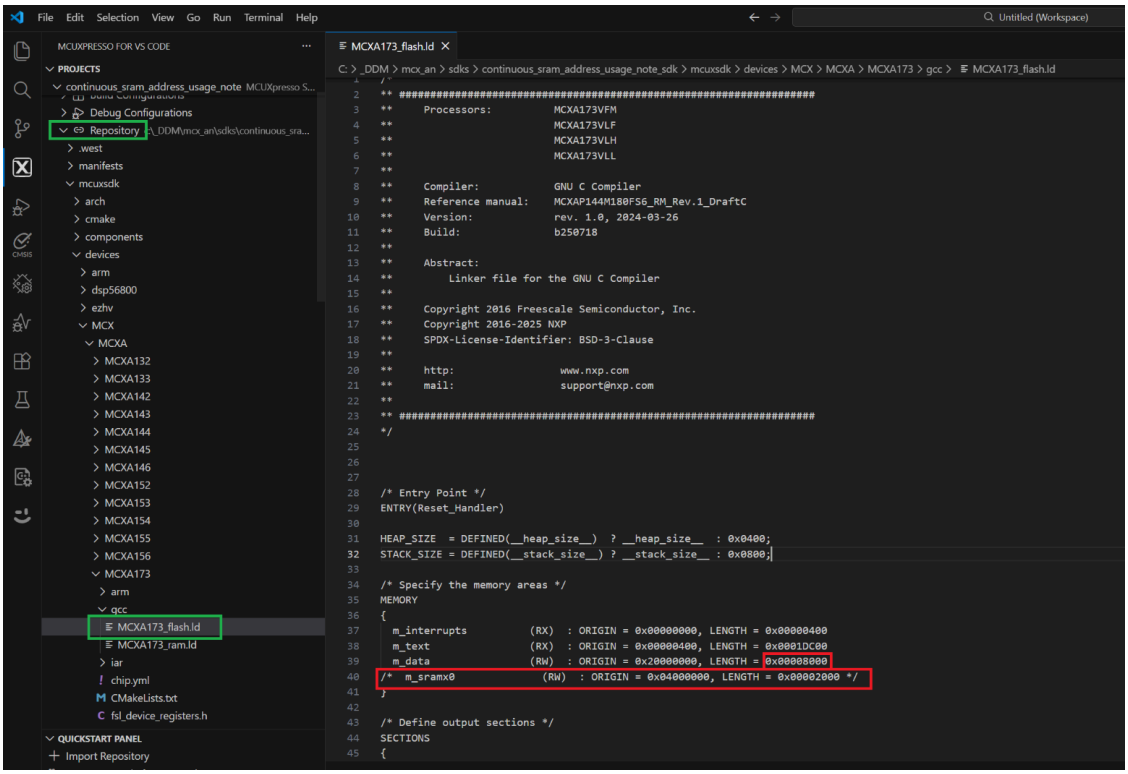

Figure 3. MCX A173 SRAM settings in MCUXpresso for VSC

3.2 MCUXpresso IDE

This section introduces how to modify the project code to implement continuous SRAM address in MCUXpresso IDE.

- For MCX A174, as shown in Figure 4:
  1. Modify the size of SRAM to include the SRAM X0 alias region.
  2. Modify the location and size of SRAMX to reserve SRAM X0 region to ensure the data security.
  3. Change SRAM Size from `0xC000` to `0xE000`, including the SRAM X0 alias region.
  4. Remove the SRAMX0 region, which has been merged into the unified SRAM address space.
  5. Remove the SRAMX1 region, as it is reserved for LPCAC by default.

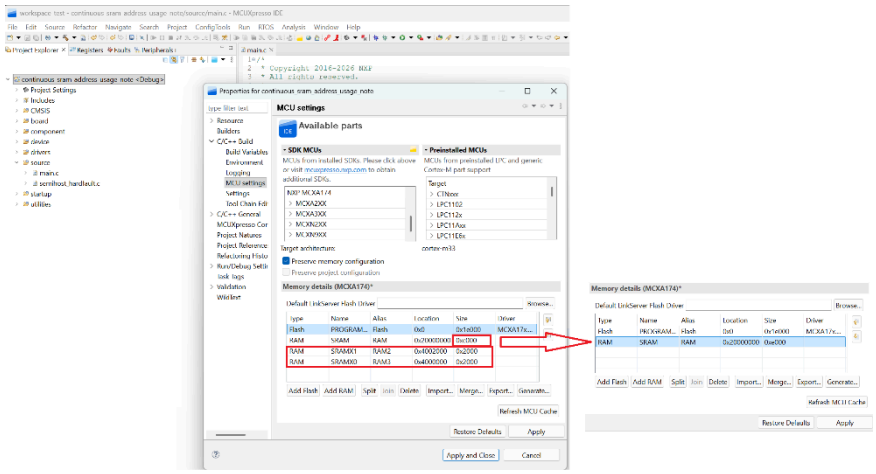

Figure 4. MCX A174 SRAM settings in MCUXpresso IDE

- For MCX A173, as shown in Figure 5:
  1. Modify the size of SRAM to include the SRAM X0 alias region.
  2. Modify the location and size of SRAMX to reserve SRAM X0 region to ensure the data security.
  3. Change the SRAM size from `0x6000` (or `0x4000`) to `0x8000`, including the SRAM X0 alias region.
  4. Remove the SRAMX0 region, which has been merged into the unified SRAM address space.
  5. Remove the SRAMX1 region, as it is reserved for LPCAC by default.

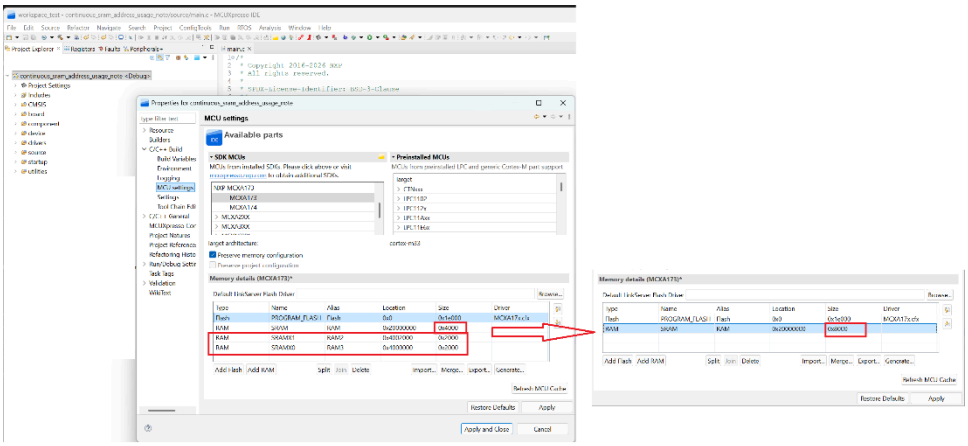

Figure 5. MCX A173 SRAM settings in MCUXpresso IDE

3.3 IAR IDE

This section introduces how to modify the project code to implement continuous SRAM address in IAR IDE.

- For MCX A174, as shown in Figure 6:
  1. Modify the `m_data_end` to include the SRAM X0 alias region.
  2. Modify the `DATA_region` to reserve SRAM X0 region to ensure the data security.
  3. Change the `m_data_end` value from `0x2000BFFF` to `0x2000DFFF`, including the SRAM X0 alias region.
  4. Comment out `m_sramx0_start` and `m_sramx0_end`, as SRAMX0 acts as an alias region.
  5. Add ";" after defining the region `DATA_region` and comment out the `| mem:[from m_sramx0_start to m_sramx0_end];`.

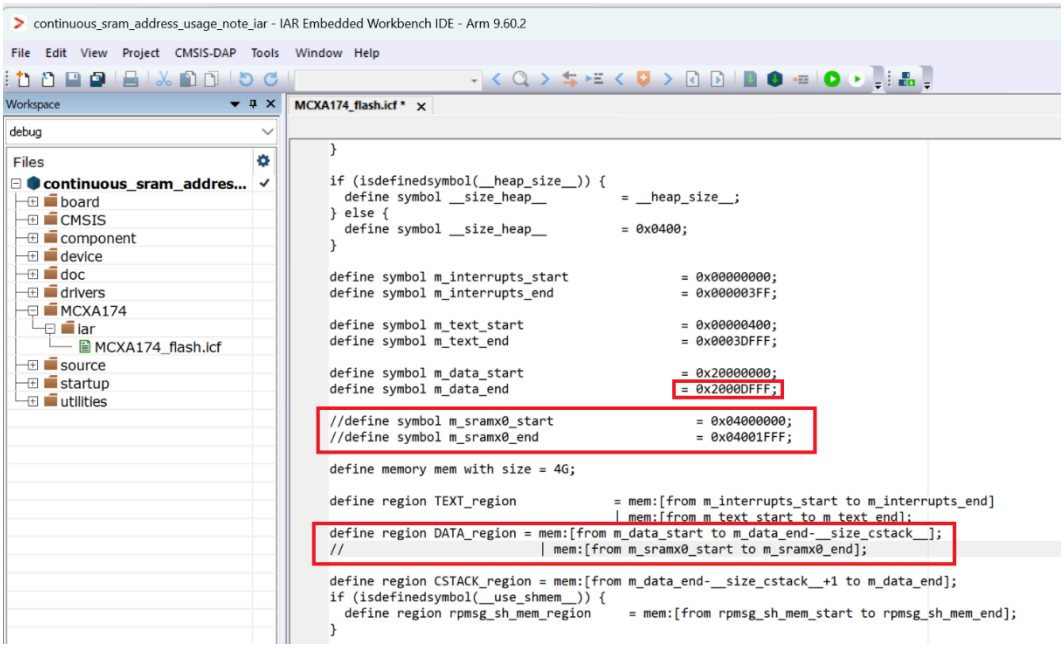

Figure 6. MCX A174 SRAM settings in IAR IDE's linker file

- For MCX A173, as shown in Figure 7:
  1. Modify the `m_data_end` to include the SRAM X0 alias region.
  2. Modify the `DATA_region` to reserve SRAM X0 region to ensure the data security.
  3. Change the `m_data_end` value from `0x20005FFF` (or `0x20003FFF`) to `0x20007FFF`, including the SRAM X0 alias region.
  4. Comment out `m_sramx0_start` and `m_sramx0_end`, as SRAMX0 acts as an alias region.
  5. Add `;` after defining the region `DATA_region` and comment out the `| mem:[from m_sramx0_start to m_sramx0_end];`.

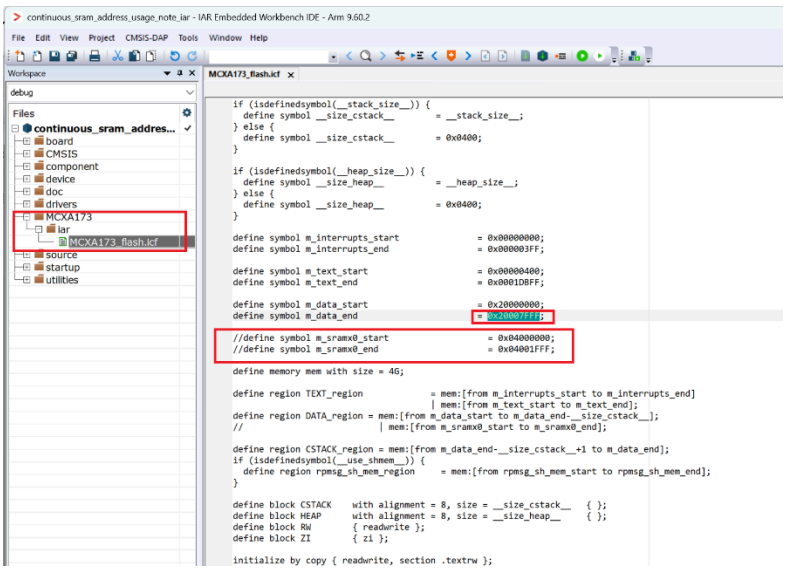

Figure 7. MCX A173 SRAM settings in IAR IDE's linker file

3.4 KEIL IDE

This section introduces how to modify the project code to implement continuous SRAM address in Keil IDE. The steps are described below:

- For MCX A174, as shown in Figure 8:
  1. Modify the `m_data_size` to include the SRAM X0 alias region.
  2. Configure the scatter (*.*sct*) file of the project.
  3. Update `m_data_size` from `0x0000C000` to `0x0000E000`.
  4. Comment out `m_sramx0_start` and `m_sramx0_size`, as SRAMX0 acts as an alias region.

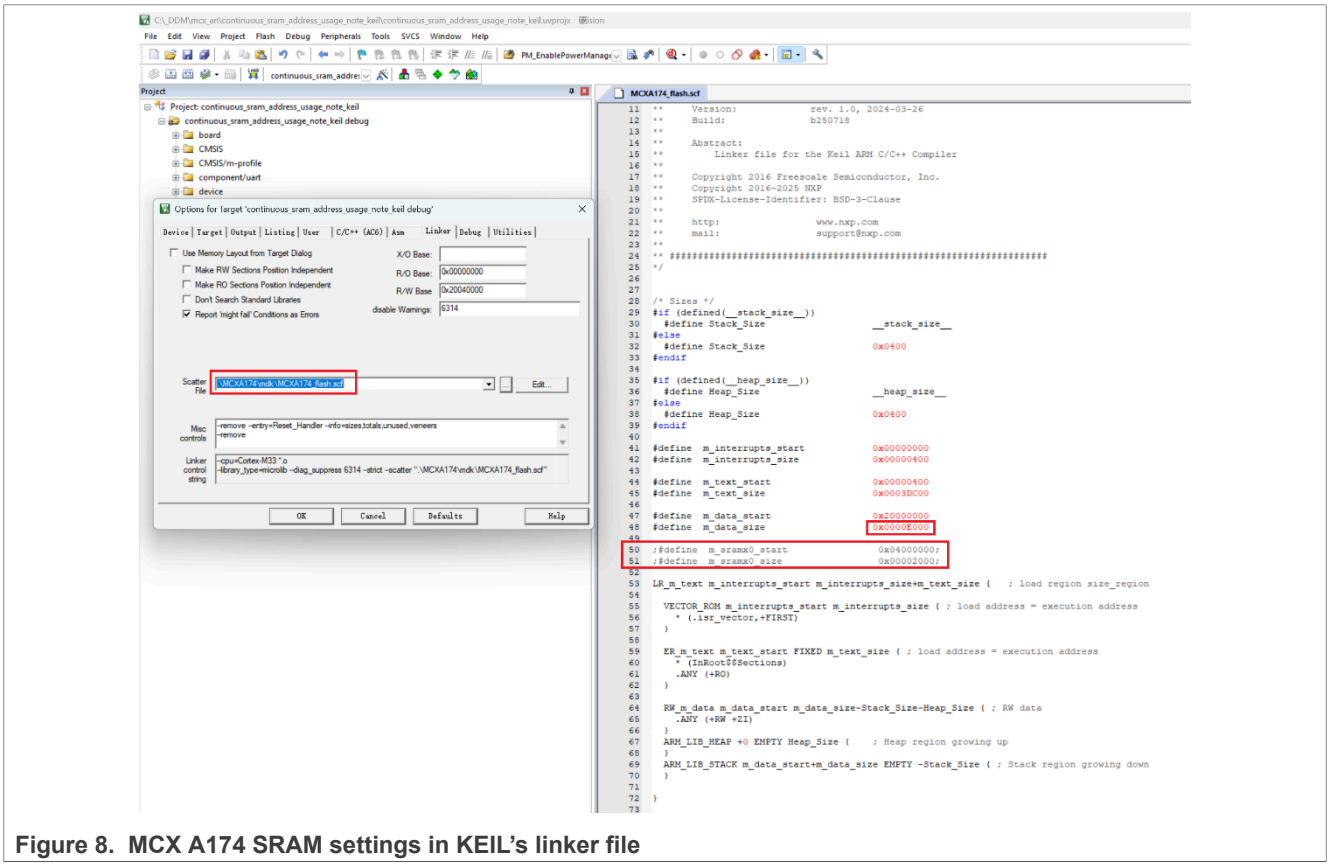

Figure 8. MCX A174 SRAM settings in KEIL's linker file

- For MCX A173, as shown in Figure 9:
  1. Modify the `m_data_size` to include the SRAM X0 alias region.
  2. Configure the scatter (*.*sct*) file of the project.
  3. Update `m_data_size` from `0x00006000` (or `0x00004000`) to `0x00008000`.
  4. Comment out `m_sramx0_start` and `m_sramx0_size`, as SRAMX0 acts as an alias region.

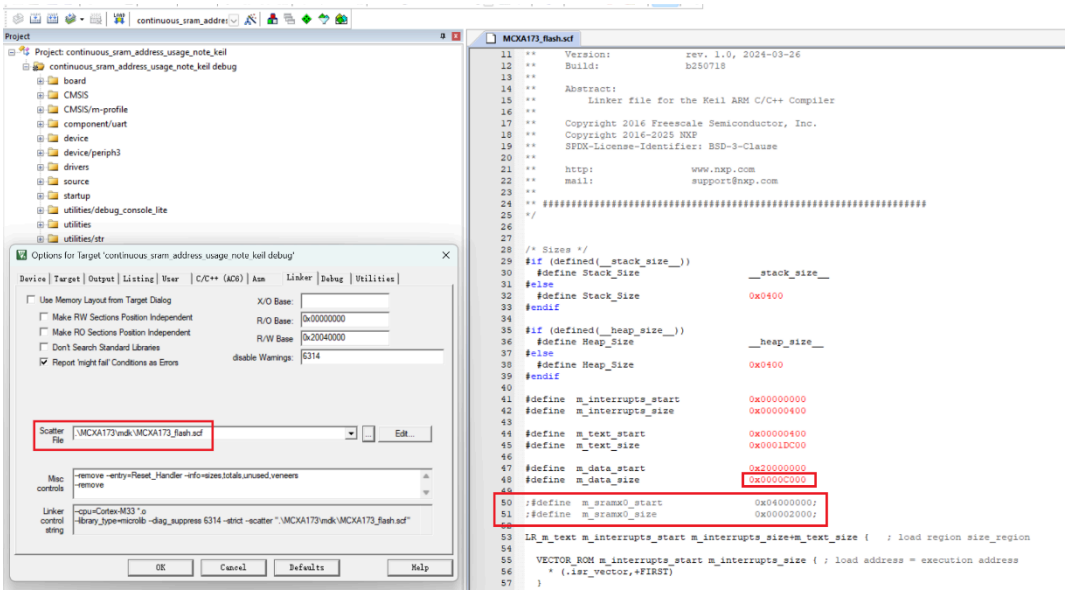

Figure 9. MCX A173 SRAM settings in KEIL's linker file

4 Summary

This application note introduces how to configure and use the SRAM X0 alias to form a continuous SRAM address and provides a demo to validate the feasibility of a continuous SRAM address.

5 References

The following are some additional documents that you can refer to for more information on the MCX A343 and A344 devices:

- *MCX A343 and A344 Data Sheet* (document MCXAP100M180F40)
- *MCXA343 and A344 Reference Manual* (document MCXAP100M180F40RM)
- *FRDM-MCXA344 Board User Manual* (document UM12441)
- *Continuous SRAM Address Usage on MCXA15x* (document AN14377)

6 Acronyms

Table 3 lists the acronyms used in this document.

Table 3. Acronyms

Acronym	Description
ADC	Analog-to-Digital Converter
AOI	AND/OR/INVERT
BGA	Ball grid array
CAN	Controller Area Network
CMC	Core Mode Controller
DAC	Digital-to-Analog Converter

Table 3. Acronyms...*continued*

Acronym	Description
DMA	Direct memory access
DVFS	Dynamic voltage and frequency scaling
DWT	Data Watchpoint and Trace
ECC	Error correction code
EIM	Error Injection Module
EMC	Electromagnetic compatibility
ERM	Error recording module
ESD	Electrostatic discharge
FD	Flexible data rate
FlexCAN	Flexible Data Rate Controller Area Network
FlexIO	Flexible Input/Output
FlexPWM	Flexible Pulse Width Modulator
FMC	Flash Memory Controller
FMU	Flash Memory Module
FS	Full speed
GPIO	General-purpose input/output
HVD	High-Voltage Detect
HVQFN	Heat sink, very thin, quad flat package, non-leaded
I/O	Input/output
I^2C	Inter-Integrated Circuit
I3C	Improved Inter-Integrated Circuit
ISP	In-system programming
ITM	Instruction Trace Macro cell
JTAG	Joint Test Action Group
LCD	Liquid-crystal display
LFBGA	Low-profile, fine pitch, ball grid array
LPCAC	Low-Power Cache Controller
LPI2C	Low-Power Inter-Integrated Circuit
LPSPI	Low-Power Serial Peripheral Interface
LPUART	Low-Power Universal Asynchronous Receiver/Transmitter
LQFP	Low-profile, quad flat package
LVD	Low-Voltage Detect
MBC	Memory Block Checker
MCU	Microcontroller unit
OpAmp	Operational amplifier
OS	Operating system

Table 3. Acronyms...*continued*

Acronym	Description
QDC	Quadrature Decoder
QFN	Quad flat package, non-leaded
QFP	Quad flat package
RAM	Random-access memory
SOSC	System oscillator
SPC	System Power Control
SRAM	Static random-access memory
SWD	Serial wire debug
SWO	Serial wire debug trace data output
TCM	Tightly coupled memory
TDI	Test data input
TDO	Test data output
TMS	Test mode select
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VFBGA	Very thin, fine pitch, ball grid array
WUU	Wake-Up Unit

7 Note about the source code in the document

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8 Revision history

Table 4 summarizes the revisions to this document.

Table 4. Revision history

Document ID	Release date	Description
AN14994 v.1.0	16 April 2026	Initial public release

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