AN14982

Battery Monitoring in MCX L255

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Document information

Information	Content
Keywords	AN14982, MCX L255 MCUs, MCX devices, battery monitoring, ADC, power modes
Abstract	This document describes measuring and periodic monitoring of device supply or battery voltage and enabling monitoring in low power modes with low battery interrupts alert feature.

1 Introduction

This application note describes the process to measure and periodically monitor the supply or battery voltage, which powers the device. Either Low-Power Analog-to-Digital Converter (LPADC) or High-Speed Analog-to-Digital Converter (HSADC) is used for battery voltage measurement. In low-power modes, the Counter Timer (CTimer) or Low-Power Timer (LPTimer) are required to facilitate optimized Analog-to-Digital Converter (ADC) operation.

For more information about the device peripherals, refer to the *MCX L25x Reference Manual* (MCXLP184M096F50RM).

This document also describes the methods to measure battery voltage in Low-Power mode. For more information on low-power modes, refer to the *MCX L25x Reference Manual* (MCXLP184M096F50RM) or *Implementing MCX L25x Low-power Mode* (AN14949).

2 MCX L255 overview

The MCX L255 Microcontroller Units (MCUs) expand the MCX Arm Cortex-M33 product offerings with a dual-core microcontroller. It features a real-time (or Main) domain with a CM33 core operating at frequencies up to 96 MHz, and an Ultra-Low-Power (ULP) sense (or AON) domain with a CM0+ core operating up to 10 MHz.

This dual-domain combination allows to address low-power applications requiring Always-on (AON) data monitoring, processing, or communication, especially on battery operating devices. This device has two ADCs: an HSADC located in the Main domain and an LPADC located in the AON domain.

3 Voltage measurement using ADC

The ADC module performs analog-to-digital conversions on any of the software-selectable analog input channels using a successive approximation algorithm. The selectable trigger events from software or hardware sources initiate the conversions.

3.1 Voltage reference

The ADC provides both low and high-voltage references, called Voltage Reference High (VREFH) and Voltage Reference Low (VREFL).

MCX L255 provides multiple VREF options for ADC. Following are the options for both HSADC and LPADC:

The HSADC voltage references can be selected using CFG[REFSEL]:

• CFG[REFSEL]=00: Selects VDD_ANA for the QFP100 package and dedicated VREFH pin for the BGA184 package.

• CFG[REFSEL]=01: Selects VREFI (provides an option to use the onboard accurate voltage through the P3_0 pin).

• CFG[REFSEL]=10: Selects the VDD_ANA supply pin.

The LPADC voltage references can be selected using CFG[REFSEL]:

• CFG[REFSEL]=0: Selects VDD_ANA_LPADC.

• CFG[REFSEL]=1: Selects VDD_ANA_LPADC.

The VREFL voltage reference in both the ADCs is always connected to VSSA (Analog ground).

3.2 ADC trigger inputs

The ADC can either be triggered using software or hardware (from other peripherals). HSADC and LPADC trigger inputs can be routed to other peripherals using Main domain INPUTMUX and the AON domain INPUTMUX, respectively. Hardware triggers can be enabled by setting the Trigger Enable bit in the Trigger Control register (TCTRLx[HTEN]).

3.3 ADC channel input

Both the Main domain ADC and the AON domain ADC provide multiple input channels.

3.4 ADC result output

The ADC output is a 12-bit to 16-bit unsigned value. The result output represents a voltage sensed by the ADC at the channel input.

The following equations describe the relationship between the ADC result and the channel voltage:

Channel voltage calculation

$$\text{Channel Voltage} = \frac{\text{ADC result output}}{2^r} \times \left(\text{VREFH} - \text{VREFL}\right) \quad (1)$$

Note: *'r' represents the ADC output resolution.*

ADC result output calculation

$$\text{ADC result output} = \frac{\text{Channel Voltage}}{\left(2^r - 1\right)} \times \left(\text{VREFH} - \text{VREFL}\right) \quad (2)$$

Note: *'r' represents the ADC output resolution.*

In the MCX L255 device, the VREFL is always connected to the ground, meaning: VREFL = 0 V.

Therefore, the ADC result output depends on channel voltage and VREFH. As the VREFH voltage is fixed, the ADC result output depends on the channel voltage only.

3.5 Battery voltage calculation

The battery voltage or supply voltage can be measured when it is connected to the VREFH pin of the ADC.

Section 3.5 describes that the ADC result is dependent on channel voltage and VREFH. If the voltage supplied at the ADC channel is fixed and VREFL = 0 V, the VREFH voltage can be calculated using the ADC result output.

VDD_ANA can be selected as the VREFH source, and the reference voltage can be computed using the equation shown below.

$$\text{VREFH} = 2^r \times \frac{\text{Channel Voltage}}{\text{ADC result output}} \quad (3)$$

If 'r' = 16, channel voltage = 1.2 V

$$\text{VREFH} = 65535 \times \frac{1.2\,V}{\text{ADC result output}} \quad (4)$$

$$\text{VREFH} = \left(2^r - 1\right) \times \frac{\text{Channel Voltage}}{\text{ADC result output}} \quad (5)$$

If 'r' = 16, channel voltage = 1.2 V

$$\text{VREFH} = 65535 \times \frac{1.2\,V}{\text{ADC result output}} \quad (6)$$

In MCX L255, the band gap reference circuit is used to provide a stable reference voltage.

3.6 Band gap reference as a fixed voltage source

A band gap reference is an analog circuit that generates a voltage that is designed to remain stable across temperature, supply voltage, and process variations. The MCX L255 device includes a band gap module, which provides a stable output of 1.2 V.

3.6.1 Enabling band gap and band gap measurement using ADC

The band gap can be enabled using the BG_EN bit in the band gap Reference Control register (BGR_CTRL[BG_EN]).

The band gap buffer must be enabled using band gap Buffer Enable bit (BRG_CTRL[BG_BUFFEN]) to enable band gap voltage on ADC channel.

In the MCX L255, the band gap voltage is connected to channel number twenty-seven on both ADC modules.

The ADC channel can be selected using ADC channel-selection bits in the Command Low Buffer register (CMDLx[ADCH]).

3.7 Autonomous battery monitoring using Compare function in ADC

The ADC Compare function enables automatic detection of low-battery conditions by comparing each conversion result against a preset threshold. It generates an interrupt only when the threshold is crossed.

3.7.1 Compare function

The HSADC module optionally compares the result of a conversion with the contents of two value registers for less-than, greater than, inside-range or outside-range detection. The Compare function operates in any of the conversion modes and configurations. After the ADC module samples and converts the input signal, the Compare Function Enable bit in the Command High Buffer register (CMDHa[CMPEN]) guides the automatic Compare operation, which allows the conversion result to be stored only when the Compare condition evaluates as true. Several command-sequencing options associated with the Compare function are available, as summarized in Table 1.

Table 1. ADC Compare function

CMDHa(CMPEN)	Compare function	Description
0b00	Compare disabled	Do not perform a Compare operation. Always store the conversion result to the First-In, First-Out (FIFO).
0b01	Reserved	
0b10	Store on true	Perform a Compare operation. Store the conversion result to the FIFO at the end of averaging *only if* the Compare condition is true. If the Compare result is false, do not store the result to the FIFO. In both true and false cases, the LOOP setting is applied and the LOOP counter increments before determining whether the current command has been completed or if more LOOP iterations are required.
0b11	Repeat Compare until true	Perform a Compare operation. Store the conversion result to the FIFO at the end of averaging *only if* the Compare condition is true. Once the Compare condition becomes true, the LOOP setting is applied and the LOOP counter

Table 1. ADC Compare function*...continued*

CMDHa(CMPEN)	Compare function	Description
		increments before deciding whether the current command has been completed or if more LOOP iterations are required. If the Compare is false, do not store the result to the FIFO. The conversion repeats without considering the LOOP setting, and the LOOP counter does not increment.

Depending on the values programmed in the Compare Value High (CVH) and Compare Value Low (CVL) bit fields in the Compare Value register (CVx[CVH] and CVx[CVL]), the Compare operation checks whether the conversion result is less than, greater than, or if the result falls within or outside the range determined by two Compare values. The use of these Compare values is summarized in Table 2.

Table 2. Compare operations

CVa[CVL] vs. CVa[CVH]	Operation	Description
set CVa[CVL] < CVa[CVH]	Outside range (General form)	Compare is true if the result is less than the CVa[CVL] value or greater than the CVa[CVH] value.
set CVa[CVH] to max value set CVa[CVL] to compare point	Less than	Compare is true if the result is less than the CVa[CVL] value.
set CVa[CVL] to min value set CVa[CVH] to compare point	Greater than	Compare is true if the result is greater than the CVa[CVH] value.
set CVa[CVL] > CVa[CVH]	Inside range	Compare is true if the result is less than the CVa[CVL] value and greater than the CVa[CVH] value.

3.7.2 Enabling ADC interrupts

ADC result data is stored in a FIFO buffer. The LPADC offers two FIFO buffers, where FIFO0 holds up to sixteen entries and FIFO1 holds a single entry. The HSADC offers a single FIFO buffer, which holds up to eight entries.

The Result FIFO Counter bit field in the FIFO Control register (FCTRLa[FCOUNT]) indicates the number of valid data words stored in each RESFIFO. A programmable watermark threshold supports configurable notification of data availability. When FCTRLa[FCOUNT] is greater than the value stored in the Watermark Level Selection bit field (FCTRLa[FWMARK]), the associated *Result FIFO x Ready Flag* is set in the Status Register (STAT[RDY]).

When the FIFO0 Watermark Interrupt Enable bit is set in the Interrupt Enable Register (IE[FWMIEx]), a watermark interrupt request is generated. Reading from RESFIFO provides the oldest unread data word entry in the FIFO and decrements FCTRLa[FCOUNT]. When FCTRLa[FCOUNT] falls equal to or below FCTRLa[FWMARK], the RDY flag is cleared.

3.7.3 Interrupts on low battery

If the voltage reference (VREFH) is reduced, the ADC result output value increases for a fixed channel voltage. In other words, if the channel voltage is fixed, the ADC result output is inversely proportional to the VREFH voltage. If the *greater than* Compare operation is selected in the Compare function, the ADC stores the result only when the result output is greater than a certain value stored in the CVH bit field. With FWMARK set to 0, the ADC generates an interrupt whenever a single result is stored in the FIFO buffer.

If the FIFO watermark is set to 0, the Compare function is enabled, FIFO watermark interrupts are enabled, CVL is 0, CVH is not zero, and the ADC is triggered periodically. Then, the ADC generates an interrupt only when the battery voltage drops below the threshold value (that is, when the channel voltage exceeds the CVH value).

4 Enablement in low-power modes

As MCX L20 includes two available cores, the user can choose the appropriate core based on their use case requirement, specifically, which core they use and which set of peripherals are required to make a functional application.

To support this flexibility, the MCX L20 provides nine different power modes.

- Active (All On)
- Sleep
- Deep-Sleep
- Power-Down 1
- Power Down 2
- Deep-Power Down 1
- Deep-Power Down 2
- Deep-Power Down 3
- Shutdown

Figure 1 illustrates the power states of the CM33 core and the CM0+ core across the different Low-power modes.

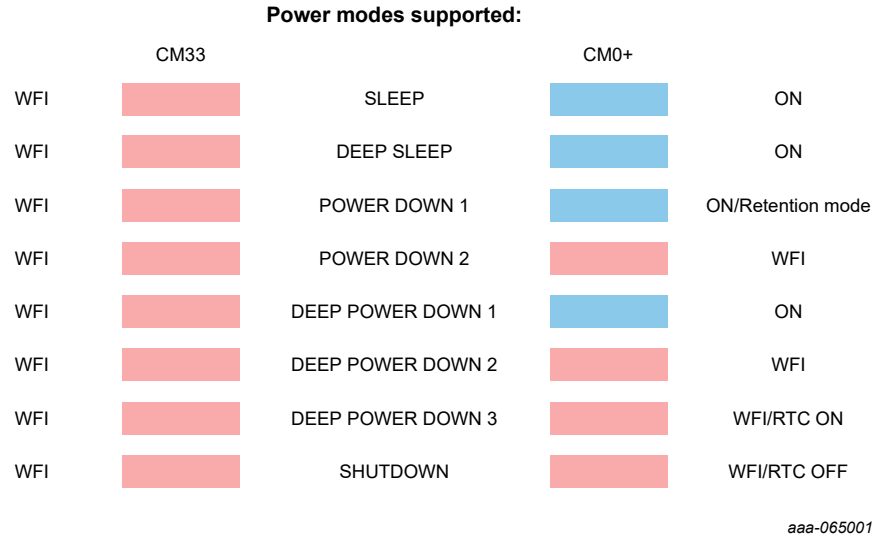

Figure 1. Core states in Low-power modes

The device supports multiple wake-up sources to exit from Low-power modes. These sources are managed through the Sleep Mode Manager (SMM).

For more details on Low-power modes and available wake-up sources, refer to the e *Implementing MCX L25x Low-power Mode* (AN14949).

4.1 Sleep and Deep-Sleep mode

Main domain peripherals only work in Active, Sleep, and Deep-Sleep mode. In Active mode, the CM33 is ‘on’ and can trigger the ADC (either HSADC or LPADC) using software. In Sleep and Deep-Sleep modes, the HSADC must be hardware-triggered by another peripheral. The ADC interrupts can also serve as a wake-up source in low-power modes.

4.1.1 Sleep mode

The CM33 core enters Wait For Interrupt (WFI) state in Sleep mode, but the Main domain peripherals remain operational. A timer, such as CTimer, can trigger the HSADC, which enables battery voltage measurements in Sleep mode as well. The HSADC interrupt can be used to wake up the device when the battery voltage is low (refer to the Section 3.7).

The CM0+ core is ‘on’ in Sleep mode; therefore, the LPADC can be triggered using either software or hardware.

4.1.2 Deep-Sleep mode

The CM33 core enters WFI state in Deep-Sleep mode, and the Main domain peripherals are clock-gated. Clock gating can be disabled for certain peripherals through the Control Automatic Clock Gating x register (GLB_ACCx). A timer, such as a CTimer, can trigger the HSADC, which enables battery-voltage measurements in Deep-Sleep mode as well. The HSADC interrupt can be used to wake up the device when the battery voltage is low (refer to the Section 3.7).

The CM0+ core is ‘on’ in Deep-Sleep mode; therefore, the LPADC can be triggered using either software or hardware.

Note: *Ensure to attach SIRC clock to peripherals and enable SIRC clock in Deep-Sleep mode using SIRCCSR register.*

4.2 Deep-Power-Down 1 (DPD1) mode

In DPD1 mode, the CM33 core and Main domain peripherals are power-gated, and the Main domain peripherals, including HSADC cannot be used.

The CM0+ core is ‘on’ in DPD1 mode; therefore, the LPADC can be triggered using either software or hardware. The LPADC interrupt can serve as a wake-up source. For example, the LPADC interrupt can wake the device when a low-battery condition is detected through the Compare functionality (refer to the Section 3.7).

Note: *Ensure to enable the clock attached for the peripherals using CLK_CONFIG register.*

4.3 DPD2 mode

In DPD2 mode, the CM33 core and Main domain peripherals are power-gated, and the Main domain peripherals, including HSADC cannot be used.

The CM0+ core enters WFI in DPD2 mode; therefore, the LPADC cannot be triggered using software. Instead, peripherals, such as LPTimer, can be used to periodically trigger the LPADC in DPD2 mode. The LPADC interrupt can be used as a wake-up source when the battery voltage is low (refer to the Section 3.7).

Note: *Ensure to enable the clock attached for the peripherals using CLK_CONFIG register.*

5 Acronyms

Table 3 lists the acronyms used in this document along with their description.

Table 3. Acronyms

Term	Description
ADC	Analog-to-Digital Converter
CTimer	Counter/Timer
CVH	Compare Value High

Table 3. Acronyms...*continued*

Term	Description
CVL	Compare Value Low
DPD	Deep Power Down
FIFO	First-In, First-Out
HSADC	High-Speed Analog-to-Digital Converter
LPADC	Low-Power Analog-to-Digital Converter
LPTimer	Low-Power Timer
SMM	Sleep Mode Manager
ULP	Ultra-Low-Power
VREFH	Voltage Reference High
VREFL	Voltage Reference Low
WFI	Wait for Interrupt

6 Related documentation

Table 4 lists the references used to supplement this document.

Table 4. Related documentation/resources

Document	Link/how to access
MCX L25x Reference Manual (MCXLP184M096F50RM)	Contact your local Field Applications Engineer (FAE) or sales representative
Implementing MCX L25x Low-power Mode (AN14949)	Contact your local FAE or sales representative

7 Revision history

Table 5 summarizes the revisions to this document.

Table 5. Revision history

Document ID	Release date	Description
AN14982 v.2.0	25 May 2026	Initial public release
AN14982 v.1.0	15 April 2026	Initial NDA release

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