AN14931

PN5190 LPCD and ULPCD

Rev. 1.0 — 17 June 2026 **Application note**

Document information

Information	Content
Keywords	PN5190, ULPCD, LPCD, low power
Abstract	This document describes how to setup, test and optimize the LPCD and ULPCD on the PN5190.

1 Introduction

This document describes how to setup, test and optimize the Low-Power Card Detection (LPCD) and the Ultra Low-Power Card Detection (ULPCD) on the PN5190. This is valid for both the B1 and B2 version of the PN5190.

It offers guidance on how to optimize the read and detection range in combination with power consumption.

The LPCD can be used in any of the available power configurations (refer to ref.[4] or ref.[5]). The LPCD puts the PN5190 into Standby in the power saving mode, which reduces the overall current consumption to values of approximately 250 µA. The SPI interface is still available during Standby.

The ULPCD requires the internal DCDC to be disabled, therefore, only the power configurations 3, 4, or 5 are available in combination with ULPCD. The ULPCD puts the PN5190 into Ultra Low-Power (ULP) mode, which reduces the overall current consumption to values of approximately 25 µA. The SPI interface is not available during the ULP mode, and only a specific GPIO (besides VEN) can be used by the host MCU to wake up the PN5190.

Note: *The given current consumption number very much depend on settings.*

2 Antenna tuning

The best antenna tuning for the LPCD and ULPCD is the standard "symmetric" antenna tuning, as described in ref.[3]. It makes sense to use the maximum possible antenna impedance to reduce the driver current:

- low impedance = high driver current = high read range
- high impedance = low driver current = low read range

The antenna impedance defines the possible output power and current consumption during the normal card reading operation, but does not at all influence the card detection range and hardly influences the (U)LPCD current consumption. So, the card read range shall be checked with the maximum possible VDDPA to ensure the required read performance in combination with required current consumption in RFON condition.

Note: *Consider the possible VDDPA settings: The **maximum VDDPA** can be the **VUP - 300 mV**, if the TXLDO is used.*

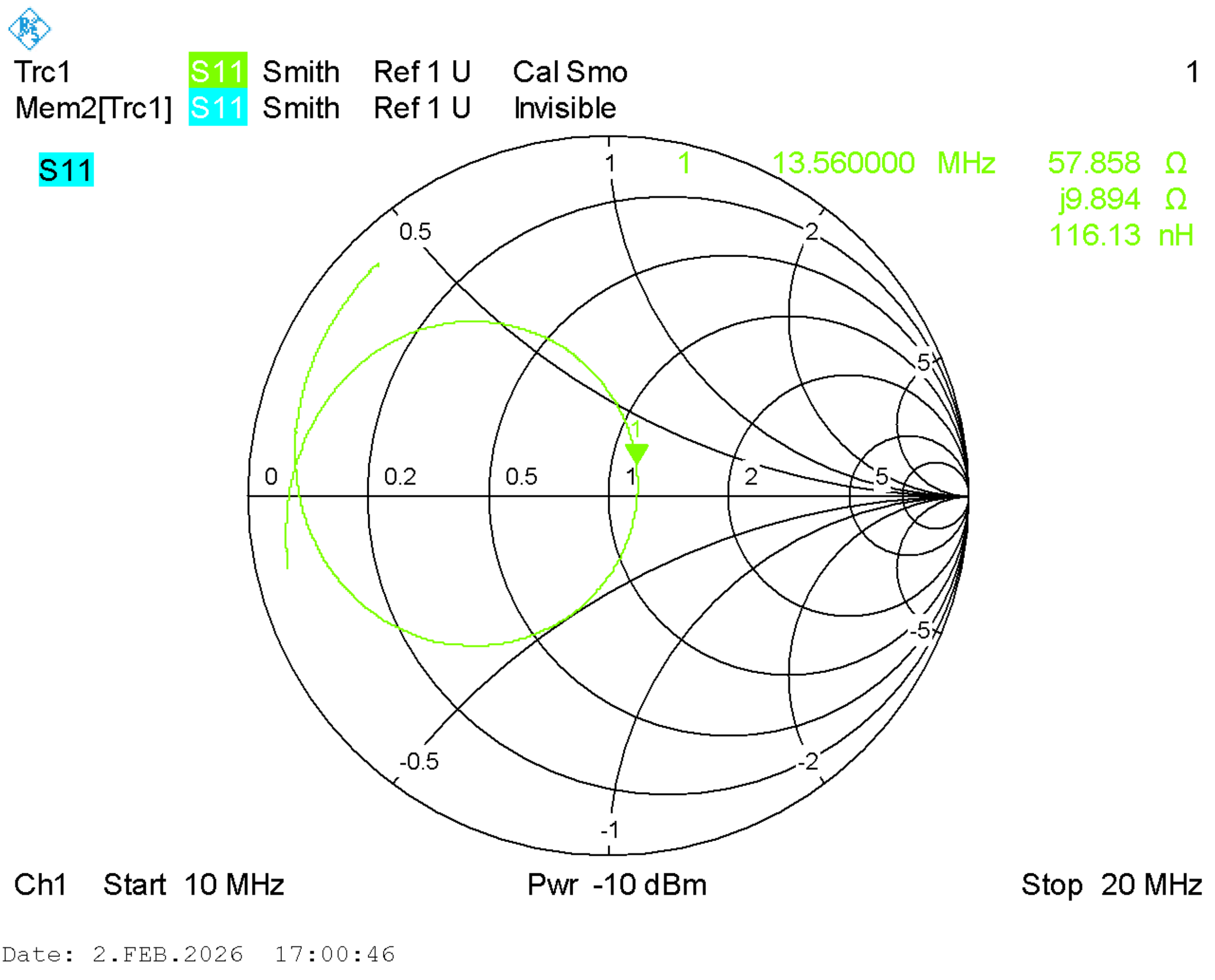


Figure 1. Small low power antenna tuning example

The Figure 1 shows a typical example tuning of a small low power antenna (22mm x 26mm PCB antenna), which is taken to test and optimize the ULPCD performance in the following sections. The antenna q-factor should be as high as possible. The "symmetric" antenna tuning in combination with the PN5190 waveshaping settings typically allows a q-factor of 30 or higher. The higher the q-factor, the lower the current consumption at the same read range. The higher the q-factor, the better the (U)LPCD detection range.

Note: *It makes sense to tune the antenna "symmetrically" with a target impedance with no imaginary component. However, due to tolerances the imaginary part can hardly become zero in reality. Ending up at a negative imaginary component reduces the overall performance, so it is sensible to keep the tuning at some level of positive imaginary impedance (+j) to avoid this negative impact.*

This small example antenna now has the required read range: A MIFARE DESFire card can be operated at 25mm distance, while the unloaded current consumption is low enough. The current = 46mA @ VDDPA = 3.0V. This allows the operation of the device with VBAT = 3.3V with enabled DPC.

Note: *These values only serve as a low power example. Whether or not the read range of 25 mm is good enough depends on the application. With a larger antenna and/or a larger output power, significantly larger read ranges can be achieved.*

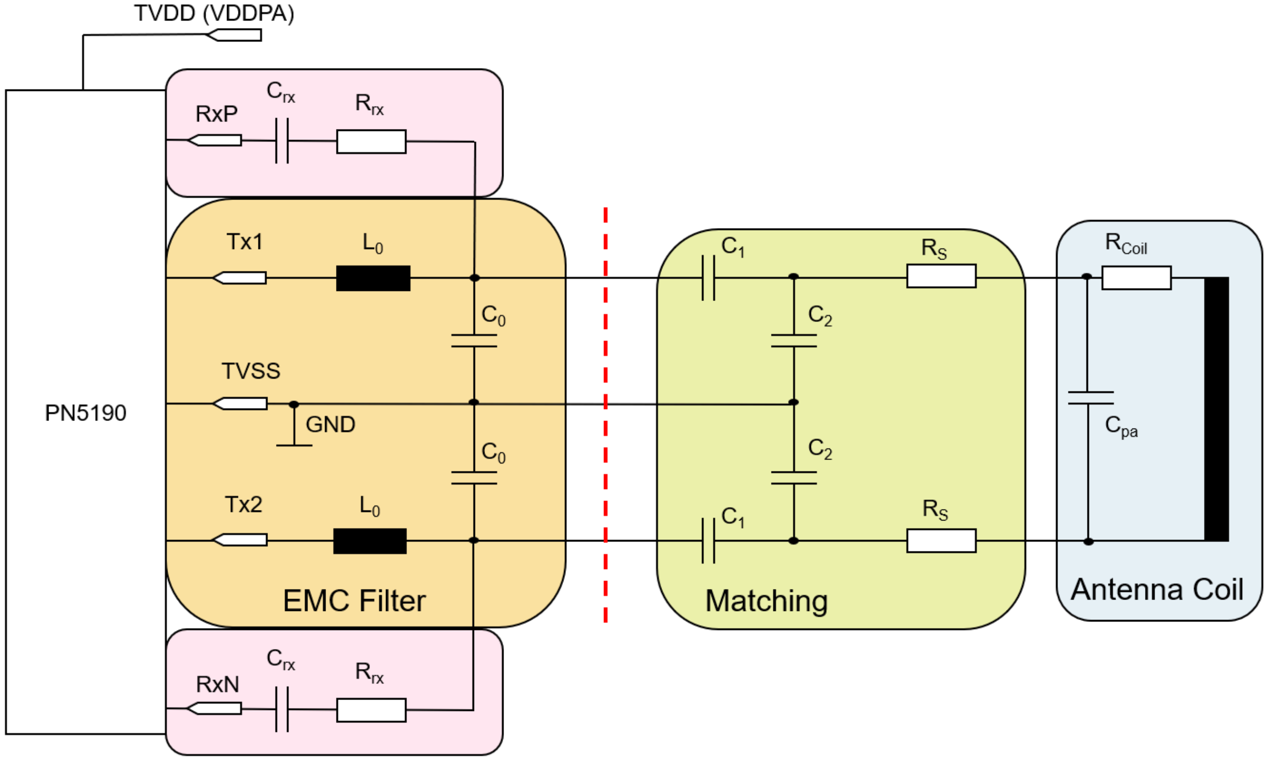


Figure 2. Antenna tuning circuit

3 Receiver adjustment

It is recommend to use the standard antenna design guidance, see ref.[3]. The overall guidance for the optimum RX resistor value is derived from the HFATT value. The HFATT value range starts at 0 and ends at 63dec, and therefore the default setup targets a value of 40dec in the unloaded case of full RF power. This guarantees the operation under all relevant loading and detuning conditions without leaving the HFATT control range.

This applies for the (U)LPCD in principle, too. However, in a typical (U)LPCD reader design, normally the RF power is much lower due to:

1. The (U) LPCD antenna design, which typically has a higher impedance to save power.
2. The maximum VDDPA setting, which in case of ULPCD is limited to VUP - 300mV.

This lower RF power causes a much lower HFATT value. Still, it might not be required to compensate for this lower HFATT value with a lower RX resistor: It makes more sense to keep the RX resistor high to avoid too much damping, as long as the HFATT value "always" stays within its control range. The critical parameter in this low power case typically is the lowest possible VDDPA (typically 1.5V), which then should still cause an HFATT value >0.

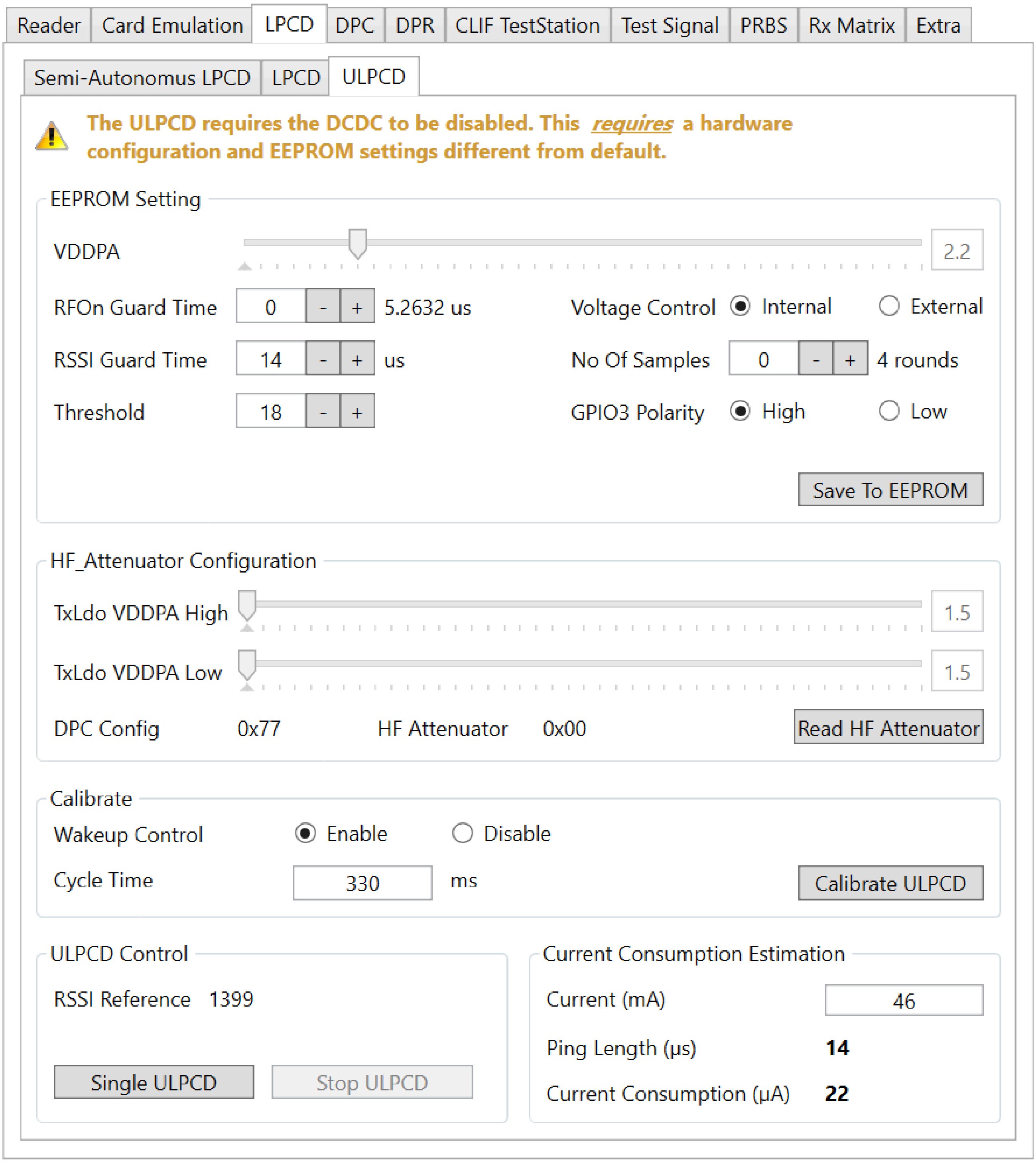
Using the 22mm x 26mm sample antenna with the tuning, as shown in Figure 1, the Figure 3 shows the reading of the HFATT value at VDDPA = 1.5 V, using the NFC Cockpit ULPCD function <Read HF Attentuator>. This function sets the VDDPA to the value, which is adjusted with the two sliders, executes an RFON and reads the HFATT value from the RX_CTRL_STATUS register. It can be observed that the HFATT value is 0, which has the risk that the HFATT control range is exceeded, and therefore the detection range is reduced.

One option would be to reduce the RX resistor value (of R_{rx} as shown in Figure 2), which increases the RX voltage level, which then increases the HFATT value. However, this might damp the antenna tuning circuitry, and therefore lower the q-factor.

The other option is to increase the VDDPA slightly, as shown in Figure 4. With VDDPA = 2.2 V, the HFATT value raises to 4, which guarantees the operation within the control range. This is possible, because the VDDPA does not need to be reduced below 2.2 V during the antenna loading, i.e. even with VDDPA = 2.2V (and RDON feature disabled), the current consumption does not exceed the desired limit, and the RF power does not exceed any critical value. So in summary, with this antenna tuning, the minimum VDDPA can be 2.2 V without any problem.

Note: *Make sure that the VDDPA setting for the ULPCD matches the selection: in case of the second option the VDDPA for the ULPCD must be set to 2.2 V (or higher) to ensure that even during the ULPCD, the HFATT control range is not exceeded. Otherwise, the detection range might be decreased.*

Note: *Make sure that the limiting factor for the read range is the RF power, but not the RX! Otherwise, the reader device would waste power.*



The ULPCD requires the DCDC to be disabled. This *requires* a hardware configuration and EEPROM settings different from default.

EEPROM Setting

VDDPA: 2.2

RFOn Guard Time: 0 5.2632 us

Voltage Control: ● Internal ○ External

RSSI Guard Time: 14 us

No Of Samples: 0 4 rounds

Threshold: 18

GPIO3 Polarity: ● High ○ Low

HF_Attenuator Configuration

TxLdo VDDPA High: 1.5

TxLdo VDDPA Low: 1.5

DPC Config 0x77

HF Attenuator 0x00

Calibrate

Wakeup Control: ● Enable ○ Disable

Cycle Time: 330 ms

ULPCD Control

RSSI Reference 1399

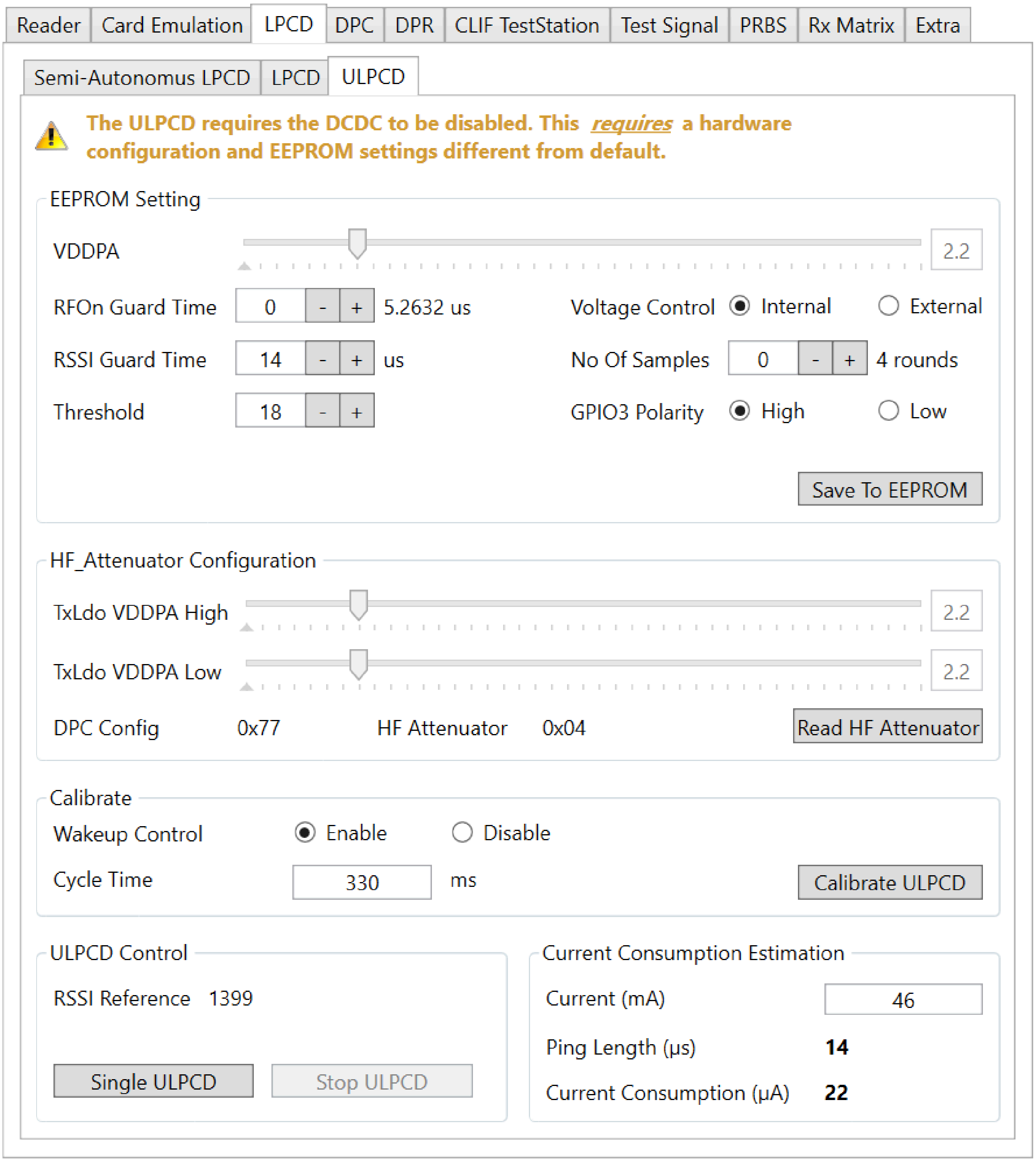
Current Consumption Estimation

Current (mA): 46

Ping Length (µs): **14**

Current Consumption (µA): **22**

Figure 3. HFATT value low power example @ VDDPA = 1.5 V



⚠ **The ULPCD requires the DCDC to be disabled. This *requires* a hardware configuration and EEPROM settings different from default.**

EEPROM Setting

VDDPA 2.2

RFOn Guard Time 0 5.2632 us

RSSI Guard Time 14 us

Threshold 18

Voltage Control ● Internal ○ External

No Of Samples 0 4 rounds

GPIO3 Polarity ● High ○ Low

HF_Attenuator Configuration

TxLdo VDDPA High 2.2

TxLdo VDDPA Low 2.2

DPC Config 0x77

HF Attenuator 0x04

Calibrate

Wakeup Control ● Enable ○ Disable

Cycle Time 330 ms

ULPCD Control

RSSI Reference 1399

Current Consumption Estimation

Current (mA) 46

Ping Length (µs) **14**

Current Consumption (µA) **22**

Figure 4. HFATT value low power example @ VDDPA = 2.2 V

4 TXLDO and TX driver configuration

In principle the driver concept allows two options for the (U)LPCD: either the TXLDO is used or it is disabled.

Note: *Be aware that a clean and stable power supply is essential to achieve the best detection range.*

Note: *Operating the PNEV5190BP for (U)LPCD testing requires an external power supply with a stable 5 V supply, since the typical USB supply from the connected PC can be unstable and increase the jitter.*

4.1 TXLDO enabled

The recommended (and default) setting uses the TXLDO, even in low power applications. This corresponds to the power configuration 1 and 2 for LPCD, and 3 or 4 for (U)LPCD. The usage of the TXLDO reduces the maximum VDDPA:

VDDPAmax = VUP - 300 mV

This costs a bit of read range or requires a slightly lower impedance to compensate for the lower VDDPA, but it keeps the DPC enabled:

- The ULPCD can use VDDPA = 1.5 V (or any other level up to the VDDPA max).
- The DPC can easily help to avoid "overcurrent", i.e. the DPC settings define the maximum current (= target current + hysteresis), even under loading conditions.
- The DPC allows to reduce the RF power in close distance to save power or to limit the RF field strength.
- All DPC-related features are available: AWC, ARC, etc.

4.2 TXLDO disabled

Disabling the TXLDO requires to supply the VDDPA externally. This corresponds to the power configuration 5, therefore VDDPAmin = VDDPAmax = VUP = VBAT.

- This provides 300 mV more to the TX driver, which increases the possible read range with higher impedance (lower current).
- The ULPCD uses the same VDDPA, i.e. always runs with the maximum VDDPA. This might cause a higher current consumption during the ULPCD as well as a higher noise level, i.e. reduced (U)LPCD sensitivity.
- TXLDO needs to be disabled (via EEPROM setting)!
- No DPC function is available, i.e. no overcurrent protection, no RF power control, and no DPC-related functions like AWC or ARC are available.

5 Crystal settings

The startup time of the crystal plays a major role during the normal startup of the PN5190, but also during the (U)LPCD ping startup. The faster the crystal, the lower the current consumption. The ref.[1] provides instructions for optimization.

It is not allowed to use an external clock input in combination with the LPCD or ULPCD, but only a crystal.

The FW 02.0E or higher (for the B1) or FW 03.08 or higher (for the B2) offer the related test signals to optimize the crystal startup behavior and timing, which can be used to optimize the current consumption in case of ULPCD.

6 LPCD settings

The LPCD offers several options. The semi-autonomous LPCD mode allows to check the LPCD performance without going into standby. It simply allows to calibrate the LPCD and then read the I and Q channel signals for reference without using the LPCD_SWITCH_MODE command.

The LPCD_SWITCH_MODE command offers:

- a calibration without going into standby (bControl = 0x02)
- a calibration including standby (bControl = 0x0C)
- the LPCD execution without calibration (bControl = 0x03)
- the LPCD execution including calibration (bCotnrol = 0x04)
- the LPCD execution in HCE (bControl = 0x13)

The recommendation is to use the LPCD execution including the calibration (bControl = 0x4): this command option executes the calibration and then automatically enters LPCD in one step. The calibration is completed including entering standby.

Executing the calibration without standby might give a slightly different result compared to executing the calibration including standby, since the overall signal levels might be slightly different. Including the standby into the calibration increase the accuracy.

6.1 Semi-autonomous LPCD mode

The LPCD semi-autonomous mode does not the LPCD_SWITCH_MODE command, but is only based on reading and writing registers. The PN5190 does not enter Standby mode. Before starting the LPCD calibration in the semi-autonomous mode, the RSSI target and the RSSI hysteresis need to be written into the LPCD_CONTROL register, as shown in Figure 5. This is done automatically, if the <Calibrate LPCD> in the Semi-autonomous mode tab of the NFC Cockpit is used (see Figure 6).

LPCD_CALIBRATE_CTRL

Register address: 0x50

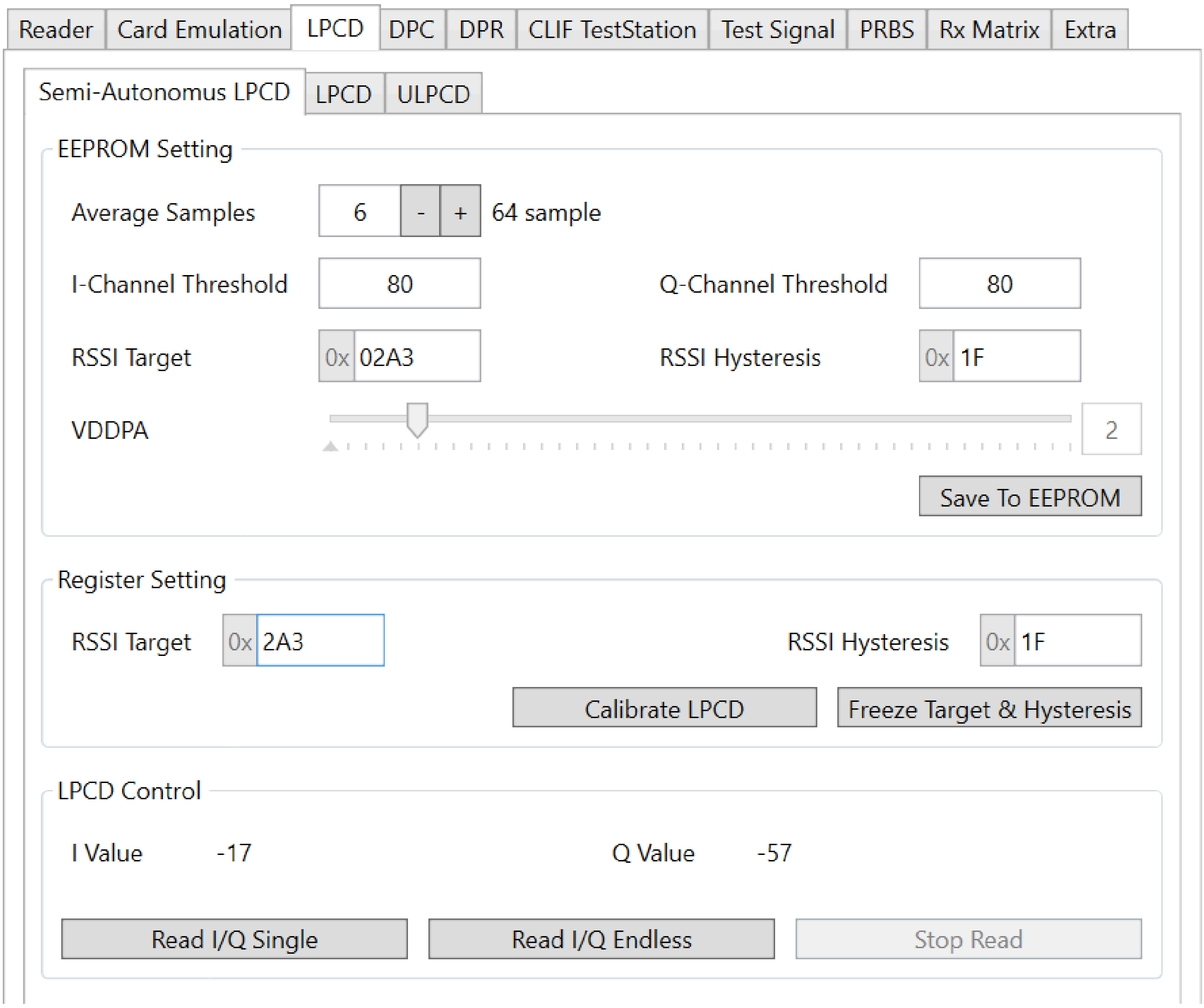
○ EEPROM
● Register

801F02A3

Write Operation
● All bits
○ Single bit

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit selection	☑	☑	☑	☑	☑	☑	☑	☑	☑	☑	☑	☑	☑	☑	☑	☑	☑	☑	☑	☑	☑	☑	☑	☑	☑	☑	☑	☑	☑	☑	☑	☑
Binary	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	1	0	1	0	1	0	0	0	1	1
Field	RESERVED	FREEZE_VALUE...	RESERVED						RSSI_HYSTERE...								RSSI_TARGET															

Figure 5. LPCD_CALIBRATE_CTRL register



Average Samples: 6 — 64 sample
I-Channel Threshold: 80
Q-Channel Threshold: 80
RSSI Target: 0x 02A3
RSSI Hysteresis: 0x 1F
VDDPA: 2

RSSI Target: 0x 2A3
RSSI Hysteresis: 0x 1F

I Value: -17
Q Value: -57

Figure 6. Semi-autonomous LPCD

After calibration, the I and Q values can be read from the IQ_CHANNEL_VALS register. The continuous reading indicates the jitter. Placing a card or phone shows the detuning and loading effect.

6.2 Regular LPCD mode

The regular LPCD measures the detuning or loading of the antenna via I and Q channel signals. The antenna detuning is independent from the RF power level, so it makes sense to reduce the RF power level as much as possible for two reasons:

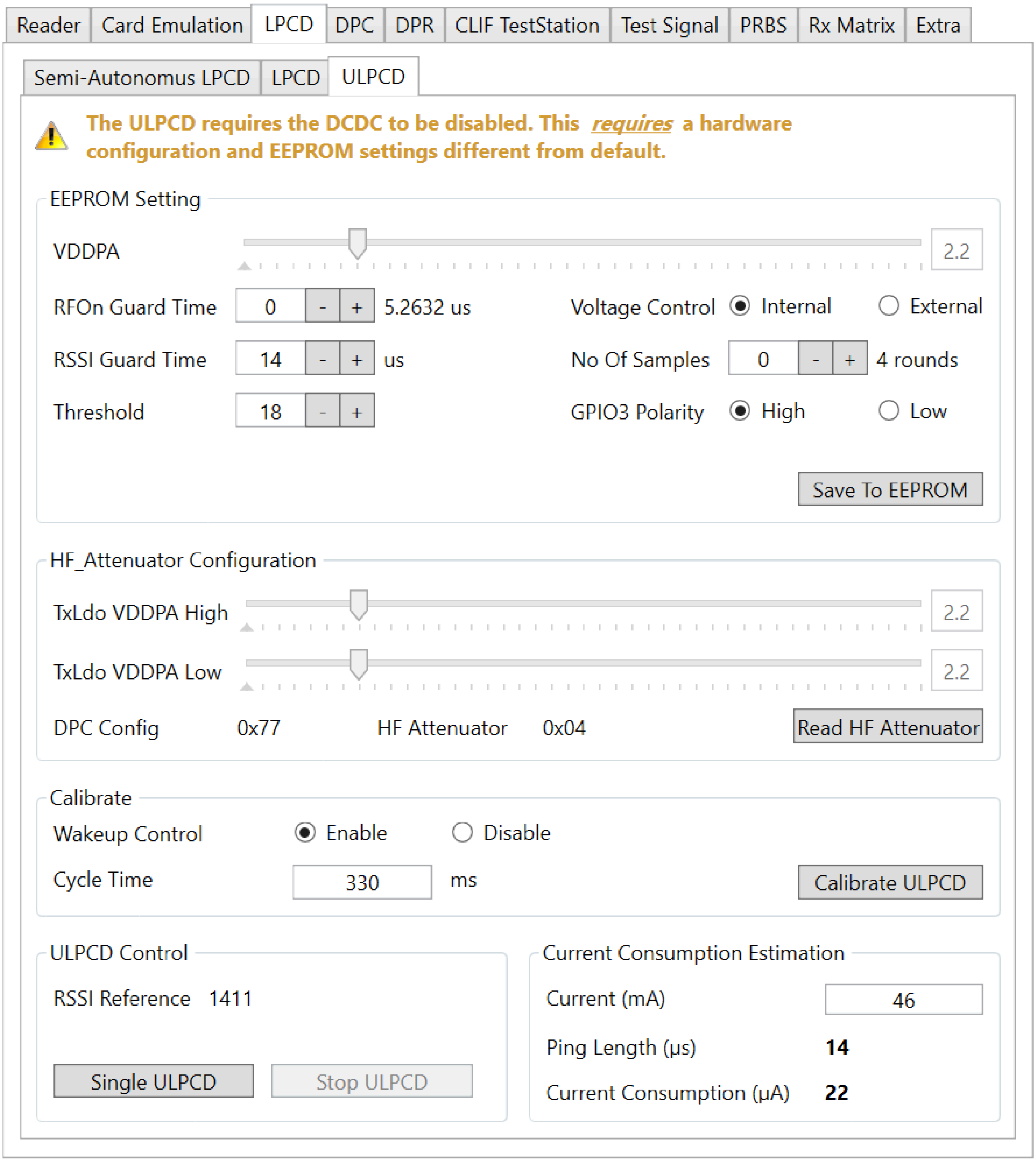
1. to save power (current consumption)
2. to avoid overcurrent under loading condition

The LPCD does not use the DPC, so the RF pulse uses the VDDPA setting, which is defined in LPCD_VDDPA (0x4AF). Be aware that a strong loading might cause a very low antenna impedance and thus a very high TX driver current, if the LPCD_VDDPA is set too high.

The only relevant LPCD setting besides the cycle time is the LPCD_THRESHOLD: a value slightly beyond the jitter gives the best sensitivity, i.e. the best detection range.

7 ULPCD settings

It is recommended to optimize the ULPCD parameters with the NFC Cockpit (refer to ref.[6]). The NFC Cockpit allows to easily modify the ULPCD relevant settings, execute measurements, the ULPCD calibration, and ULPCD execution. The Figure 7 shows a typical start condition for a test.



The ULPCD requires the DCDC to be disabled. This *requires* a hardware configuration and EEPROM settings different from default.

EEPROM Setting

VDDPA 2.2

RFOn Guard Time 0 5.2632 us

Voltage Control ● Internal ○ External

RSSI Guard Time 14 us

No Of Samples 0 4 rounds

Threshold 18

GPIO3 Polarity ● High ○ Low

HF_Attenuator Configuration

TxLdo VDDPA High 2.2

TxLdo VDDPA Low 2.2

DPC Config 0x77

HF Attenuator 0x04

Calibrate

Wakeup Control ● Enable ○ Disable

Cycle Time 330 ms

ULPCD Control

RSSI Reference 1411

Current Consumption Estimation

Current (mA)	46
Ping Length (µs)	**14**
Current Consumption (µA)	**22**

Figure 7. NFC Cockpit ULPCD tab

The overall target of the optimization shall be to reduce the average current consumption as much as possible, while achieving the best detection range without false wake-up. The ULPCD wakes up due to antenna loading and detuning, beyond a certain threshold window. The smaller the threshold window, the more sensitive the ULPCD gets. The wider the threshold window, the more robust the ULPCD gets. It is important to keep the jitter small, which then allows a small threshold window, i.e. a large detection range without false wake-up.

7.1 Prerequisites

The ULPCD operation requires to disable the DCDC and maybe the DPC, i.e. to use the configuration example 3, 4 or 5 (as listed in ref.[4] or ref.[5]). The required EEPROM configuration is listed there, too.

7.1.1 Disable DCDC

For the ULPCD it is required to disable the DCDC. The most typical configuration is the configuration 3. For the hardware design that means, the DCDC inductor shall be removed and VBATPWR, BOOSTLX, VDDBOOST, and VUP shall be connected to VBAT. This hardware configuration needs to be reflected in the EEPROM settings:

DCDC_ PWR_ CONFIG (address 0000h) must be set to 0x21.

The DPC configuration as such does not have to be changed, and it is recommended to keep the DPC enabled (power configuration 3 or 4). Only the VDDPA setting for the normal reader operation needs to be adjusted.

Note: *The required modifications (jumper settings and EEPROM settings) for the PNEV5190BP are listed in ref.[2].*

7.1.2 VDDPA setting

As stated above, the DPC does not need to be disabled. Disabling the DPC does not give any benefit, if the TXLDO is used (configuration 3 or 4), but keeping the DPC enabled provides additional features, even if the DPC is not required from an RF point of view: At minimum the DPC provides an adjustable current limiter.

The PN5190 default EEPROM configuration provides the maximum output power with enabled DCDC, so the maximum VDDPA is set to 5.7 V. This needs to be limited to VUP - 300mV.

Example: Supply voltage level = 3.3 V, so VDDPA max = 3.0 V:

TXLDO_VDDPA_MAX_RDR (0008h) = 0x0F

Note: *The VDDPA setting for the ULPCD itself is independent from the TXLDO_VDDPA_MAX_RDR setting, since the VDDPA for the ULPCD ping is defined in ULPCD_VDDPA_CTRL (04BFh).*

7.2 HFATT value

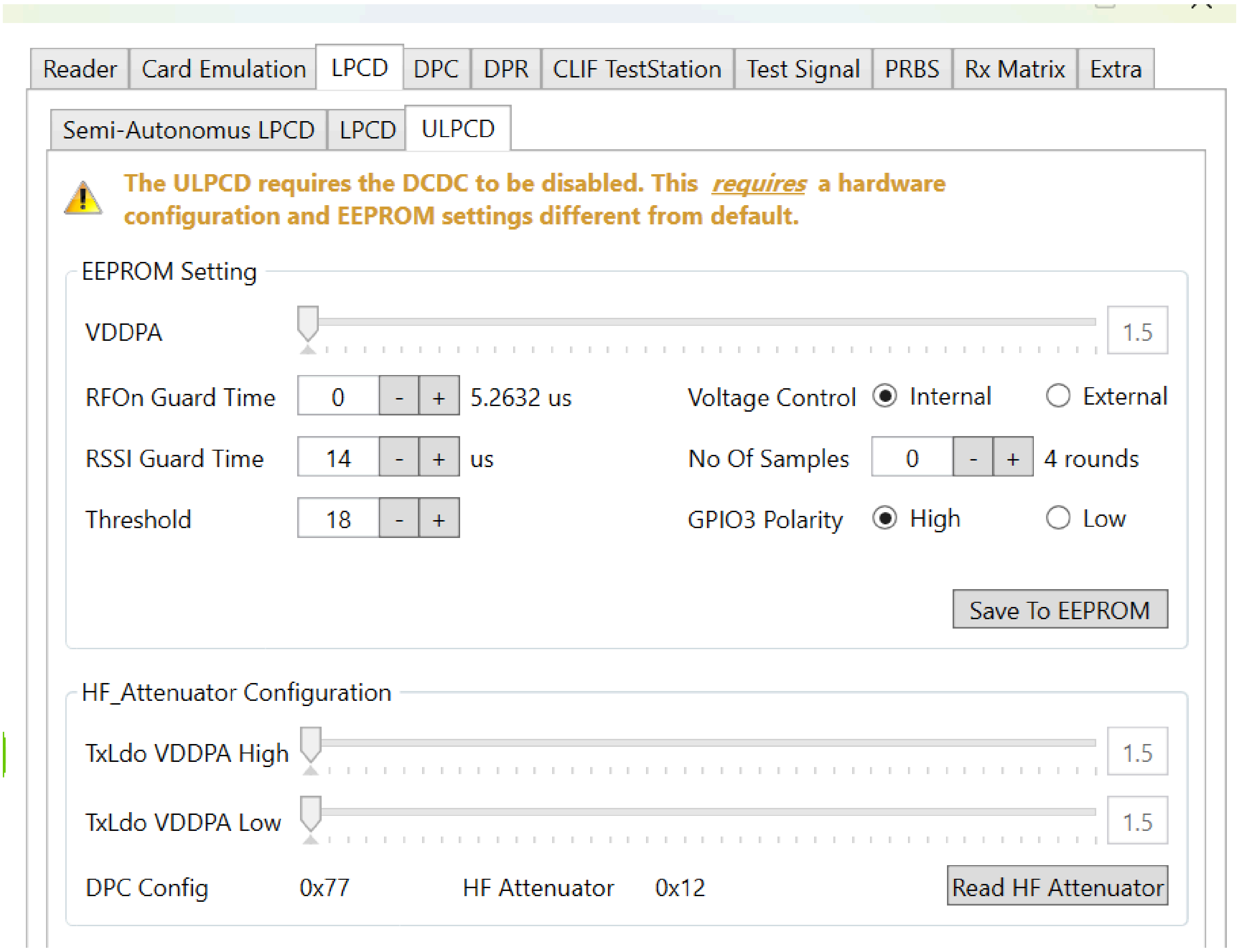
As stated in previous sections, it is a key requirement for the ULPCD to operate the PN5190 RX within the HF attenuator control range. During the normal NFC operation, the RX uses the HF attenuator to provide an optimum input level: The PN5190 automatic gain control (AGC) uses a control loop, which controls the RX input level. This is done fully automatically, but requires a proper RX connection. The value of the RX resistor is a key parameter, which needs to be adjusted once for a certain antenna tuning, as stated in ref.[3].

The HFATT value can be read from the RX_CTRL_STATUS register (0028h), bit 3...8. This value indicates the level of attenuation, which shall not exceed the given range from 0 to 63dec. So, with the smallest signal at the RX, the HFATT value shall not reach 0, and with the largest signal at the RX, the HFATT value shall not reach 63.

For the ULPCD, the RX is used in a different way, which requires the HFATT value to be set by the host (as command parameter of the SWITCH_MODE_LPCD command). It is required to use a value of HFATT, which fits to the RX settings and the RF level in such way that the resulting RSSI value is in the "sensitive range". The best and recommended way to derive the correct HFATT value is to enable the RF in the normal PCD operation ("reader mode"), using the same power level as during the ULPCD, and then read the RX_CTRL_STATUS register.

The read value then shall be used as an input parameter for the ULPCD calibration and execution. The Figure 8 shows the HFATT value on the PNEV5190BP with the default antenna, using the setting of ULPCD VDDPA = 1.5V.

Also in case of ULPCD (i.e. with, e.g., in this case VDDPA = 1.5 V), the HFATT shall not be 0 or 63. If the HFATT value is 0, either the RX resistor value can be reduced or the VDDPA can be increased.



The ULPCD requires the DCDC to be disabled. This *requires* a hardware configuration and EEPROM settings different from default.

VDDPA 1.5

RFOn Guard Time 0 5.2632 us

Voltage Control ● Internal ○ External

RSSI Guard Time 14 us

No Of Samples 0 4 rounds

Threshold 18

GPIO3 Polarity ● High ○ Low

TxLdo VDDPA High 1.5

TxLdo VDDPA Low 1.5

DPC Config 0x77

HF Attenuator 0x12

Figure 8. PNEV5190BP default HFATT at VDDPA = 1.5V

Note: *The NFC Cockpit requires <Read HF Attenuator> before the ULPCD can be tested. The shown HFATT value is then automatically taken as the required command parameter, when executing the ULPCD calibration or single ULPCD.*

In the normal ULPCD application, the HFATT value can be read **once** under defined loading condition (for example, unloaded), and then is stored in the host MCU. Alternatively, it can be read regularly to maybe improve the ULPCD performance under changing loading conditions, but then it should be done carefully:

1. Make sure that the loading conditions and the used VDDPA setting do not cause any overcurrent.
2. Use the DPC_CONFIG register (005Eh) to temporarily disable the DPC before RFON.
3. Set the required VDDPA temporarily (if different than 1.5V) with the TXLDO_VDDPA_CONFIG register (00054h).
4. Execute a <Load Protocol> (for example, for A106), followed by an <Rf Field on>.
5. Read the RX_CTRL_STATUS register.

Note: *Writing the EEPROM settings regularly (within the application) is not recommended at all, since it can reduce the life time of the memory. So, disabling the DPC and setting the required VDDPA can be done via registers (RAM only) without modifying the EEPROM settings.*

7.3 Jitter measurement

When the ULPCD VDDPA and HFATT value settings are correctly set, a ULPCD calibration can be executed. The ULPCD calibration executes a regular ULPCD cycle including the RF ping, at which the RSSI value is measured. Instead of using this RSSI value to determine whether or not a card has been detected during the calibration, the RSSI value is simply returned to the host as part of the ULPCD response (LPCD_CALIBRATION_DONE Status data). This value then is required to be used as a command parameter together with the HFATT value, when starting the ULPCD execution.

Instead of starting the ULPCD execution, for testing purposes it makes sense to execute the ULPCD calibration several times, and every time read the RSSI value. Reading this value many times under the same loading conditions (for example, unloaded) should return the same RSSI value in principle. However, due to tolerances and noise, the RSSI value typically jitters.

The Figure 9 shows the result of such jitter measurements for different RSSI Guard Time values. All the measurements have been done with no loading, Number of Samples = 0 and VDDPA = 2.2 V, using the 22 mm x 26 mm antenna.

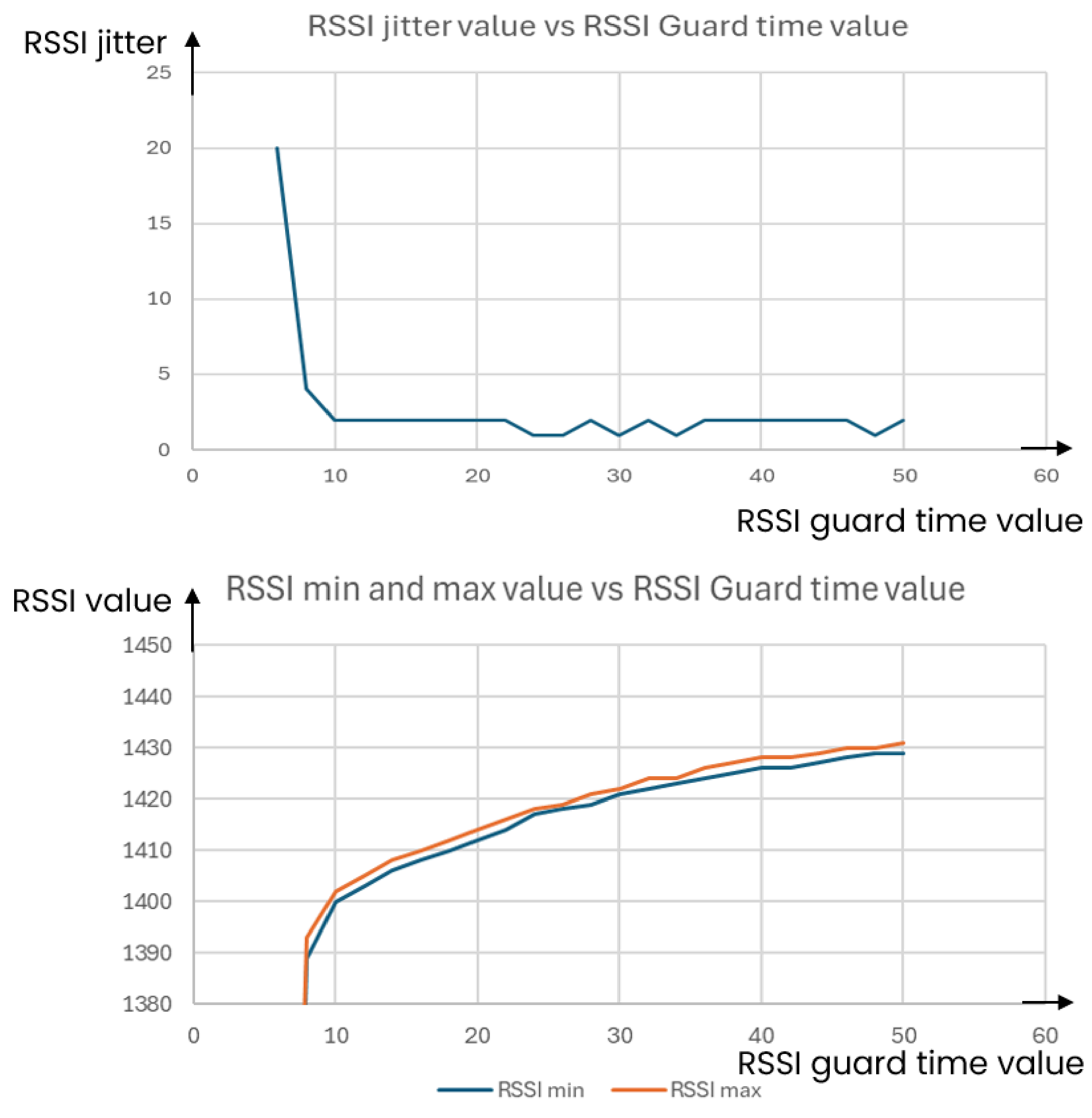


Figure 9. RSSI value and jitter vs RSSI guard time

It can be seen that the jitter with a very low RSSI Guard time (<10) is extremely high. The corresponding RSSI value itself is extremely small, too. As soon as the RSSI Guard time >12, the jitter is reduced to 2 (= ±1). Increasing the RSSI Guard time further does not give any benefit in this setup, but only increases the ping length (and thus the current consumption), as can be seen in Figure 10. The RSSI value in a typical scenario is in the range between 1400 and 1500.

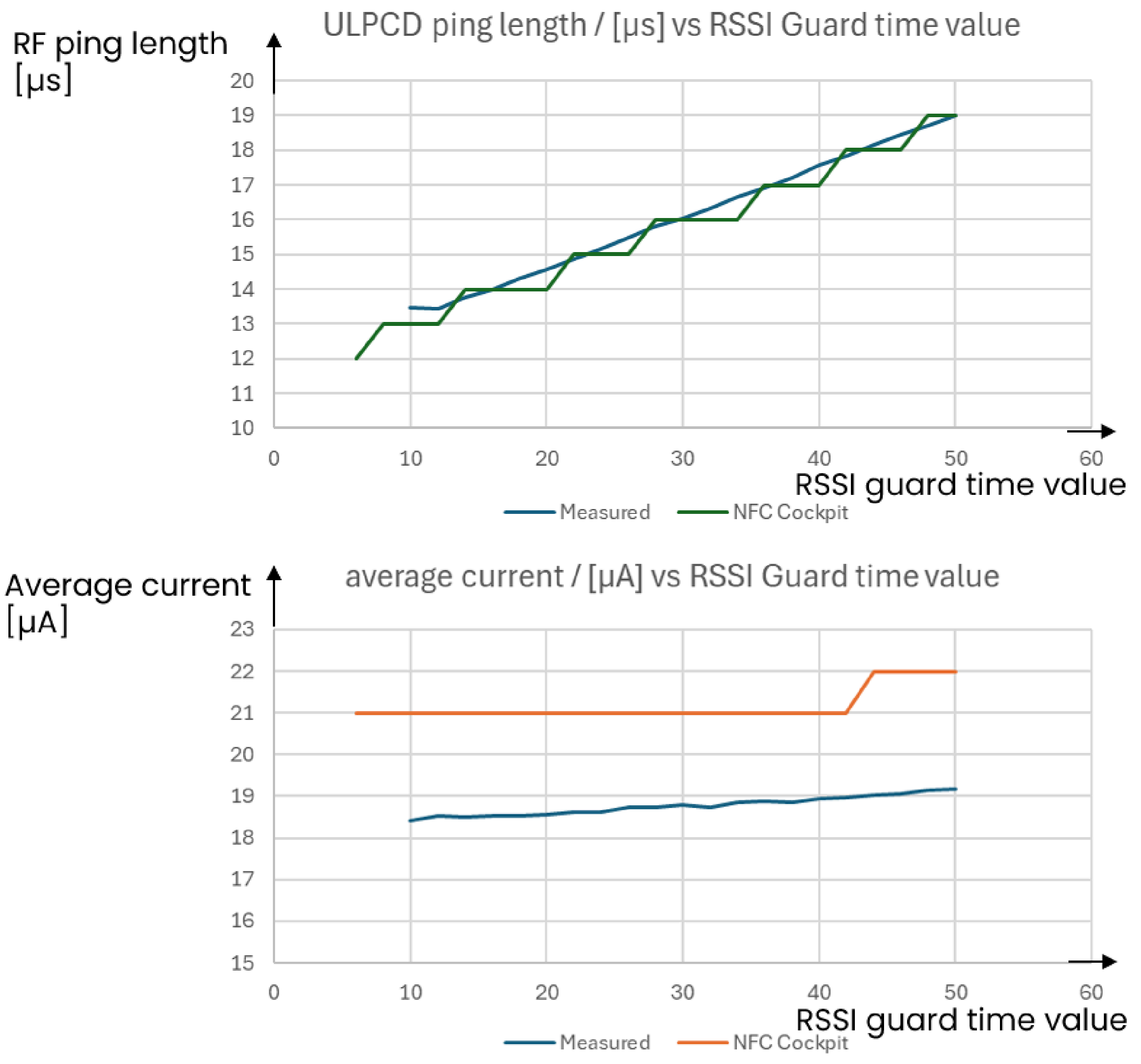


Figure 10. RF ping length and current consumption

Note: *Due to the very short RF pulse and the limited bandwidth and limited sample rate of the current measurement tool, the measured average current might be indicated 1 µA or 2 µA less than in reality. This makes the NFC Cockpit estimation result quite accurate.*

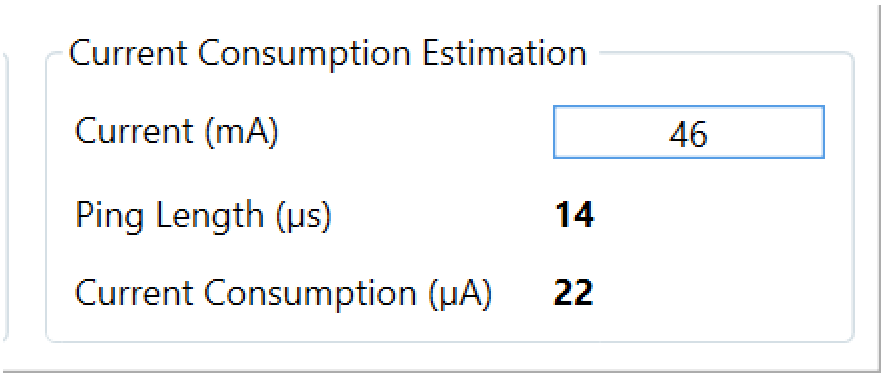
7.4 Threshold and timing

The jitter measurement clearly shows that the RSSI Guard time shall be >10, so with some small margin a value of 12 obviously is good. Increasing the number of samples quickly extends the RF ping length, but does not give any benefit in our test. The RF ping length should be as short as possible to save current. The RFON guard time has no further influence on the jitter, so we can start with a value of 0, which corresponds to ≈ 5..6 µs. The measurement as well as the NFC Cockpit indicate an overall RF ping length of ≈ 14 µs.

Decreasing the RF ping length has a negative impact on the jitter, increasing the RF ping length does not improve the behavior. So, the overall ping length of 14µs in this example obviously is the optimum.

The cycle time has a direct influence on the average current consumption, which is obvious. The NFC Cockpit allows a quick check and estimates the average current consumption based on the timing settings, as long as a reasonable value for the TX driver current is entered by the user (refer to Figure 11). The current value, which needs to be entered by the user, can be derived from the TXLDO_VOUT_CURR register (0056h), if the RF is enabled with the correct VDDPA. Here the same setup as for the HFATT value reading can be used to read this value:

1. Make sure that the loading conditions and the used VDDPA setting do not cause any overcurrent.
2. Use the DPC_CONFIG register (005Eh) to temporarily disable the DPC before RFON.
3. Set the required VDDPA temporarily (if different than 1.5V) with the TXLDO_VDDPA_CONFIG register (00054h).
4. Execute a <Load Protocol> (for example, for A106), followed by an <Rf Field on>.
5. Read the TXLDO_VOUT_CURR register.


Current Consumption Estimation

Current (mA) 46

Ping Length (µs) **14**

Current Consumption (µA) **22**

Figure 11. NFC Cockpit ULPCD average current consumption estimation

So, with a chosen cycle time of 330ms (i.e. the ULPCD ping will check the antenna loading 3 times a second) the average current consumption ends up at ≈22 µA. If 2 ULPCD pings per second are enough, the average current decreases to ≈16 µA, if the use case requires 5 ULPCD pings per second, the average current increases to ≈33 µA.

With these values we can start to test the PN5190 ULPCD itself. The jitter in our test is ± 1, so a threshold window of 2 should be good enough to operate the ULPCD without false wake-up within a reasonable amount of time. In fact, the test shows that with a threshold of 2 (which means ±2), the ULPCD runs several hours without waking up, if no environmental change happens. With a threshold of 1, the ULPCD runs several minutes before waking up. So, starting with a threshold of 2 and then increasing step by step, we can test the ULPCD detection range with both a smartphone and a typical smart card. The result is shown in Figure 12.

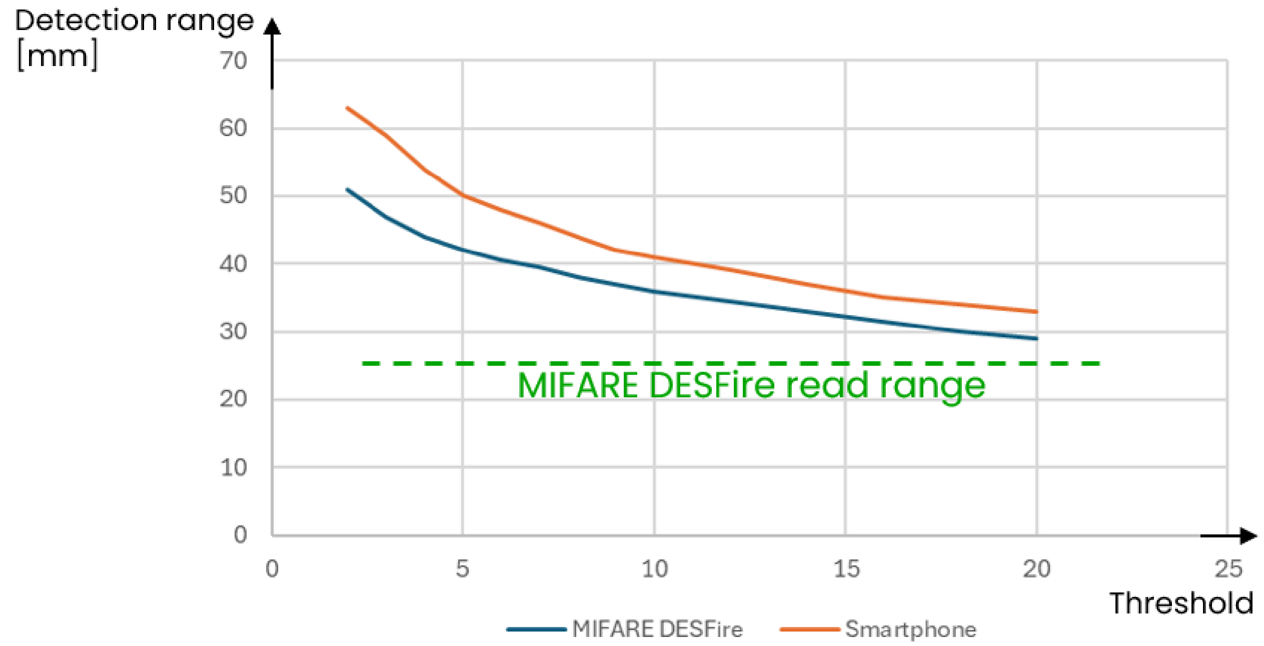


Figure 12. ULPCD range vs threshold

Considering the clean lab environment versus some more noisy environments in the field, a threshold of 2 might not be the best option for a real application. However, even with a threshold of 3 or 4, the ULPCD detection range is almost twice the chosen read range in this example. With a larger antenna and / or higher driver current (i.e. lower antenna impedance), the read range might be larger compared to the detection range: the read range can be influenced with the driver current, but the detection range is independent from the RF power.

Note: *Be aware that a higher ULPCD VDDPA level or a higher ULPCD RF output power increases the noise level and may even reduce the sensitivity and thus the ULPCD detection range.*

8 Abbreviations and acronyms

Table 1. Abbreviations

Acronym	Description
AGC	Automatic Gain Control
HFATT	HF attenuator
LPCD	Low Power Card Detection
RX	Receiver
TX	Transmitter
TXLDO	Transmitter low drop out regulator, which supplies the TX with VDDPA
ULPCD	Ultra Low Power Card Detection
VBAT	Supply voltage
VDDPA	Supply voltage of the TX driver
VUP	Supply voltage of the TXLDO

9 References

[1] Application Note – AN14518 – Crystal Oscillator Design Guide (link)
[2] Application Note – AN12551 – PN5190 design-in recommendations (link)
[3] Application Note – AN12549 – PN5190 antenna design guide (link)
[4] Data Sheet – PN5190B2 – PN5190B2 NFC Frontend (link)
[5] Data Sheet – PN5190B1 – PN5190B1 NFC Frontend (link)
[6] Configuration Tool NFC Cockpit (link)

10 Revision history

Table 2. Revision history

Document ID	Release date	Description
AN14931 v.1.0	17 June 2026	• Initial version

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