AN14917

Migration Guide from LPC5534/36/S36 to MCX A34/36 Devices

Rev. 1.0 — 5 March 2026

Application note

Document information

Information	Content
Keywords	AN14917, MCX A, MCX A34, MCX A36, LPC5534, LPC5536, LPC55S36, migration guide
Abstract	This application note introduces the MCX A3 series microcontroller, and provides migration guide from LPC5534/36/S36 to MCX A34/36 devices.

1 Introduction

This document provides an overview of the key differences between the LPC5534/36/S36 to MCX A34/36 MCUs. It also serves as a guide for migrating designs from LPC5534/36/S36 to the MCX A34/36 devices. The migration between these MCUs requires software and hardware updates. This document describes the changes require to migrate from LPC553x/S3x to MCX A34 MCUs.

This document is released along with the relevant device-specific hardware documentation such as data sheets, reference manuals, and application notes available on the following pages: MCX-A34, MCX-A36, and LPC553x

2 Comparison between LPC5534/36/S36 to MCX A34/36 MCUs

The subsections that follow compare the main features between the LPC5534/36/S36 to MCX A34/36 MCUs.

2.1 MCX A34/36 family overview

The MCX A34/36 is a family of Arm Cortex-M33-based microcontrollers designed for a wide range of embedded applications. These devices include Security Generation Index (SGI) and Public Key Cryptography (PKC) security features and offer up to 1024 kB of on-chip flash and up to 246 kB of on-chip Static Random-Access Memory (SRAM).

They include a rich set of connectivity and control peripherals, such as:

- USB full-speed device with crystal-less operation
- USB full-speed host
- Controller Area Network Flexible Data-Rate (CAN FD)
- Five general-purpose timers
- One 24-bit Multi-Rate Timer (MRT)
- One Windowed Watchdog Timer (WWDT)
- Two code watchdog timers
- One Operating System (OS) timer
- One Microtick timer
- Up to six Low-Power Universal Asynchronous Receiver-Transmitter (LPUART)
- Up to four Inter-Integrated Circuits (I2C)
- Up to two Serial Peripheral Interfaces (SPI)
- Up to one Improved Inter-Integrated Circuit (I3C) interface
- Four Analog-to-Digital Converters (ADCs) supporting:
  - 12-bit resolution at 4.0 Msps
  - 16-bit resolution at 3.2 Msps
  - Simultaneous conversion across four channels
- One 12-bit, 1 Msps Digital-to-Analog Converter (DAC)
- High-speed comparators
- Integrated Operational Amplifiers (OPAMPs)
- Two FlexPWM timers
- Two Quadrature Decoder Controllers (QDCs)

The MCX A34/36 devices are optimized for low-power operation, featuring:

- < 75 µA/MHz active current
- < 10 µA Power-down mode with Real-Time Clock (RTC) enabled and 8 kB SRAM retention
- < 2.5 µA deep Power-down mode with RTC active and 8 kB SRAM retention

2.2 LPC553x/S3x family overview

The LPC5534/36/S36 is a family of Arm Cortex-M33–based microcontrollers designed for embedded applications. These devices include the EdgeLock Secure Enclave (ELS) and PKC module, and provide up to 256 kB of on-chip flash and up to 128 kB of on-chip SRAM.

They integrate a comprehensive set of peripherals, including:

- FlexSPI with cache and dynamic decryption
- PRINCE modules for on-the-fly flash encryption/decryption
- USB full-speed device with crystal-less operation
- USB full-speed host
- CAN FD
- Five general-purpose timers
- One Serial Communication Interface Timer/Pulse-Width Modulator (SCTimer/PWM)
- One RTC/alarm timer
- One 24-bit MRT
- One WWDT
- Code watchdog timer
- One OS timer
- One Microtick timer
- Eight Flexcomm serial interfaces configurable as Universal Synchronous/Asynchronous Receiver/Transmitter (USART), SPI, high-speed SPI, I2C, or I3S
- One Digital Microphone (DMIC) interface
- One I3C interface
- Four ADCs supporting:
  - 16-bit resolution at 2.0 Msamples/s
  - 12-bit resolution at 3.2 Msamples/s
  - Simultaneous conversions across four channels
- Four comparators
- Two temperature sensors
- Three 12-bit, 1 Msps DACs
- Three OpAmps
- Two FlexPWM timers
- Two Quadrature Encoder Interfaces (QEIs)

The Arm Cortex-M33 core provides a robust security foundation offering isolation to protect valuable IP and data with TrustZone technology. It simplifies the design and software development of digital signal control systems with the integrated Digital Signal Processing (DSP) applications.

For enhanced security, the LPC5534/36/S36 devices support:

- Secure boot
- HASH
- Advanced Encryption Standard (AES)
- Elliptic Curve Cryptography (ECC)
- Rivest–Shamir–Adleman (RSA)
- Unique Universal Identifier (UUID)
- Device Identifier Composition Engine (DICE)
- Dynamic encryption/decryption
- Debug authentication

- Compliance with TBSA security guidelines

The LPC5534/36/S36 devices are optimized for power-efficient operation:

- ≤ 66 µA/MHz active current
- ≤ 8 µA Power-down mode with 8 kB SRAM retention
- ≤ 2.4 µA deep Power-down mode with RTC active and 4 kB SRAM retention

2.3 High-level comparison

Table 1 provides a high-level comparison of key features, peripherals, memory architecture, security capabilities, and system functions across the LPC5534/36/S36, MCX A343/344, and MCX A365/366 devices to support hardware and software migration analysis.

Table 1. MCX A343/344, MCX A365/366, and LPC5534/36/S36 high-level comparison

Features		LPC5534/36/S36	MCX A343/344	MCX A365/366
CPU core platform	Cortex-M33	Single core 150 MHz	Single core 180 MHz	Single core 240 MHz
	TrustZone	Yes	-	-
Coprocessor	PowerQuad (DSP)	Yes	-	-
	Smart Direct Memory Access (SmartDMA)	-	Yes	Yes
	Neural Processing Unit (NPU)	-	-	-
	CoolFlux DSP	-	-	-
	CASPER	Yes	-	-
	Math Acceleration Unit (MAU)	-	Yes	Yes
Memory	Flash	128 KB or 256 KB	128 KB or 256 KB with 8 KB Customer Manufacturing Programmable Area (CMPA)	512 KB or 1024 KB with 56 KB secure installer and with 8 KB CMPA
	Flash cache	8 KB	8 KB	8 KB
	SRAM	Up to 112 KB (no ECC) With 16 KB (with ECC)	Up to 64 KB Including 8 KB shared with cache Including 8 KB with ECC	Up to 256 KB Including 8 KB shared with cache Include 8 KB with ECC
	FlexSPI	Yes, with 8 KB cache, support (Execute-in-Place) XIP, Octal/Quad SPI	-	-
	Read-Only Memory (ROM)	Yes	Yes	Yes
	One-Time Programmable Electronic Fuse (OTP e-Fuse)	Yes	-	-
Security	Secure key management	Physical Unclonable Function (PUF/UDF)	-	PKC

Table 1. MCX A343/344, MCX A365/366, and LPC5534/36/S36 high-level comparison*...continued*

Features		LPC5534/36/S36	MCX A343/344	MCX A365/366
	Secure subsystem	Yes	Yes	Yes
	Anti tamper pin	4x pins	-	6x pins
	Generic Lightweight Integrity Key (GLIKEY)		Yes	Yes
	True Random Number Generator (TRNG)	Yes	-	Yes
	AES	AES-256	-	AES-256
	ECC	ECC P-256	-	ECC-384
	RSA	RSA-2048/4096	-	RSA-2048/3072
	Secure Hash Algorithm (SHA)	SHA-224/256/384/512 HMAC SHA-256	-	SHA-256/384/512 HMAC SHA-256
	DICE	Yes	-	-
	UUID	128-bit	128-bit	128-bit
	Device lifecycle management	-	Yes	Yes
	Code read protection	Yes	Yes	Yes
	Master Boot Control (MBC)	-	Yes	Yes
	PRINCE	Yes	-	-
	Code watchdog	1x	1x	2x
	Secure installer	-	-	Yes
General system	Direct Memory Access (DMA)	2x DMA (52 channels/16 channels)	1x DMA (8 channels)	1x DMA (8 channels)
	Cyclic Redundancy Check (CRC)	Yes	Yes	Yes
Clock system	Free-Running Oscillator (FRO) 1 MHz	Yes	-	-
	FRO12 MHz	Yes	-	-
	FRO 96/12 MHz	Yes	-	-
	FRO144 MHz	-	-	-
	FRO 180 MHz	-	Yes	Yes
	FRO192 MHz	-	-	-
	FRO 32 kHz	Yes	-	-
	FRO16 kHz	-	Yes	Yes
	32 kHz Crystal Oscillator (RTCOSC)	Yes	-	-

Table 1. MCX A343/344, MCX A365/366, and LPC5534/36/S36 high-level comparison*...continued*

Features		LPC5534/36/S36	MCX A343/344	MCX A365/366
	External Crystal Oscillator (SOSC)	16 MHz or 32 MHz	8 MHz to 50 MHz	8 MHz to 50 MHz
	Phase-Locked Loop (PLL)	2x PLL, up to 550 MHz	-	1x PLL, up to 550 MHz
Communication interface	Universal Asynchronous Receiver/Transmitter (UART)	8x Flexcomm 1x High-speed SPI (50 MHz)	4x	6x
	SPI		2x	4x
	I2C		2x	2x
	Inter-IC Sound/ Synchronous Audio Interface (I2S/SAI)		-	-
	I3C	1x	-	1x
	Flexible Input/Output (FlexIO)	-	-	1x
	Controller Area Network (CAN)	1x	1x	2x
	High-speed USB	-	-	-
	Full-speed USB	1x Device/Host	-	1x Device/Host
	Ultra Secure Digital Host Controller (uSDHC)	1x	-	-
Analog	ADC	4x single-ended input 16-bit 2.0 Msps	2x single-ended input 16-bit 3.0 Msps	4x single-ended input 16-bit 3.2 Msps
		2x differential input 16-bit 2.0 Msps	Emulated as a single-channel differential input with 16-bit resolution and a sample rate of 3.0 Msps	Emulated as a dual-channel differential input with 16-bit resolution and a sample rate of 3.2 Msps
		4x single-ended input 12-bit 3.2 Msps	2x single-ended input 12-bit 3.75 Msps	4x single-ended input 12-bit 4.0 Msps
		2x differential input 12-bit 3.2 Msps	Emulated as a single-channel differential input with 12-bit resolution and a sample rate of 3.75 Msps	Emulated as a dual-channel differential input with 12-bit resolution and a sample rate of 4.0 Msps.
	DAC	3x 12bit DAC 1 Msps	-	1x 12bit DAC 1 Msps
	Comparator	3x HighSpeed CMP	3x High-speed CMP	3x HighSpeed CMP
	OPAMP	4x OPAMP with PGA	3x OPAMP without PGA	4x OPAMP without PGA
	Internal VREF	Internal VREF source	-	-

Table 1. MCX A343/344, MCX A365/366, and LPC5534/36/S36 high-level comparison*...continued*

Features		**LPC5534/36/S36**	**MCX A343/344**	**MCX A365/366**
Motor control subsystem	FlexPWM	2x FlexPWM (4x submodule for each)	2x FlexPWM (4x submodule for each)	2x FlexPWM (4x submodule for each)
	ENC/QEI/QDC	2x QEI	2x QDC	2x QDC
	AND/OR Inverter (AOI)	2x	2x	2x
Timers	Ctimer	5x 32-bit	3x 32-bit	5x 32-bit
	SCTimer/PWM	1x 32-bit or 2x 16-bit	-	-
	Low-Power Timer	-	1x	1x
	Frequency Measurement Timer	1x	1x	1x
	MRT	4x	1x	1x
	WWT	1x	1x	1x
	RTC	RTC with calendar	Simple RTC without calendar and external 32 kHz crystal	Simple RTC without calendar and external 32 kHz crystal
	Micro timer (UTICK)	1x	1x	1x
	OS event timer	1x	1x	1x
Human Machine Interfaces (HMI)	Digital Pulse-Density Modulation (PDM) microphone	1channel; supports connection of up to 2x Microelectromechanical System (MEMS)	-	-
	Segment Liquid Crystal Display (LCD)	-	-	4 x 44 segment LCD interface
	General-Purpose Input/Output (GPIO)	66GPIOs on HLQFP100 39GPIOs on HTQFP64	86GPIOs on LQFP100 55GPIOs on LQFP64 41GPIOs on LQFP48 20GPIOs on H-PQFN32	114GPIOs on WFBGA169 114GPIOs on LQFP144 83GPIOs on LQFP100 53GPIOs on LQFP64
Operation details	Internal core buck DC-DC	Yes, 1.8 V to 3.6 V	-	-
	Internal core Low-Dropout Regulator (LDO)	Yes, 1.8 V to 3.6 V	Yes, 1.71 V to 3.6 V	Yes, 1.71 V to 3.6 V
	Always On Domain on VDD_VBAT pin	Yes, 1.71 V to 3.6 V	-	-
	Operating Voltage	1.8 V to 3.6 V	1.71 V to 3.6 V	1.71 V to 3.6 V
	Input/Output (I/O)	VDDIO_1 is 1.8 V to 3.6 V VDDIO_2 is 1.08 V to 3.6 V	VDDIO is only 1.71 V to 3.6 V	VDDIO is only 1.71 V to 3.6 V
	V_HBM	±2000 V	±2000 V	±2000 V
	V_CDM	±500 V	±500 V	±500 V
Package	WFBGA169	-	-	Yes
	LQFP144	-	-	Yes

Table 1. MCX A343/344, MCX A365/366, and LPC5534/36/S36 high-level comparison*...continued*

Features		LPC5534/36/S36	MCX A343/344	MCX A365/366
	HLQFP100	Yes	-	-
	LQFP100	-	Yes	Yes
	HTQFP64	Yes	-	-
	LQFP64	-	Yes	Yes
	LQFP48		Yes	-
	HVQFN48	Yes	-	-
	H-PQFN32	-	Yes	-

3 System module comparison

This section summarizes the key architectural differences between LPC5534/36/S36 and MCX A34/36 devices.

3.1 Memory system differences

The subsections that follow compare the internal flash, SRAM, alias windows, and ROM between LPC5534/36/S36 and MCX A34/36 devices and highlights practical migration steps.

3.1.1 Memory system on LPC5534/36/S36

Table 2 provides the memory layout and address mapping for the LPC5534/36/S36 devices.

Table 2. Memory system on LPC5534/36/S36

Memory type	Start address	End address	Size	MCU	Comment
Internal Flash	0x0000 0000	0x0003 D7FF	246 kB	LPC55(S)36	User Flash
	0x0003 D800	0x0003 FFFF	10 kB	LPC55(S)36	CMPA
SRAM	0x2000 0000	0x2001 BFFF	112 kB	LPC55(S)36	SRAM on CM33 system bus
SRAM X	0x0400 0000	0x0000 3FFF	16 kB	LPC55(S)36	SRAM X on CM33 code bus
FlexSPI	0x0800 0000	0x0FFF FFFF	Up to 128 MB	LPC55(S)36	-
Boot ROM	0x0300 0000	0x0302 FFFF	192 kB	LPC55(S)36	On CM33 code bus

3.1.2 Memory system on MCX A344

Table 3 outlines the memory layout and address mapping for the MCX A344 device.

Table 3. Memory system on MCX A344

Memory type	Start address	End address	Size	MCU	Comment
Internal Flash	0x0000 0000	0x0003 DFFF	248 kB	MCX A344	User Flash
	0x0003 E000	0x0003 FFFF	8 kB	MCX A344	CMPA
SRAM	0x2000 0000	0x2000 BFFF	48 kB	MCX A344	SRAM on CM33 system bus
SRAM X0_ Alias	0x2000 C000	0x2000 FFFF	8 kB	MCX A344	SRAM X0 alias to CM33 code bus

Table 3. Memory system on MCX A344*...continued*

Memory type	Start address	End address	Size	MCU	Comment
SRAM X0	0x0400 0000	0x0400 1FFF	8 kB	MCX A344	SRAM X0 on CM33 code bus, can be set alias to SRAM on CM33 system bus
SRAM X1	0x0400 2000	0x0400 3FFF	8 kB	MCX A344	SRAM X1 on CM33 code bus, can be LPCACHE
Boot ROM	0x0300 0000	-	-	MCX A344	On CM33 code bus

3.1.3 Memory system on MCX A366

Table 4 outlines the memory layout and address mapping for the MCX A366 device.

Table 4. Memory system on MCX A366

Memory type	Start address	End address	Size	MCU	Comment
Internal Flash	0x0000 0000	0x000F DFFF	1016 kB	MCX A366	User Flash
	0x000F E000	0x000F FFFF	8 kB	MCX A366	CMPA
SRAM	0x2000 0000	0x2003 BFFF	240 kB	MCX A366	SRAM on CM33 system bus
SRAM X0_ Alias	0x2003 C000	0x2000 FFFF	8 kB	MCX A366	SRAM X0 alias to CM33 code bus
SRAM X0	0x0400 0000	0x0400 1FFF	8 kB	MCX A366	SRAM X0 on CM33 code bus, can be set alias to SRAM on CM33 system bus
SRAM X1	0x0400 2000	0x0400 3FFF	8 kB	MCX A366	SRAM X1 on CM33 code bus, can be LPCACHE
Boot ROM	0x0300 0000	-	-	MCX A366	On CM33 code bus

3.1.4 Memory system comparison

On the MCX A34/36 MCUs, the memory address is compatible with LPC5534/36/S36 devices.

3.2 Clock source differences

The system clocking module provides the clock signals to the core, memories, and peripherals (register interfaces and peripheral clocks).

3.2.1 Clocking diagram on LPC5534/36/S36

Figure 1 presents the LPC5534/36/S36 clocking scheme, including the main clock sources and their distribution to the CPU, AHB, and APB domains.

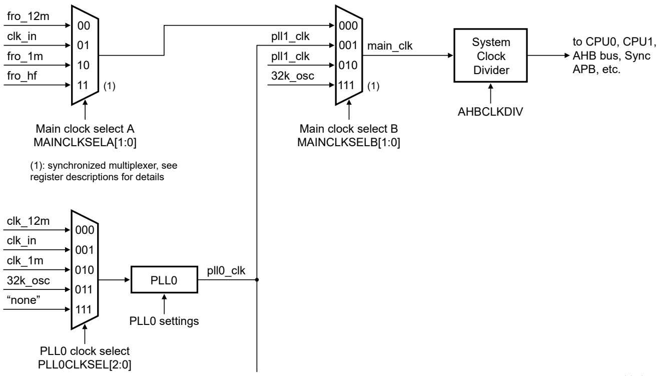

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Figure 1. LPC5534/36/S36 CPU, AHB, and APB bus clock diagram

3.2.2 Clocking diagram on MCX A343/344

Figure 2 presents the MCX A343/344 clocking scheme, highlighting the main oscillators, dividers, and system clock paths.

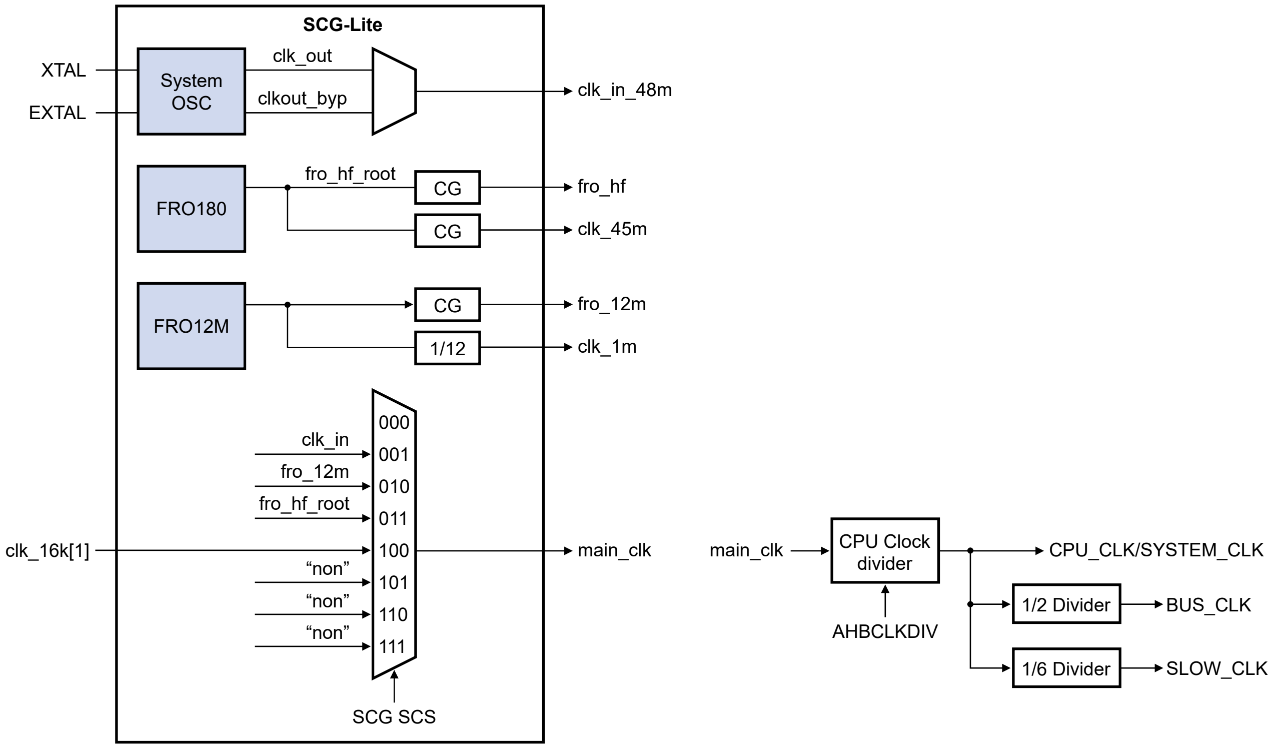

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Figure 2. MCX A343/344 CPU, AHB and APB bus clock diagram

3.2.3 Clocking diagram on MCX A365/366

The MCX A34/36 devices added SLOW clock (1/6 CPU clock) to flash memory, APB bus, and other domain. This SLOW clock is not available on the LPC5534/36/S36 devices.

Figure 3 shows the CPU, AHB, and APB clocking structure for the MCX A345/346 and A365/366 devices.

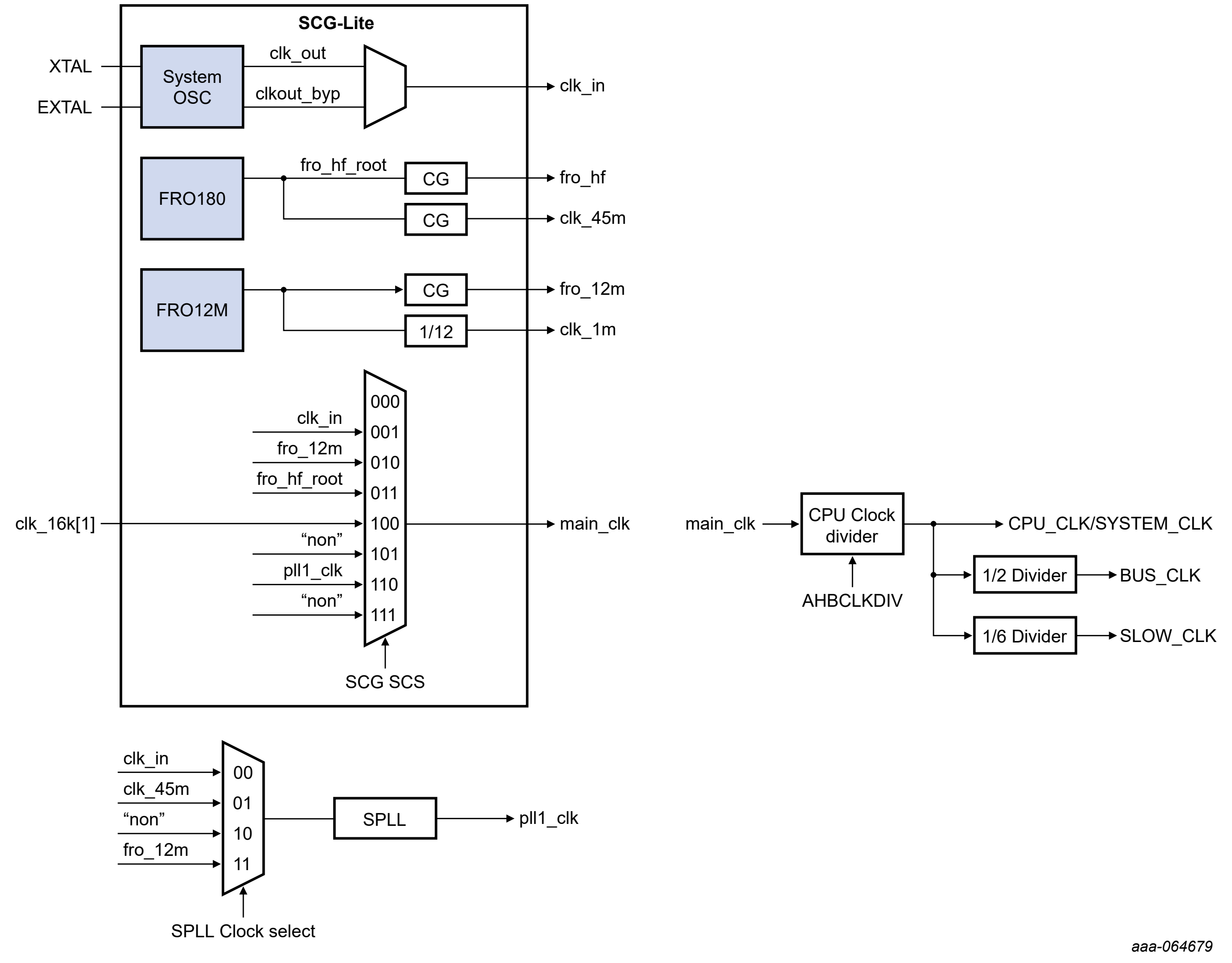

Figure 3. MCX A345/346 and A365/6 CPU, AHB, and APB bus clock diagram

3.2.4 Clock features comparison

Compared with LPC5534/36/S36, MCX A34 and A36 family devices do not support an external 32 kHz crystal. MCX A34/36 internal clock source FRO180M increased accuracy to ±1 %.

Table 5 compares the key clock features of the MCX A34/36 and LPC5534/36/S36 devices.

Table 5. MCX A343/344, MCX A365/366, and LPC5534/36/S36 clock feature comparison

Feature	MCX A343/344	MCX A365/366	LPC5534/36/S36
Max Core Frequency	180 MHz	240 MHz	150 MHz
PLL	No PLL	1x PLL up to 550 MHz	2x PLL up to 550 MHz
External Oscillator	8 MHz to 50 MHz	8 MHz to 50 MHz	16 MHz or 32 MHz 32.768 kHz
Internal FRO	FRO180M (180 MHz, ±1 %) FRO12M (12 MHz, ±3 %) FRO16K (16 kHz, ±6 %)	FRO180 M (180 MHz, can set to 240 MHz, ±1 %)) FRO12M (12 MHz, ±3 %) FRO16K (16 kHz, ±6 %)	FRO-96/12 MHz (96 MHz, ±2 %) FRO-1 MHz (±15 %) FRO-32 kHz (±2 %)

4 Peripheral module comparison

The peripheral module comparison highlights the architectural and functional differences between LPC5534/36/S36 and MCX A334/36 peripherals. It summarizes which modules were redesigned, removed, or enhanced.

4.1 Changed modules

The subsections that follow describe the peripheral modules that have been redesigned in the MCX A34/36 devices. Although their functionality remains broadly similar to LPC5534/36/S36 devices, some updates may require driver or configuration adjustments.

4.1.1 SYSCON

The SYSCON module has been redesigned in the MCX A34/36 devices; however, its overall functionality remains consistent with that of the LPC5534/36/S36 devices.

4.1.2 Internal flash memory

The internal flash module has been redesigned in the MCX A34/36 devices, although its overall functionality remains comparable to the LPC5534/36/S36 devices. The MCX A34/36 also provide faster flash performance than the LPC5534/36/S36.

Table 6. MCX A34/36 and LPC5534/36/S36 flash feature comparison

Feature	Description	MCX A34/36	LPC5534/36/S36
Flash array - Phrase	Represents the smallest portion of the flash memory that can be programmed in a single operation.	The MCX A34/36 devices program flash in 16-byte phrases.	The LPC5534/36/S36 devices do not have flash phrases and instead require a minimum program size of 512 bytes.
Flash array - sector	Represents the smallest portion of the flash memory that can be erased in a single operation.	The MCX A34/36 flash architecture uses 8-KB sectors for erase operations.	The LPC5534/36/S36 architecture uses a minimum erase size of 512 bytes.
Flash array - Page	Represents the largest portion of the flash memory that can be programmed in a single operation.	The MCX A34/36 devices allow programming up to 128 bytes.	The LPC5534/36/S36 devices allow programming up to 512 bytes.
Flash memory controller - Prefetch buffer	Prefetch the next 128-bit flash memory location.	The MCX A34/36 devices use a 16-byte prefetch buffer.	NA
Flash memory controller - Cache	The flash cache memory stores already fetched data. This code is immediately available for repeated execution without any wait states. If needed, it operates as a one-set, four-way associative cache with 128-bit (16-byte) cache line entries.	The MCX A34/36 devices implement a 64-byte, one-set, four-way associative flash cache with 128-bit (16-byte) cache lines.	NA
Functional Safety - Flash ECC		The MCX A34/36 devices support one-bit error correction and two-bit error detection.	The LPC5534/36/S36 devices support only one-bit error correction.

Table 6. MCX A34/36 and LPC5534/36/S36 flash feature comparison*...continued*

Feature	Description	MCX A34/36	LPC5534/36/S36
Functional Safety - Flash Error Reporting Module (ERM)	The ERM provides information and optional interrupt notification on memory ECC and parity error events.	The MCX A34/36 devices report ECC two-bit errors.	NA
Functional Safety - Flash EIM	The EIM provides a method for diagnostic coverage of internal memories. It enables you to induce artificial errors on error-checking mechanisms.	The MCX A34/36 devices support both single-bit and double-bit error injection	NA
Flash performance - Access frequency	The flash access timing is configured using either the FCTRL[RWSC] register or the FLASHTIM setting.	The MCX A34/36 devices require: • 200 MHz < Freq <= 240 MHz, RWSC = 5, 6 system clocks flash access time. • 160 MHz < Freq <= 200 MHz, RWSC = 4, 5 system clocks flash access time. • 120 MHz < Freq <=160 MHz, RWSC = 3, 4 system clocks flash access time. • 80 MHz < Freq <=120 MHz, RWSC = 2, 3 system clocks flash access time. • 40 MHz < Freq <=80 MHz, RWSC = 1, 2 system clocks flash access time. • 40 MHz or below, RWSC = 0, 1 system clock flash access time.	The LPC5534/36/S36 devices require: • 150 MHz, when FLASHTIM = 0xB, 12 system clocks flash access time. • 100 MHz, when FLASHTIM = 0x7, 8 system clocks flash access time. • 12 MHz, when FLASHTIM = 0x1, 2 system clocks flash access time.

4.1.3 IOCON to PORT comparison

In the MCX A34/36 devices, the PORT module replaces the IOCON module used in LPC5534/36/S36 devices, while maintaining largely similar functionality.

4.1.4 GPIO

The GPIO module has been redesigned in the MCX A34/36 devices, although its overall functionality remains comparable to that of the LPC5534/36/S36. The MCX A34/36 GPIO only supports an I/O supply range of 1.71 V to 3.6 V, whereas the LPC5534/36/S36 support two main I/O supply domains:

- VDDIO_1 (1.8 V to 3.6 V)
- VDDIO_2 (1.08 V to 3.6 V)

Unlike the LPC5534/36/S36 devices, which provides true open-drain capability on pins PIO0_13 and PIO0_14, the MCX A34/36 devices do not support open-drain I/O. The MCX A34/36 devices also support up to eight high-drive-strength GPIO pins capable of sourcing up to 20 mA per pin, and they provide 5 V-tolerant input capability on two GPIO pins.

4.1.5 RTC

The RTC module has been redesigned in the MCX A34/36 devices. The LPC5534/36/S36 include a full-function RTC with calendar capability and support for an external 32 kHz crystal input. In contrast, the MCX A34/36 devices provide only a simplified RTC that does not include calendar functionality or an external 32 kHz input, relying solely on the internal FRO16K oscillator.

4.1.6 LPTMR and WKT

The LPC5534/36/S36 devices integrate the Wake-Up Timer (WKT), whereas the MCX A34/36 devices use the Low-Power Timer (LPTMR). The LPTMR and WKT provide similar functionality.

The LPTMR can be configured to operate either as a time counter with an optional prescaler or as a pulse counter with an optional glitch filter, across all power modes, including low-power states. It is reset only during a VSYS warm reset, allowing it to serve as a basic time-of-day counter.

4.1.7 I3C

The I3C module on the MCX A345/346 and MCX A365 366 devices has been updated based from the LPC5534/36/S36 implementation, while maintaining largely similar functionality. The MCX A343 and MCX A344 devices do not include an I3C module.

4.1.8 CAN

Both the LPC5534/36/S36 and MCX A34/36 devices include a CAN module. Although the CAN module architecture has been redesigned in the MCX A34/36 devices, the overall functionality remains largely similar to that of LPC5534/36/S36. Both the family devices support the CAN 2.0 and CAN-FD communication protocols.

4.1.9 Flexcomm and LPUART/LPI2C/LPSPI

The LPC5534/36/S36 devices use the Flexcomm architecture to support USART, SPI, I2C, and I2S peripherals, whereas the MCX A34/36 devices do not support Flexcomm and LP_Flexcomm modules.

In the MCX A34/36 devices, the UART module has been fully redesigned; although the core functionality is retained, however; there are notable differences exist:

- The LPUART in the MCX A34/36 devices do not support Synchronous mode and 32 kHz Clock operation mode.
- It adds support for TXD and RXD signal swapping, operation up to 24 MHz, and received-idle detection.

The I2C module has also been redesigned in the MCX A34/36 devices, while maintaining functionality similar to that of LPC5534/36/S36. The SPI module has been updated as well, and the LPSPI on MCX A34/36 also supports 2-bit and 4-bit modes, which are not available in the LPC5534/36/S36 SPI implementation.

4.1.10 I2S

The LPC5534/36/S36 device use an I2S interface provided by the Flexcomm module for connecting to audio codecs. In contrast, the MCX A34/36 devices do not include a native I2S interface. However, similar I2S functionality can be emulated on MCX A 34/36 devices using the FlexIO module.

4.1.11 DMIC

The LPC5534/36/S36 devices use a DMIC interface for receiving Pulse-Density Modulation (PDM) data from multiple digital microphones and processes it to produce 24-bit Pulse Code Modulation (PCM) data. The MCX A34/36 devices do not include any DMIC or MICFIL.

4.1.12 USB

The USB module has been redesigned in the MCX A34/36 devices; however, its overall functionality remains largely similar to that of the LPC5534/36/S36 devices.

4.1.13 DMA

The DMA module has been redesigned in the MCX A34/36 devices; however, its overall functionality remains similar to that of the LPC5534/36/S36 devices.

4.1.14 New modules

The SYSCON module configuration has been fully redesigned in the MCX A34/36 devices.

4.1.15 CMC

The LPC5534/36/S36 do not include a Core Mode Controller (CMC), whereas the MCX A34/36 devices integrate this feature. The CMC manages the sequencing of the CPU and associated logic through the different operating modes.

4.1.16 EIM

The LPC5534/36/S36 devices do not integrate EIM, whereas the MCX A34/36 devices integrate this feature.

The EIM is primarily used for diagnostic purposes and provides a method for diagnostic coverage of internal memories, such as system RAM, cache RAMs, and peripheral memories. See the chip specific EIM information to determine which functional safety features are supported by this method.

The EIM allows users to inject artificial errors on error-checking mechanisms of a system, such as Error Correcting Code (ECC) for RAM read data and parity bits. For each such mechanism that EIM supports on the chip, EIM can inject single-bit and multibit inversions on data in the applicable target bus. Injecting faults on memory accesses can be used to exercise the Single-Error Correction - Double-Error Detection (SEC-DED) ECC function of the related system.

4.1.17 ERM

The LPC5534/36/S36 devices do not integrate ERM, whereas the MCX A34/36 devices integrates this feature.

The ERM provides information and optional interrupt notification on memory error events associated with ECC and parity. The ERM collects error events on memory accesses for memory arrays, such as flash memory, system RAM, or peripheral RAMs. ERM supports various channels for memory sources where each ERM channel is associated with a different memory module. See the chip specific ERM information for details about supported memory sources and specific memory channel assignments.

If the memory supports ECC, then ERM syndrome and error address information are captured along with the error event. ERM does not capture syndrome or error address for cache memories or memory with parity instead of ECC.

4.1.18 14-bit DAC and 12-bit DAC

The LPC5534/36/S36 devices include three instances of the 12-bit, 1 Msps DAC module: DAC0, DAC1, and DAC2, each supported by a compatible DAC controller. The MCX A343/344 devices do not include a DAC module. The MCX A365/366 devices provide a single instance of a 12-bit, 1 Msps DAC module (DAC0) with a compatible DAC controller.

4.1.19 FlexIO

The LPC5534/36/S36 and MCX A343/344 devices do not integrate a FlexIO module, whereas the MCX A365/366 devices integrate this feature.

The FlexIO module, originally introduced in the Freescale Kinetis KL43 family, can emulate various serial communication protocols, such as UART, SPI, and I2C.

The FlexIO module is flexible, and can be configured according to the communication requirements. The main components of the FlexIO module are the shifters, timers, and pins. Data is loaded into a shifter, and a timer generates the shifter clock and use a pin to output the data from the shifter.

4.1.20 SmartDMA

The LPC5534/36/S36 devices do not include SmartDMA, whereas the MCX A34/36 devices integrate this feature.

SmartDMA is a lightweight processing core that supports a reduced instruction set and operates similarly to an Arm core.

As the controller of the AHB matrix, SmartDMA can access all its assigned targets, including GPIO peripheral control and data registers. Its primary purpose is to handle event-driven and I/O-driven tasks to offload workload from the Arm processor in the system.

4.1.21 MAU and PowerQuad

The MCX A34/36 devices use MAU to accelerate math calculation. The MAU supports operations, such as trigonometric, reciprocal, square, square root, sine, cosine and, arctan algorithms.

In contrast, the LPC5534/36/S36 devices support PowerQuad to accelerate math calculation. PowerQuad includes seven internal computation engines that support:

- Transform operations
- Transcendental functions
- Trigonometry functions
- Dual biquad Infinite Impulse Response (IIR) filtering
- Matrix accelerator
- Finite Impulse Response (FIR) filtering
- Coordinate Rotation Digital Computer (CORDIC)

4.1.22 Segment LCD

The LPC5534/36/S36 and MCX A343/344 devices do not integrate a segment LCD interface. In contrast, the MCX A365/366 devices integratea segment LCD interface that supports panels with up to a 4×44 segment LCD panel.

4.1.23 OPAMP

Both the LPC5534/36/S36 and MCX A34/36 devices integrate OPAMPs. However, the OPAMPs in the MCX A34/36 devices do not include a Programmable Gain Amplifier (PGA) and offer improved slew rate performance compared to the OPAMPs in the LPC5534/36/S36 devices.

5 Boot mode

This section outlines the boot options and ISP interfaces supported by the MCX A34/36 and LPC5534/36/S36 devices, highlighting key differences that affect migration.

5.1 Serial download mode

Table 7 compares the boot devices and supported ISP interfaces for the MCX A34/36 and LPC5534/36/S36 devices.

Table 7. Boot device comparison

Part Number	Boot Device	Description
MCX A3xx	Internal flash only	Supports ISP only through LPUART. Does not support ISP via LPI2C, LPSPI, FlexCAN, and USB.
LPC55(S)3x	Internal flash Serial NOR flash via FlexSPI Serial NAND flash via FlexSPI	Supports ISP through UART, SPI, I2C, CAN, and USB.

For more information about the MCX A34/36 Booting options, refer to MCX A3xx SoC Reference Manual.

6 Development environment and tools

This section summarizes the software packages, IDEs, debug tools, and utility programs supported by the MCX A34/36 and LPC5534/36/S36 devices, outlining the development resources available for building, debugging, and programming applications on both platforms.

6.1 Software support package and tools

Table 8 provides a comparison of the software packages, development tools, and utilities supported by the MCX A34/36 and LPC5534/36/S36 devices.

Table 8. Software support package and tools comparison

IDE	MCX A34/36	LPC5534/36/S36	Description
SDK	MCUXpresso SDK	MCUXpresso SDK	Provides the drivers and example projects for both the series, MCX A3xx and LPC55(S)3x.
IDE	IAR KEIL MCUXpresso GCC Visual Studio Code	IAR KEIL MCUXpresso GCC	Provides the development IDEs to program, compile, debug, and download applications.
Debug tool	J-Link ULINK2 DAP-Link MCU-Link	J-Link ULINK2 DAP-Link MCU-Link	It is used to debug the software on the chips.
Serial download tool	blhost.exe	blhost.exe	Like the MFG tool, it is used to program images to the boot devices directly using the serial downloader.

Table 8. Software support package and tools comparison*...continued*

IDE	MCX A34/36	LPC5534/36/S36	Description
Image tool	elftosb.exe	elftosb.exe	It is used to generate bootable images, including signed or encrypted images.

7 Hardware design

This section summarizes key hardware differences between the LPC5534/36/S36 and MCX A34/36 devices.

7.1 Power supply

The subsections that outlinesthe power-supply requirements for MCX A34/36 and LPC5534/36/S36 devices.

7.1.1 Power supply on MCX A34/36 devices

The MCX A34/36 devices only support LDO mode.

Figure 4 shows the typical power supply configuration for MCX A34/36 devices.

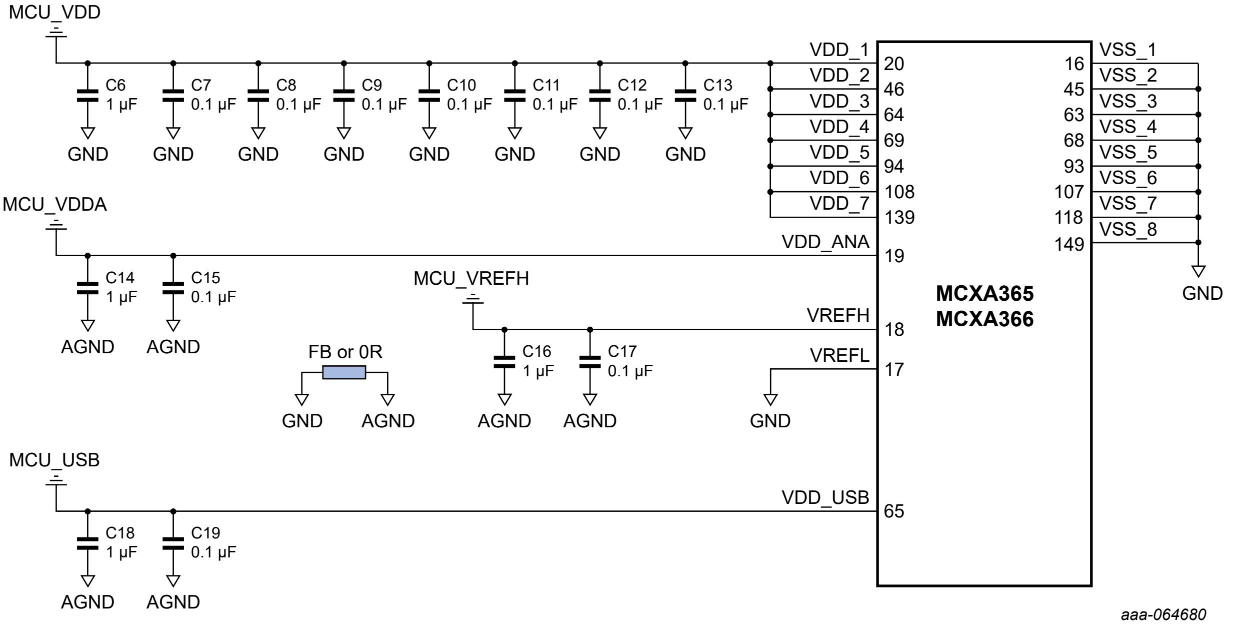

Figure 4. MCX A34/36 power supply system

7.1.2 Power supply on LPC5534/36/S36 devices

ALL LPC5534/36/S36 devices support an internal DC-DC converter and a selectable LDO such that DC-DC converter can be bypassed.

Figure 5 and Figure 6 illustrate the recommended power supply configurations for LPC5534/36/S36 devices.

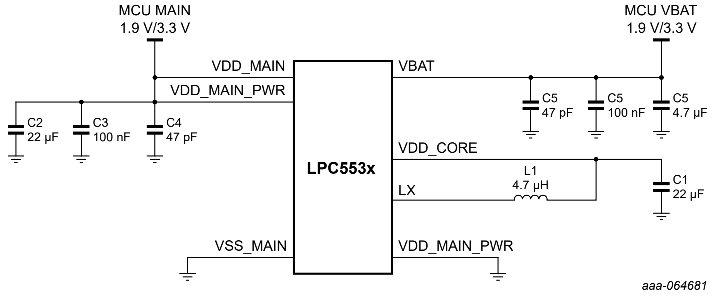

Figure 5. Using internal DC-DC converter (Power-efficient)

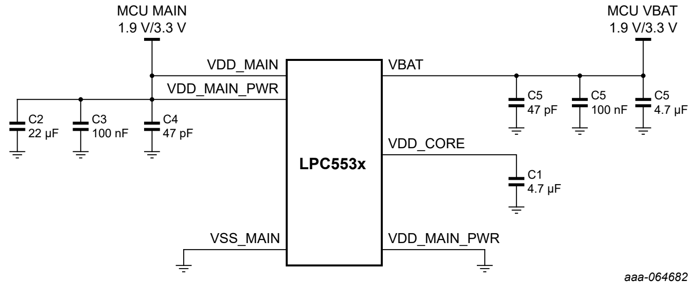

Figure 6. Using internal LDO(Low-cost)

7.2 Oscillator design

Table 9 compares the oscillator options supported by the MCX A34/36 and LPC5534/36/S36 devices, highlighting key differences in external clock sources and 32 kHz crystal support.

Table 9. Oscillator design

Oscillator design	MCX A34/36	LPC5534/36/S36
External oscillator support	Supports an external oscillator in the range of 8 MHz to 50 MHz	Support an external oscillator ranging at 16 MHz or 32 MHz and a software-configurable capacitor bank.
32 kHz oscillator support	Does not support an external 32 kHz oscillator	Support external 32.768 kHz oscillator and support software-configurable capacitor bank

7.3 Wake-up timing

Table 10 compares the wake-up times of the LPC5534/36/S36 and MCX A34/36 devices across various low-power modes.

Table 10. Wake-up timing comparison

Part Number	Sleep	Deep Sleep	Power Down	Deep power down
LPC55(S)3x	3.2 µS	76 µS	405 µS	2.9 ms
MCX A343/A344	0.24 µS	9.18 µS	19.36 µS	0.81 ms
MCX A365/A366	0.42 µS	9.01 µS	18.84 µS	1.57 ms

7.4 Package/Pinout differences

The following list summarizes the package and pinout options available across the LPC5534/36/S36 and MCX A34/36 device families:

- The LPC5534 and LPC5536 devices are available in HVQFN48, HTQFP64, and HLQFP100 packages.
- The LPC55S36 device is available in HVQFN48 and HLQFP100 packages.
- The MCX A343/A344 devices are offered in LQFP100, LQFP64, LQFP48, and H-PQFN32 packages.
- The MCX A365/A366 devices are offered in WFBGA169, LQFP144, LQFP100, and LQFP64 packages.

7.5 Minimum system consideration

When migrating from LPC5534/36/S36 to MCX A34/36 devices, several hardware considerations must be reviewed. Although both families share similar reset, ISP, and debug circuits for a minimum system, their power supply architectures differ significantly. The LPC5534/36/S36 devices support an integrated DC-DC converter, whereas the MCX A34/36 devices rely solely on an LDO-based power supply. Therefore, appropriate adjustments to the power supply circuit are required during migration.

8 Acronyms

Table 11 lists the acronyms used in this document.

Table 11. Acronyms

Acronym	Description
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
AOI	AND/OR Inverter
CAN	Controller Area Network
CAN FD	Controller Area Network Flexible DataRate
CMC	Core Mode controller
CMPA	Customer Manufacturing Programmable Area
CORDIC	Coordinate Rotation Digital Computer
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DICE	Device Identifier Composition Engine
DMA	Direct Memory Access
DMIC	Digital Microphone Interface
DSP	Digital Signal Processing
ECC	Elliptic Curve Cryptography
EIM	Error Ingestion Module
ELS	EdgeLock Subsystem
ERM	Error Recording Module
FIR	Finite Impulse Response
FlexIO	Flexible Input/Output
FlexSPI	Flash Execute-in-Place Serial Peripheral Interface
FRO	Free-Running Oscillator
GLIKEY	Generic Lightweight Integrity Key

Table 11. Acronyms*...continued*

Acronym	Description
GPIO	General Purpose Input/Output
V_CDM	Electrostatic Discharge Voltage, Charged-Device Model
V_HBM	Electrostatic Discharge Voltage, Human Body Model
H-PQFN	Thermal Enhanced - Plastic Quad Flat Non-Lead
HVQFN	Plastic, Thermal Enhanced Very Thin Quad Flat Package
I/O	Input/Output
SAI	Synchronous Audio Interface
IIR	Infinite Impulse Response
IP	Intellectual Property
I2C	Inter Integrated Circuit
I2S	Inter-IC Sound
I3C	Improved InterIntegrated Circuit
LCD	Liquid Crystal Display
LPTMR	Low-Power Timer
LPUART	LowPower Universal Asynchronous ReceiverTransmitter
MAU	Math Acceleration Unit
MBC	Master Boot Control
MCU	Microcontroller Unit
MEMS	Microelectromechanical system
MICFIL	Microphone Interface
MRT	Multi-Rate Timer
NPU	Neural Processing Unit
OPAMP	Operational Amplifier
OS	Operating System
OTP eFuse	One Time Programmable Electronic Fuse
PCM	Pulse Code Modulation
PDM	Pulse Density Modulation
PKC	Public Key Cryptography
PLL	Phase-Locked Loop
PUF	Physical Unclonable Function
QDC	Quadrature Decoder Controller
QEI	Quadrature Encoder Interface
ROM	ReadOnly Memory
RSA	Rivest–Shamir–Adleman
RTC	Real-Time Clock
SCTimer/PWM	Serial Communication Interface Timer / PulseWidth Modulator

Table 11. Acronyms*...continued*

Acronym	Description
SEC-DED	SingleError Correction - DoubleError Detection
SGI	Security Generation Index
SHA	Secure Hash Algorithm
SmartDMA	Smart Direct Memory Access
SOSC	System Oscillator
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
TRNG	True Random Number Generator
UART	Universal Asynchronous Receiver/Transmitter
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
uSDHC	Ultra Secure Digital Host Controller
UUID	Universally Unique Identifier
WKT	Wake-up Timer
WWDT	Windowed Watchdog Timer

9 Related documentation

Table 12. Related documentation/resources

Document	Link/how to access
LPC553x Reference Manual (document LPC553x RM)	LPC553xRM
Migration Guide from LPC55xx to MCX Nx4x (document AN14249)	AN14249
MCX A345, A346, A355, A356, A365 and A366 Reference Manual (document MCXAP144M240 F60RM)	MCXAP144M240F60RM
MCX A343 and MCX A344 Reference Manual (document MCXAP100M180F40RM)	MCXAP100M180F40RM

10 Revision history

Table 13 summarizes the revisions to this document.

Table 13. Revision history

Document ID	Release date	Description
AN14917 v.1.0	5 March 2026	Initial public release

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Date of release: 5 March 2026
Document identifier: AN14917