AN14790

PF51x3 hardware design guide

Rev. 1.0 — 9 April 2026 **Application note**

Document information

Information	Content
Keywords	PMIC, Low-voltage, Automotive, RADAR, ASIL B
Abstract	The PF51x3 integrates multiple high performance buck regulators and LDO regulators. It can operate as a standalone point-of-load regulator IC, or as a companion chip to a larger PMIC. PF51x3 is a low-voltage PMIC family integrating three part numbers: the PF5103 (full option device), the PF5113 for NXP RADAR applications, and the PF5123 (without LDO). This family can be used for many general applications, including infotainment, domain controllers, and high-end consumer and industrial applications.

1 Introduction

1.1 Device description

The PF51x3 is a power management integrated circuit (PMIC) designed to be the primary core power supply for high-end ADAS application processors. For the full capability of the PF51x3 family, we have this list of features:

- Buck regulators
  - SW1, SW2, SW3: 0.5 V to 3.3 V; 3500 mA; 1.5 % accuracy
  - Dynamic voltage scaling
  - Configurable as multi-phase regulator
  - Programmable current limit (4 A, 5 A, 6 A)
- LDO regulators with load switch option
  - LDO1: 0.75 V to 3.3 V; 200 mA; 1.5 % accuracy
  - LDO2: 0.75 V to 3.3 V; 500 mA; 1.5 % accuracy
- PGOOD output
  - PGOOD output also used as processor reset signal
  - Independent safety assertion path for certain faults, to ensure safe state
- FCCU input
  - Monitoring MCU fault signal (by PWM detection or level detection)
- Advanced clock management
  - Clock synchronization through configurable input sync pin
  - Manual clock frequency tuning
- System features
  - Advanced state machine for seamless processor interface
  - I^2C communication interface (3.4 MHz)
  - Programmable soft start sequence and power-down sequence
  - Programmable regulator configuration
  - Advanced thermal monitoring and protection
- OTP (One-time programmable) memory for device configuration
- Functional Safety features to fit up to ASIL B safety level
  - Independent voltage monitoring with programmable fault protection; 1 % accuracy
  - Independent clock monitoring
  - Watchdog monitoring – simple
  - OV monitoring of internal regulators
  - I^2C CRC and secure write protection mechanism
  - Analog built-in self-test (ABIST)

1.2 Family overview

Table 1. PF51XX device family

Feature	PF5103	PF5113	PF5123
BUCK1	0.5 V to 3.3 V Current capability: 3.5 A (Single/multi phase)	0.8 V, 0.825 V, 0.9 V,1.2 V Current capability: 2.6 A (Single phase)	0.5 V to 3.3 V Current capability: 3.5 A (Single/multi-phase)
BUCK2	0.5 V to 3.3 V Current capability: 3.5 A (Single/multi phase)	1.3 V, 1.5 V, 1.8 V, 2.3 V, 2.5 V, 3.3 V Current capability: 3.5 A (Single phase)	0.5 V to 3.3 V, Current capability: 3.5 A (Single/multi-phase)
BUCK3	0.5 V to 3.3 V Current capability: 3.5 A (Single/multi phase)	1.1 V, 1.3 V, 1.5 V, 2.5 V, 3.3 V Current capability: 2.6 A (Single phase)	0.5 V to 3.3 V Current capability 3.5 A (Single/multi-phase)
LDO1	0.75 V to 3.3 V, 0.2 A	1.8 V or 3.3 V, 0.2 A	No
LDO2	0.75 V to 3.3 V, 0.5 A	1.8 V or 3.3 V, 0.25 A	No
PWRON	Yes	Yes	Yes
SYNC_STANDBY	Yes	Yes	Yes
XFAILB_FCCU	Yes	Yes	Yes
I2C	Yes	Yes	Yes
PGOOD	Yes	Yes	Yes
INTB_RSTB	Yes	Yes	Yes
Watchdog	Simple	Simple	Simple
Safety	QM, ASILB	QM, ASILB	QM, ASILB

2 Simplified block diagram

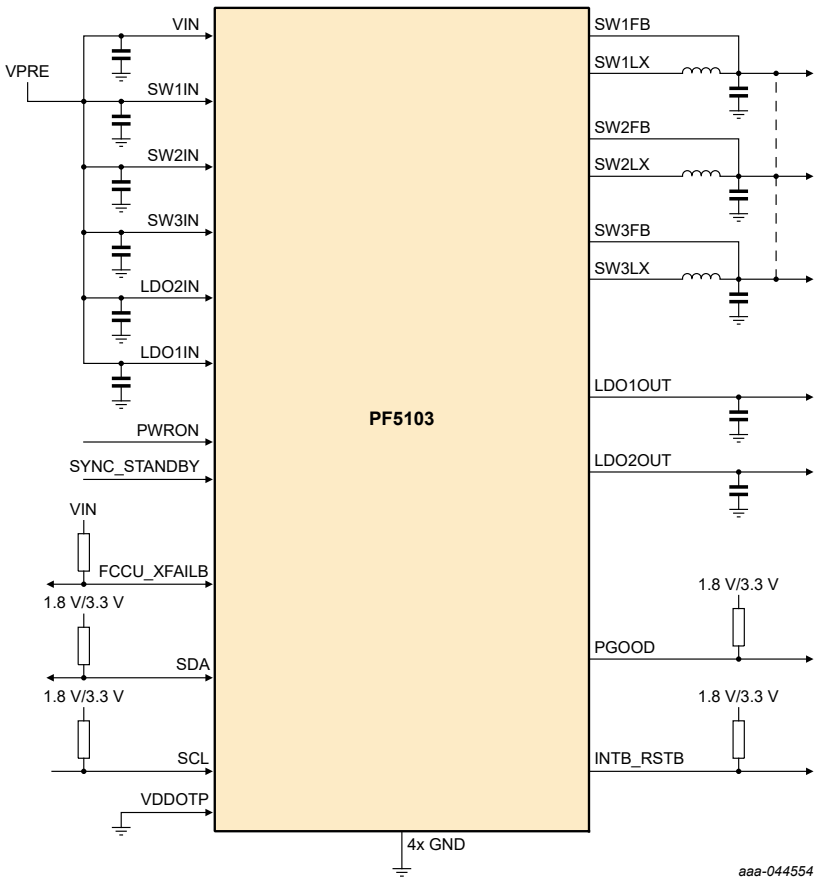


Figure 1. Simplified block diagram

Note:

- *PF5113 and PF5103 have the same hardware implementation*
- *For PF5123, we can unpopulate the capacitors for LDO1 and LDO2 and keep them floating*

3 Pinning Information

3.1 Pinout

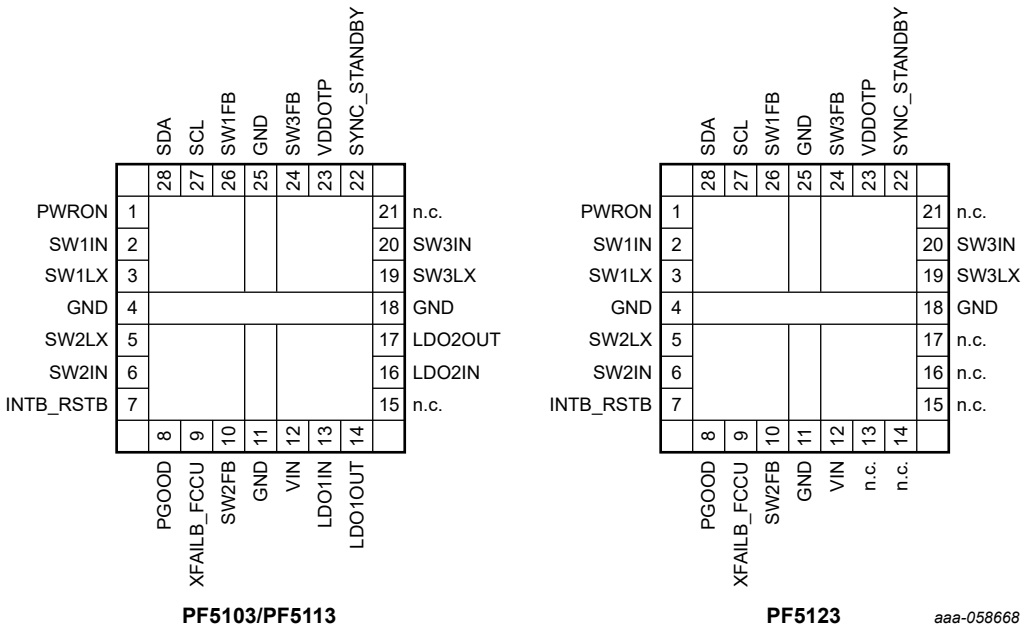


Figure 2. Pinning diagram

3.2 Unused pin termination

When a specific feature is not required on the system, certain rules should be followed to properly terminate the unused pins on the system. Likewise, some software/OTP configuration may be required to ensure proper operation of the PMIC.

Table 2. Unused pin termination

Pin number	Pin name	Connection if not used	OTP considerations
1	PWRON	Connect to VIN	
2	SW1IN	Leave floating	OTP_SW1_SEQ = 6b'000000
3	SW1LX	Leave floating	OTP_SW1_SEQ = 6b'000000
4	GND	Connect to ground	
5	SW2LX	Leave floating	OTP_SW2_SEQ = 6b'000000
6	SW2IN	Leave floating	OTP_SW2_SEQ = 6b'000000
7	INTB_RSTB	Leave floating	
8	PGOOD	Leave floating	
9	XFAILB_FCCU	Leave floating	
10	SW2FB	Leave floating	OTP_SW2_SEQ = 6b'000000
11	GND	Connect to ground	
12	VIN	N/A	
13	LDO1IN	Leave floating	OTP_LDO1_SEQ = 6b'000000

Table 2. Unused pin termination*...continued*

Pin number	Pin name	Connection if not used	OTP considerations
14	LDO1OUT	Leave floating	OTP_LDO1_SEQ = 6b'000000
15	NC	Leave floating	
16	LDO2IN	Leave floating	OTP_LDO2_SEQ = 6b'000000
17	LDO2OUT	Leave floating	OTP_LDO2_SEQ = 6b'000000
18	GND	Connect to ground	
19	SW3LX	Leave floating	OTP_SW3_SEQ = 6b'000000
20	SW3IN	Leave floating	OTP_SW3_SEQ = 6b'000000
21	NC	Leave floating	
22	SYNC_STANDBY	Connect to ground	
23	VDDOTP	Connect to ground	
24	SW3FB3	Leave floating	OTP_SW3_SEQ = 6b'000000
25	GND	Connect to ground	
26	SW1FB	Leave floating	OTP_SW1_SEQ = 6b'000000
27	SCL	Leave Floating	
28	SDA	Leave Floating	

4 Application external components

4.1 VIN

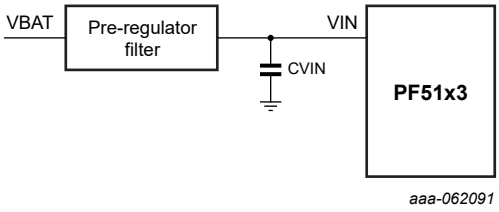


Figure 3. VIN

Table 3. VIN components

Components	Description
CVIN	Minimum 2.2 µF Voltage rating : 10 V minimum
Pre-regulator filter	Generally between 80 µF and 120 µF for the output capacitor depending on the pre-regulator part numbers chosen and filtering strategy (switching frequency, voltage at the output. and so on)

4.2 LVBUCK

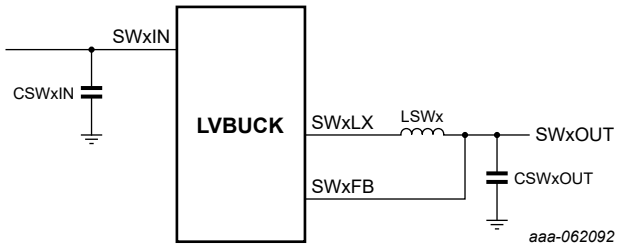


Figure 4. LVBUCK

Table 4. LVBUCK components

Components	Description
CSWxIN	Minimum 4.7 µF Voltage rating : 10 V minimum
LSWx	Case 1 : 470 nH minimum for switching frequency between 2 MHz and 3 Mhz Case 2 : 220 nH minimum for switching frequency between 3.6 MHz and 4.4 Mhz ***Note:*** *we can use a 470 nH inductance for case 2. It is completely operational, but we need to adapt the internal compensation network.*
CSWxOUT	Minimum 2 * 22 µF Voltage rating: 6.3 minimum. (Pay attention to the DC bias; the effective capacitance may change depending on the output voltage regulated.)

4.3 LDO

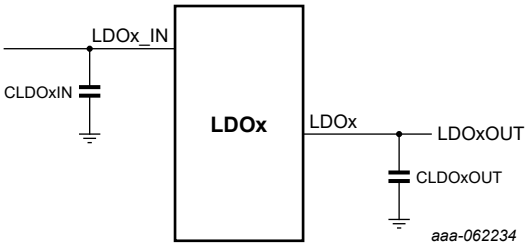


Figure 5. LDO

Table 5. LDO components

Components	Description
CLDOxIN	Minimum 1 µF Voltage rating : 10 V minimum
CLDOxOUT	Minimum 4.7 µF Voltage rating : 6.3 V minimum (Pay attention to the DC bias; the effective capacitance may change depending on the output voltage regulated)

4.4 Local I/O pins

4.4.1 PGOOD

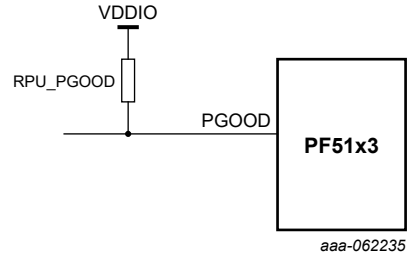


Figure 6. PGOOD

Table 6. PGOOD components

Components	Description
RPU_PGOOD	Pullup resistor, 5.1 kΩ

4.4.2 XFAILB_FCCU

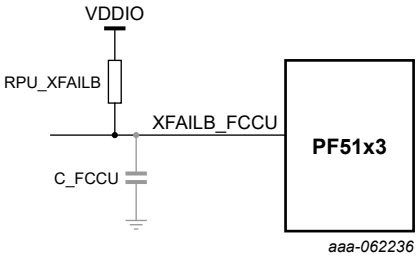


Figure 7. XFAILB_FCCU

Table 7. XFAILB_FCCU Components

Components	Description
RPU_XFAILB	Pull-up resistor, 5.1 kΩ
C_FCCU	Capacitor 1 nF, 6.3 V minimum To use only with FCCU mode enabled and XFAILB disabled. OTP setting: OTP_FCCU_EN = 1 OTP_XFAILB_EN = 0

4.4.3 INTB_RSTB

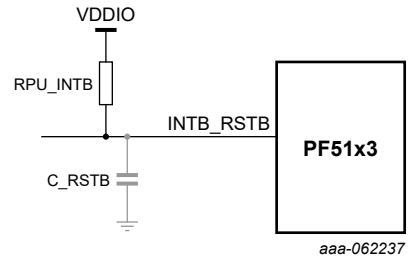


Figure 8. INTB_RSTB

Table 8. INTB_RSTB components

Components	Description
RPU_INTB	Pullup resistor, 5.1 kΩ
C_RSTB	Capacitor 1 nF, 6.3 V minimum To use only with RSTB mode enabled and INTB disabled. OTP setting: OTP_INTB_RSTB = 1

4.4.4 SYNC_STANDBY

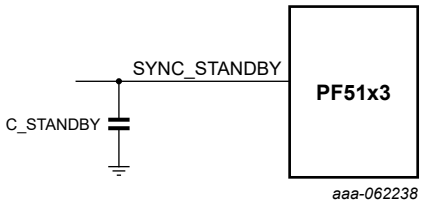


Figure 9. SYNC_STANDBY

Table 9. SYNC_STANDBY components

Components	Description
C_STANDBY	Capacitor 1 nF, 6.3 V minimum To use only with STANDBY mode enabled and SYNC mode disabled. OTP setting: OTP_SYNC_EN = 0 OTP_SYNC_STBY = 1

5 Hardware schematic

5.1 Schematic default configuration

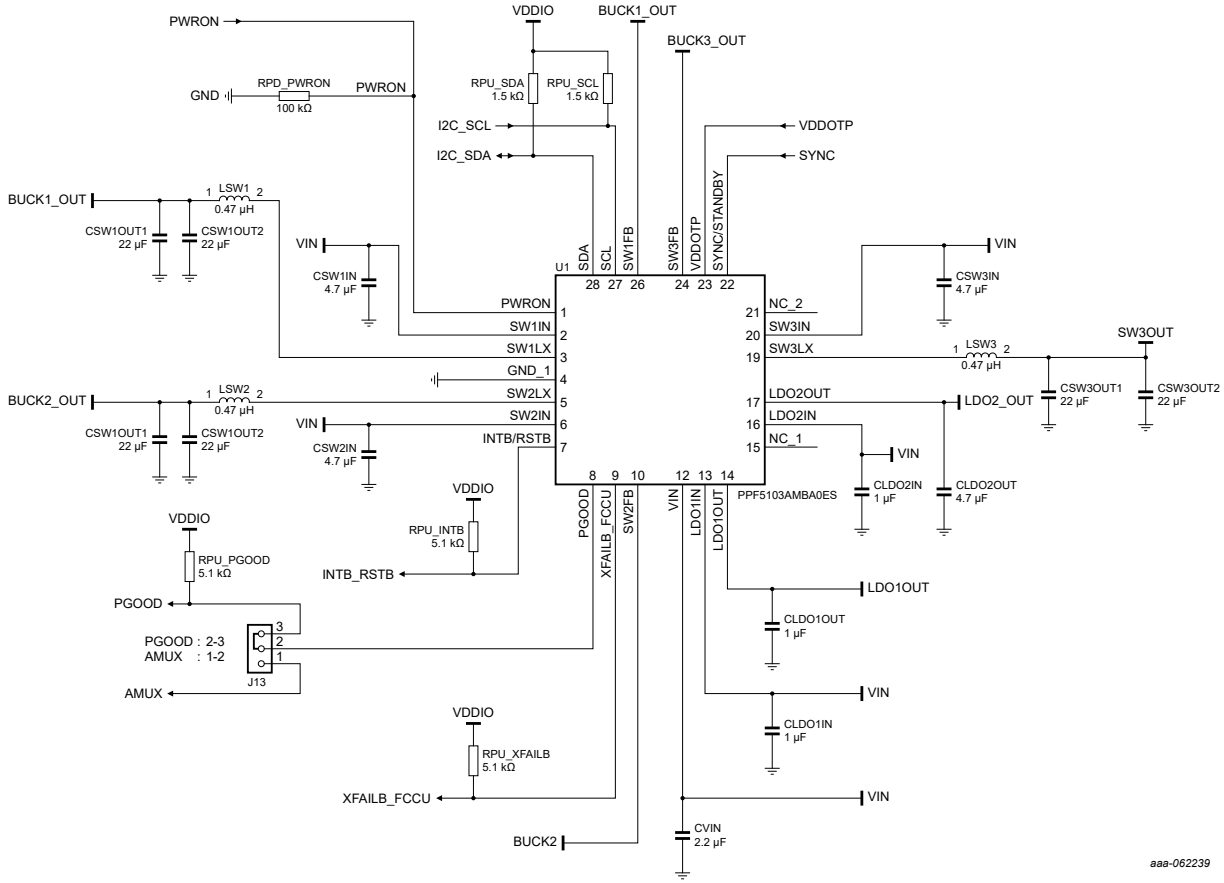


Figure 10. PF5103 PMIC schematic with default configuration

5.2 BOM default configuration – 4 MHz

Table 10. BOM for 4 MHz configuration

Reference	Quantity	Description	Manufacturer	Part number	Value
CLDO1IN,CLDO2IN	2	CAP CER 1uF 10V 10% X7S AEC-Q200 0402	MURATA	GCM155C71A105KE38D	1 µF
CSW1IN,CLDO1 OUT,CSW2IN,CLDO2 OUT,CSW3IN	5	CAP CER 4.7uF 16V 10% X7R AEC-Q200 0805	TDK	CGA4J3X7R1C475K125AB	4.7 µF
CSW1OUT1,CSW1 OUT2,CSW2 OUT1,CSW2 OUT2,CSW3 OUT1,CSW3OUT2	6	CAP CER 22uF 6.3V 20% X7T AEC-Q200 0805	TDK	CGA4J1X7T0J226M125AC	22 µF
CVIN	1	CAP CER 2.2uF 10V 10% X7S AEC-Q200 0603	TDK	CGA3E3X7S1A225K080AB	2.2 µF
LSW1,LSW2,LSW3	3	IND PWR 0.22uH@1 MHZ 8A 20% AEC-Q200 SMD	TDK	TFM252012ALMAR22MTAA	0.22 µH
RPD_PWRON	1	RES MF 100K 1/16W 5% 100ppm/C 0402	YAGEO	RC0402JR-07100KL	100 KΩ
RPU_INTB	1	RES TF 5.1K 1/4W 5% AEC-Q200 0603	ROHM	ESR03EZPJ512	5.1 KΩ
RPU_XFAILB,RPU_ PGOOD	2	RES MF 5.1K 1/10W 1% AEC-Q200 0402	KOA SPEER	RK73H1ETTP5101F	5.1 KΩ
RPU_SDA,RPU_SCL	2	RES MF 1.50K 1/16W 1% AEC-Q200 0402	VISHAY	CRCW04021K50FKED	1.5 KΩ
U1	1	IC POWER MAN AGEMENT 2.7-5.5V FCQFN28	NXP	PPF5103AMBA0ES	PPF5103 AMBA0ES

5.3 BOM default configuration – 2.5 MHz

Table 11. BOM for 2.5 MHz configuration

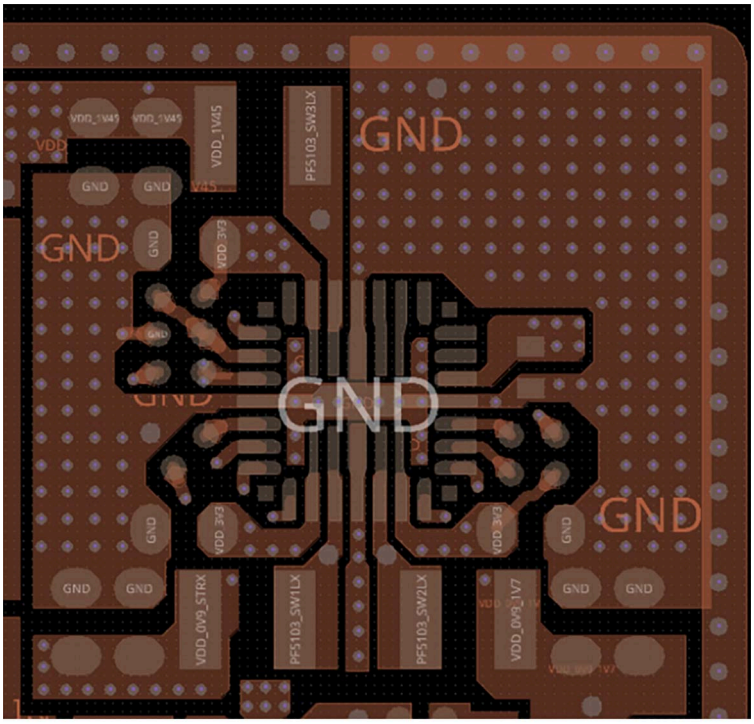
Reference	Quantity	Description	Manufacturer	Part Number	Value
CLDO1IN,CLDO2IN	2	CAP CER 1uF 10V 10% X7S AEC-Q200 0402	MURATA	GCM155C71A105KE38D	1 µF
CSW1IN,CLDO1 OUT,CSW2IN,CLDO2 OUT,CSW3IN	5	CAP CER 4.7uF 16V 10% X7R AEC-Q200 0805	TDK	CGA4J3X7R1C475K125AB	4.7 µF
CSW1OUT1,CSW1 OUT2,CSW2 OUT1,CSW2 OUT2,CSW3 OUT1,CSW3OUT2	6	CAP CER 22uF 6.3V 20% X7T AEC-Q200 0805	TDK	CGA4J1X7T0J226M125AC	22 µF
CVIN	1	CAP CER 2.2uF 10V 10% X7S AEC-Q200 0603	TDK	CGA3E3X7S1A225K080AB	2.2 µF
LSW1,LSW2,LSW3	3	IND PWR 0.47uH@1 MHz 5.8A 20% AEC-Q200 SMT	TDK	TFM252012ALMAR47MTAA	0.22 µH
RPD_PWRON	1	RES MF 100K 1/16W 5% 100ppm/C 0402	YAGEO	RC0402JR-07100KL	100 KΩ
RPU_INTB	1	RES TF 5.1K 1/4W 5% AEC-Q200 0603	ROHM	ESR03EZPJ512	5.1 KΩ
RPU_XFAILB,RPU_ PGOOD	2	RES MF 5.1K 1/10W 1% AEC-Q200 0402	KOA SPEER	RK73H1ETTP5101F	5.1 KΩ
RPU_SDA,RPU_SCL	2	RES MF 1.50K 1/16W 1% AEC-Q200 0402	VISHAY	CRCW04021K50FKED	1.5 KΩ
U1	1	IC POWER MAN AGEMENT 2.7-5.5V FCQFN28	NXP	PPF5103AMBA0ES	PPF5103 AMBA0ES

6 Layout recommendations

General layout advice:

- Route SW1FB-SW3FB away from noisy planes, shielded if necessary. Ensure the adjacent layers are SWx current loops, as small as possible with wide tracks.
- Avoid noise-sensitive signals below switch mode power supply (SMPS) power components.
- Place CVIN, CSWxIN, and CLDOxIN capacitors close to the IC, with a via on the ground side of each capacitor.
- The PF51 is a QFN 28-pin package with an exposed pad (EPAD) for enhanced thermal dissipation. Put at least five ground vias, in a cross shape, on the EPAD to the bottom layer ground island.
- NXP recommends using at least 2 oz. copper layer thickness on the outer layers to improve thermal dissipation.

See Figure 11 for an example of a top layer implementation.



aaa-062240

Figure 11. Example of top layer implementation

7 Engineering modes

Here is a summary of engineering mode descriptions with conditions to reach them:

Table 12. PF51x3 Engineering modes

Engineering modes	Normal mode	Debug mode	Test mode	Programming mode
VDDOTP voltage	VDDOTP = GND	VDDOTP > 1.4 V	VDDOTP > 1.4 V	VDDOTP = 8 V
PWRON state	PWRON = HIGH	PWRON = HIGH	PWRON = GND	PWRON = GND
State machine	Run mode Standby mode I/O Release	Run mode Standby mode I/O Release	LP_OFF	LP_OFF
Features of the mode	All features enabled	• No CRC • I²C address shall be 0x08 • Secure write disabled • Watchdog disabled	• All regulators OFF • Access to the mirrors registers (OTP registers)	Burn a permanent OTP configuration

See Figure 12 for an illustration with waveforms.

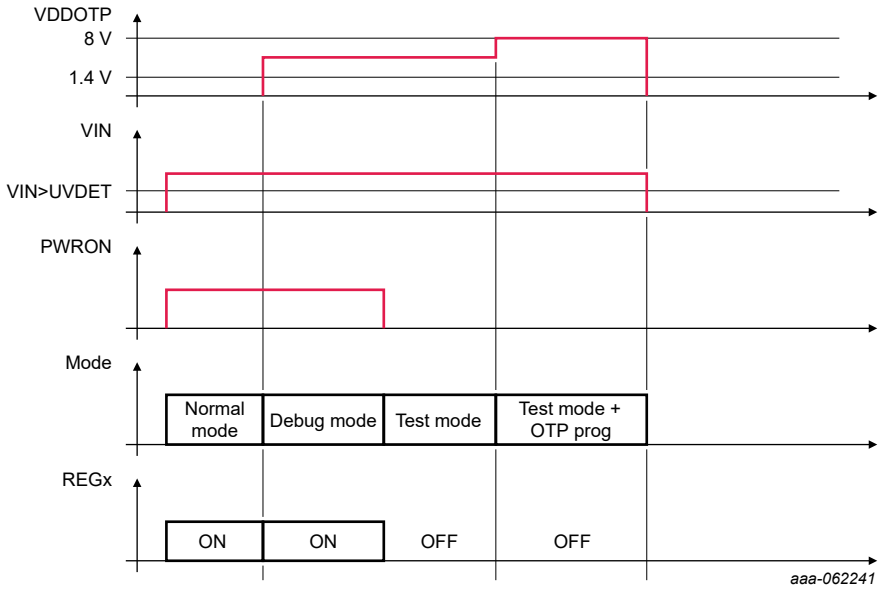


Figure 12. PF51x3 Engineering modes with waveforms

8 Operating modes

8.1 State machine

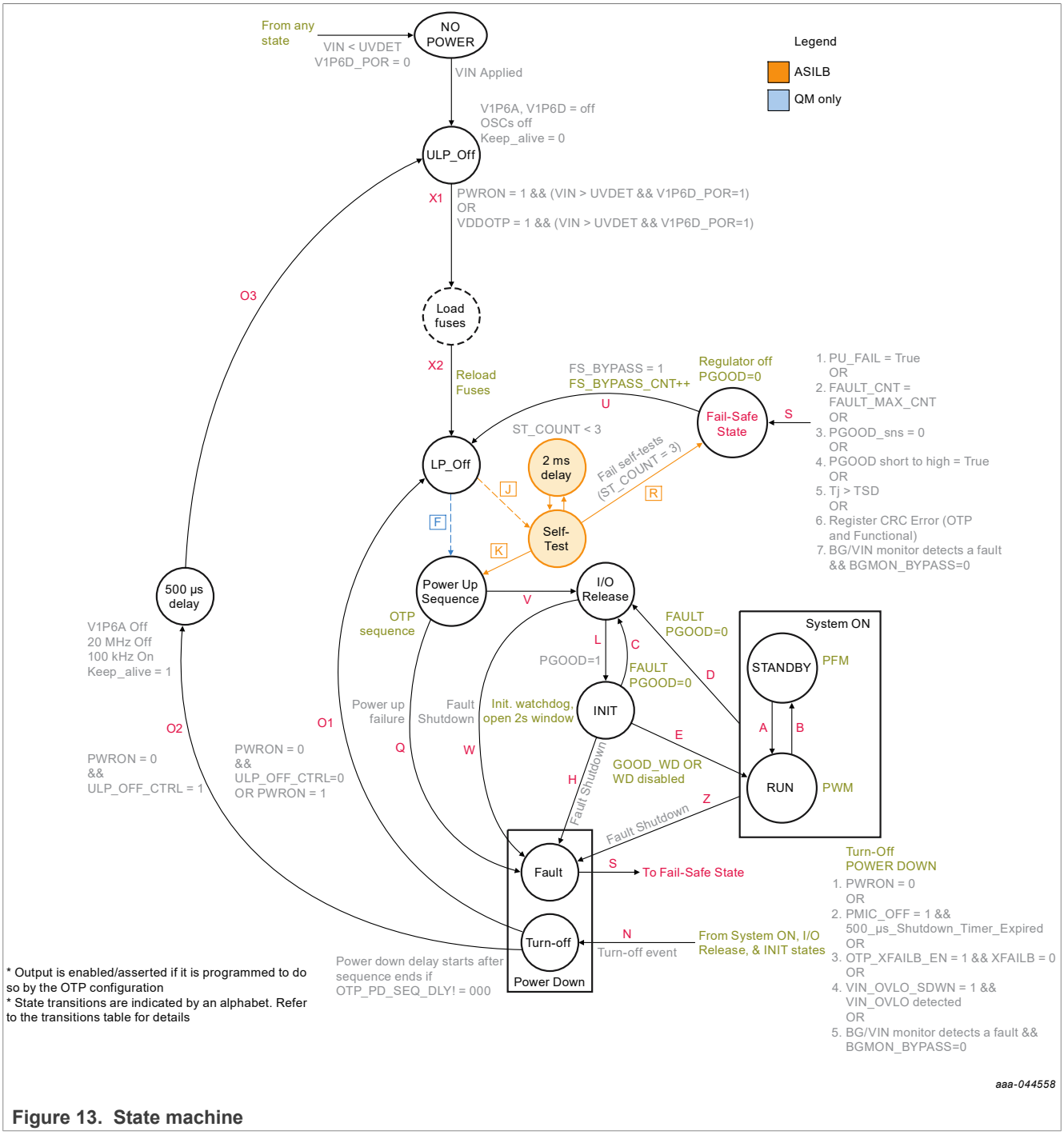


Figure 13. State machine

8.2 Run mode/Standby mode

Table 13 lists some of the characteristics of Run and Standby modes.

Table 13. Run and Standby mode specifications

Mode characteristics	Run mode	Standby mode
Buck switching strategy	PWM	PFM
Current range	Iout > 100 mA (up to 3.5 A by phase)	Iout ≤ 100 mA
OTP settings	OTP_SYNC_STBY = 0	OTP_SYNC_STBY = 1

Figure 14 illustrates the two modes.

Figure 14. Waveform views of Run (PWM) and Standby (PFM) modes

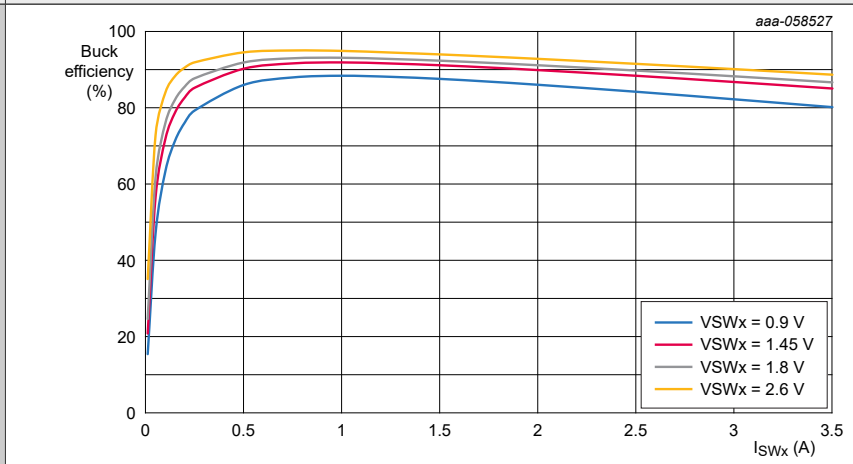
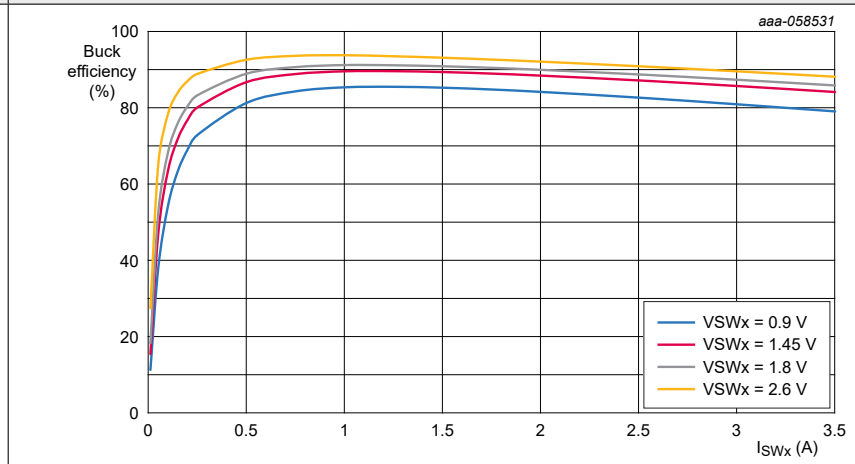
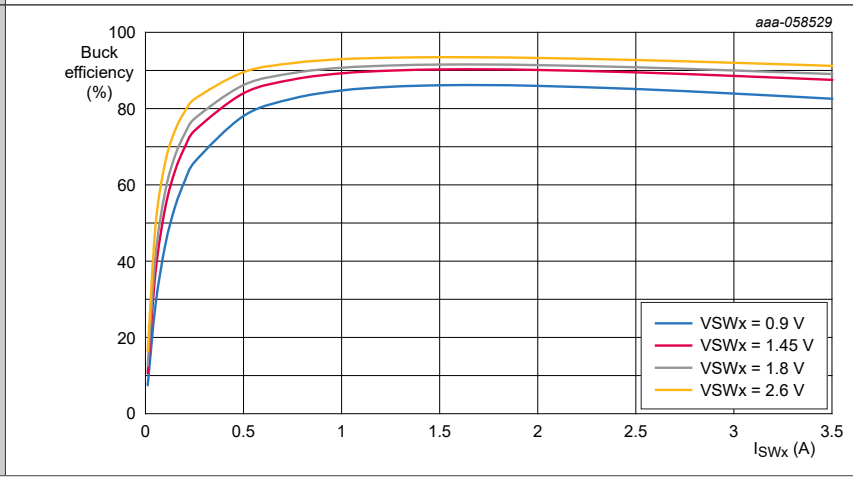
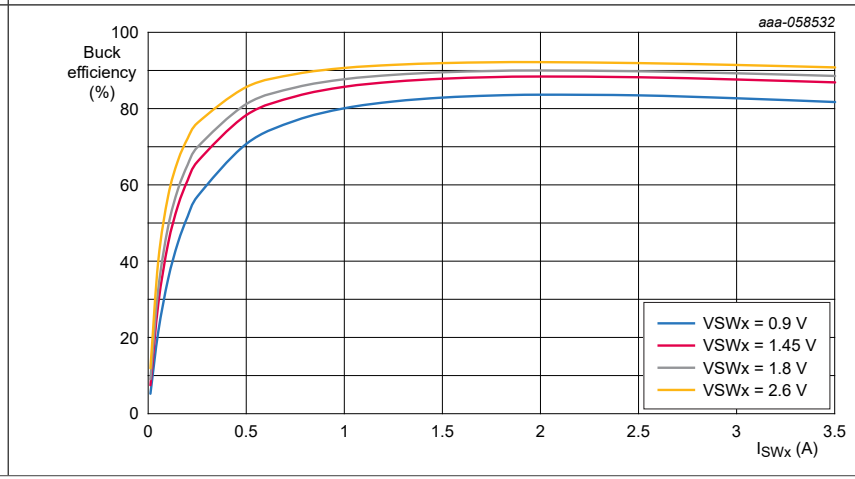
Note: *The OTP bits OTP_SYNC_STBY define the mode where the PMIC will start, but the mode may be changed using I^2C at any time by writing to functional registers.*

9 Performance

9.1 Efficiency

Here is a summary of PF51x3 efficiency performance with the reference BOM:

Table 14. Buck efficiency vs. I_{SWx} at ambient temperature T_a = 25 ℃

	2.22 MHz	4 MHz
Vin = 3.3 V		
Vin = 5 V		

9.2 Stability

Table 15 has the recommended values to set when creating the OTP to optimize stability performance :

Table 15. Recommended compensation network settings

Recommended compensation network values	Fsw = 4 MHz (L = 220 nH)	Fsw = 2.5 MHz (L = 470 nH)	Fsw = 4 MHz (L = 470 nH)
0.5 V – 1.35 V	GM_COMP = 70 µS R_COMP = 40 kΩ C_COMP = 100 pF	GM_COMP = 70 µS R_COMP = 40 kΩ C_COMP = 100 pF	GM_COMP = 53 µS R_COMP = 80 kΩ C_COMP = 100 pF
1.45 V – 2.5 V	GM_COMP = 88 µS R_COMP = 80 kΩ C_COMP = 100 pF	GM_COMP = 35 µS R_COMP = 80 kΩ C_COMP = 100 pF	GM_COMP=70 µS R_COMP = 80 kΩ C_COMP = 100 pF
2.6 V – 3.3 V	GM_COMP = 70 µS R_COMP = 80 kΩ C_COMP = 100 pF	GM_COMP = 53 µS R_COMP = 80 kΩ C_COMP = 100 pF	GM_COMP = 88 µS R_COMP = 80 kΩ C_COMP = 100 pF

Table 16 is analogous to Table 15, but with OTP settings.

Table 16. Recommended compensation network OTP settings

Recommended compensation network OTP settings	Fsw = 4 MHz (L =220 nH)	Fsw = 2.5 MHz (L = 470 nH)	Fsw = 4 MHz (L = 470 nH)
0.5 V – 1.35 V	OTP_SWx_GM_COMP = 011 OTP_SWx_R_COMP = 00 OTP_SWx_C_COMP = 11	OTP_SWx_GM_COMP = 011 OTP_SWx_R_COMP = 00 OTP_SWx_C_COMP = 11	OTP_SWx_GM_COMP = 010 OTP_SWx_R_COMP = 01 OTP_SWx_C_COMP = 11
1.45 V – 2.5 V	OTP_SWx_GM_COMP = 100 OTP_SWx_R_COMP = 01 OTP_SWx_C_COMP = 11	OTP_SWx_GM_COMP = 001 OTP_SWx_R_COMP = 01 OTP_SWx_C_COMP = 11	OTP_SWx_GM_COMP = 011 OTP_SWx_R_COMP = 01 OTP_SWx_C_COMP = 11
2.6 V – 3.3 V	OTP_SWx_GM_COMP = 011 OTP_SWx_R_COMP = 01 OTP_SWx_C_COMP = 11	OTP_SWx_GM_COMP = 010 OTP_SWx_R_COMP = 01 OTP_SWx_C_COMP = 11	OTP_SWx_GM_COMP = 100 OTP_SWx_R_COMP = 01 OTP_SWx_C_COMP = 11

Note: *The values are provided for specific use cases at Vin = 3.3 V. For other switching frequencies or passive output components that differ from the BOM, re-evaluate these settings to find the best compromise between phase margin, gain margin, and bandwidth.*

9.2.1 Use case 1 : FSW = 2.22 Mhz, SWxOUT = 1.8 V, VIN = 3.3 V

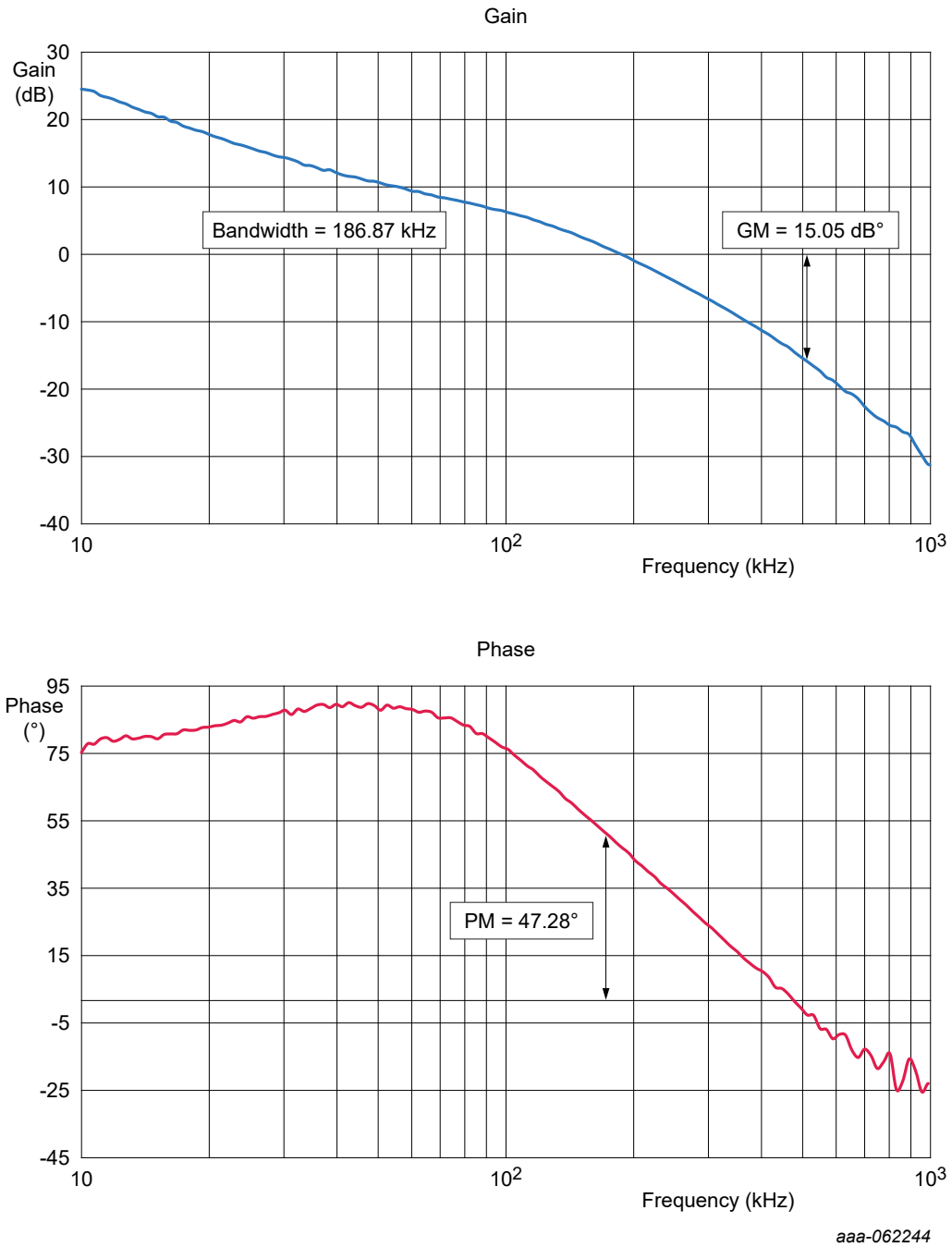


Figure 15. Use case 1

Phase margin	Gain margin	Bandwidth
47.28 °	15.05 dB	186.87 kHz

9.2.2 Use case 2 : FSW = 4 Mhz, SWxOUT = 1.8 V, VIN = 3.3 V

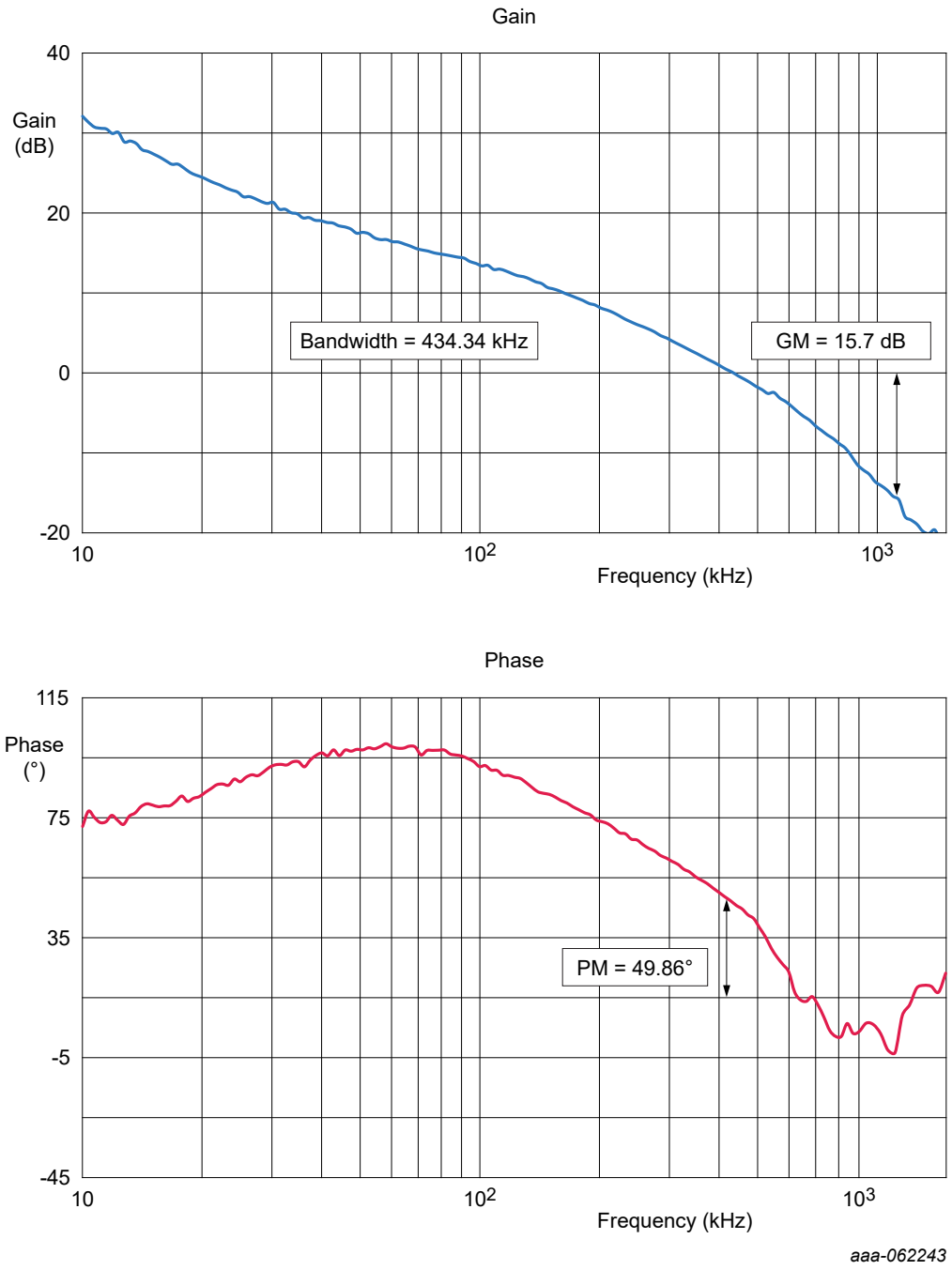


Figure 16. Use case 2

Phase margin	Gain margin	Bandwidth
49.86 °	15.7 dB	434.34 KHz

10 I²C communication

Communication with the PF5103 is done through I^{2}C, supporting high-speed operation mode up to 3.4 MHz. . SDA and SCL are pulled up externally to 1.8 V or 3.3 V with 1.5 kΩ resistors to support this high-speed operation. To use the high-speed operation mode, a suitable pullup resistor must be used in the range of 500 Ω to 1k Ω. The PF5103 is designed to operate as a companion device during I^{2}C communication. The default I^{2}C device address is set using OTP_I2C_ADD[2:0].

Table 17. PF51x3 I²C address configuration

OTP_I2C_ADD[2:0]	8-bit write address
000	0x08
001	0x09
010	0x0A
011	0x0B
100	0x0C
101	0x0D
110	0x0E
111	0x0F

See https://www.nxp.com/docs/en/user-guide/UM10204.pdf for detailed information on the digital IC communication protocol implementation. During an I^{2}C transaction, the communication will latch after the 8th bit sent. If the data sent is not a multiple of 8 bits, any word with less than 8 bits will be ignored. If only 7 bits are sent, no data is written and the logic will not provide an ACK bit to the MCU.

At an IC level, an incorrect I^{2}C command can create a system-level safety issue. For example, though the processor may have intended to set a given regulator's output to 1.0 V, it may be erroneously registered as 1.1 V due to noise in the bus. To prevent an incorrect I^{2}C configuration, various protective mechanisms are implemented.

10.1 I²C write frame

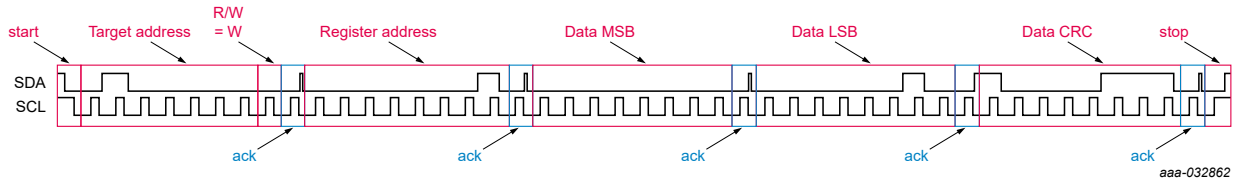


Figure 17. I²C frame example, write data

If the CRC is not enabled in OTP, the data CRC byte is not required.

10.2 I²C read frame

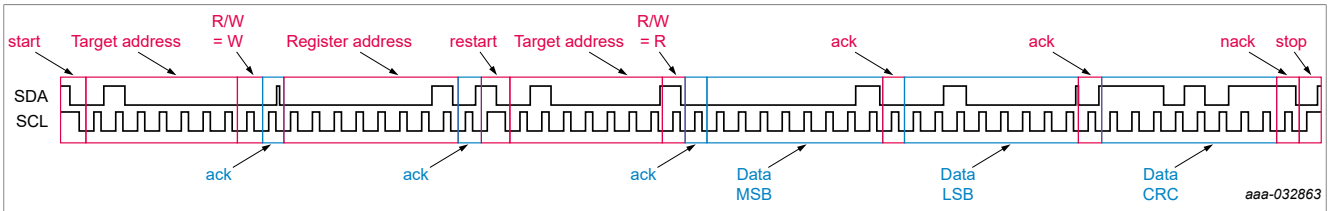


Figure 18. I²C frame example, read data

First perform an I^{2}C write access to configure the register address to read, then perform an I^{2}C read access to get data and CRC.

If the CRC is not enabled on OTP, the data CRC byte does not exist.

10.3 I²C CRC verification

When this feature is enabled, a selectable CRC verification is performed on each I^{2}C transaction.

- When OTP_I2C_CRC_EN = 0, the CRC verification mechanism is disabled.
- When OTP_I2C_CRC_EN = 1, the CRC verification mechanism is enabled.

After each I^{2}C transaction, the device calculates the corresponding CRC byte to ensure the configuration command has not been corrupted.

When a CRC fault is detected, the PF5103 ignores the erroneous configuration command and triggers a CRC_I interrupt, asserting the INTB pin, provided the interrupt is not masked.

The PF5103 implements a CRC-8-SAE, per the SAE J1850 specification.

- Polynomial = 0x11D
- Initial value = 0XFF

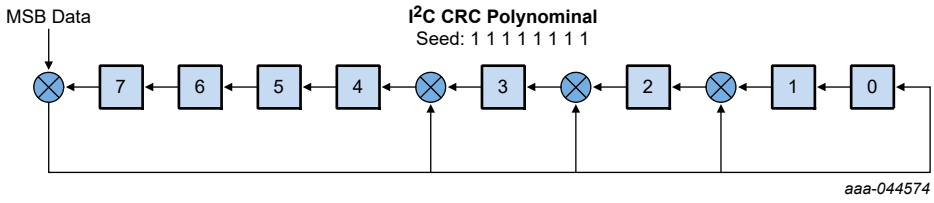


Figure 19. 8 bit SAE J1850 CRC polynomial

11 Acronyms and abbreviations

Table 18. Acronyms and abbreviations

Acronym	Description
ABIST	analog built-in self test
ADAS	advanced driver assistance systems
ASIL	automotive safety integrity level
BOM	bill of materials
CRC	cyclic redundancy check
FCCU	fault collection and control unit
I²C	inter-integrated circuit
MCU	microcontroller Unit
OTP	one time programmable
PFM	pulse-frequency modulation
PMIC	power management integrated circuit
PWM	pulse-width modulation
SMPS	switch mode power supply

12 References

1. UM10204 — I^2C-bus specification and user manual (https://www.nxp.com/docs/en/user-guide/UM10204.pdf)
2. PF51x3 data sheet — (https://www.nxp.com/products/PF51x3)

13 Revision history

Table 19. Revision history

Document ID	Release date	Description
AN14790 v. 1.0	9 April 2026	• Changed classification from confidential to public • Updated References to point to public data sheet
AN14790 v. 0.1	5 December 2025	Initial version

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Tables

Figures

Contents