AN14765

Low-Power Implementation on MCXA345 and MCXA346

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Document information

Information	Content
Keywords	AN14765, MCXA, MCXA345, MCXA346, low power, power consumption, wake-up time
Abstract	This application note introduces the power domains, power modes, highlight configurations, and low-power and wake-up optimization of MCXA345 and MCXA346. It provides different low-power and wake-up configurations through a demo for user reference.

1 Introduction

The MCXA345 and MCXA346 microcontrollers, featuring an Arm Cortex-M33, supports running up to 180 MHz, 1 MB of flash and 256 kB RAM. The MCXA345 and MCXA346 targets motor control applications optimized with high performance and MAU engine, integrated 2x FlexPWM with 4x submodule combined with AOI, up to 4x ADC, and rich serial peripheral and SmartDMA.

The power-efficient operating modes are as follows:

- 78 µA/MHz in the Active mode
- 0.579 mA in the Sleep mode
- 96.02 µA in the Deep Sleep mode
- 31.95 µA in the Power Down mode
- 473 nA in the Deep Power Down mode

This application note describes the following contents of the MCXA345 and MCXA346:

- Power domains and power supplies
- Power modes and low-power entry
- Power-related configurations
- Wake-up source and wake-up time
- Low power and wake-up optimization
- Low power demo

2 Power domains

As shown in Figure 1, the device contains the following power domains:

- SYSTEM
- CORE
- SRAM
- ANALOG

For specific modules contained in each domain, see the power domain assignments for modules table in the *MCX A345 and MCX A346 Reference Manual* (document MCXAP144M240F60RM).

- The SYSTEM domain is for power management, which contains SPC, HVD/LVD/POR, FRO16K, WUU, and other modules.
- The CORE domain is for digital logic, which contains CM33, NVIC, DMA, FRO180M, LPUART, GPIO, and other modules.

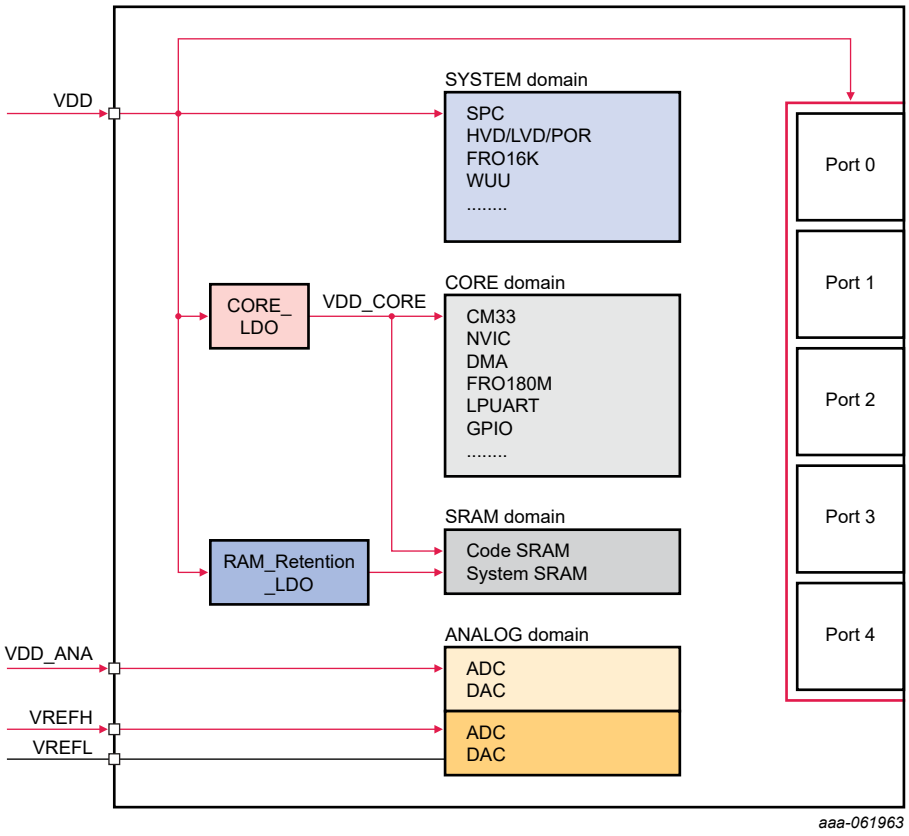

Figure 1. Power domains and power supplies

Table 1 lists the power supply and corresponding voltage range of each power domain. The power supply of the CORE domain is the output voltage VDD_CORE of CORE_LDO. In Active mode, VDD_CORE operates at 1.0 V and 1.2 V while in Power Down mode, it can operate at a lower voltage. When VDD_CORE is 1.2 V, the core can reach up to 180 MHz. When VDD_CORE is 1.0 V, the core can reach up to 45 MHz. The power supply of the SRAM domain is the output voltage of CORE_LDO or RAM_Retention_LDO. RAM_Retention_LDO supports SRAM retention switches in the Deep Power Down mode. For the power supply and corresponding voltage range of the remaining power domains, see Table 1.

Table 1. Power supplies and voltage range

Power domain	Power supply	Voltage range
CORE	LDO_CORE	Mid voltage (1.0 V), Overdrive voltage (1.2 V) (Active, Sleep, and Deep Sleep mode)
		Retention voltage (Power Down mode)
		OFF (Deep Power Down mode)
SRAM	LDO_CORE	Mid voltage (1.0 V), Overdrive voltage (1.2 V) (Active and Sleep mode)
	RAM_Retention_LDO	Retention voltage (Deep Sleep, Power Down, and Deep Power Down mode)
SYSTEM	VDD	1.71 V - 3.6 V
ANALOG	VDD_ANA	1.61 V - 3.7 V

3 Power modes and low power entry

This section describes power modes and low power entry controllers.

3.1 Power modes

The device supports Active, Sleep, Deep Sleep, Power Down, and Deep Power Down. Table 2 describes the status of Clock, CORE domain, SYSTEM domain, FLASH, SRAM, PORT, and IO in different power modes. It also helps users compare the status of these modules in different power modes. Users can easily find the status of these modules in a certain power mode. Figure 2 shows the clock/LP peripheral/IO differences in Deep Sleep and Power Down mode.

Table 2. Modules status and power modes

Mode Name	CORE domain	CM33	SYSTEM domain	Flash	SRAM	PORT[1]	IO
Active	ON	ON	ON	ON	ON	ON	ON
Sleep	ON	Static[2]	ON	ON	ON	ON	ON
Deep Sleep	Static/LP[3]	Static	ON	Static	Static	Static	ON[4]
Power Down	Static	Static	ON	OFF	Static/OFF	Static	Static
Deep Power Down	OFF[5]	OFF	ON	OFF	Static/OFF	OFF	Static

[1] PORT supports pad control functions.
[2] Static means that the module is in the state retention status (no clock but the data can be kept).
[3] LP means can be active with an async functional clock.
[4] This ON means that pinmux function can work normally in Deep Sleep mode. For example, CTimer outputs PWM through an IO in Active mode and can continue to output PWM in Deep Sleep mode.
[5] OFF means power down.

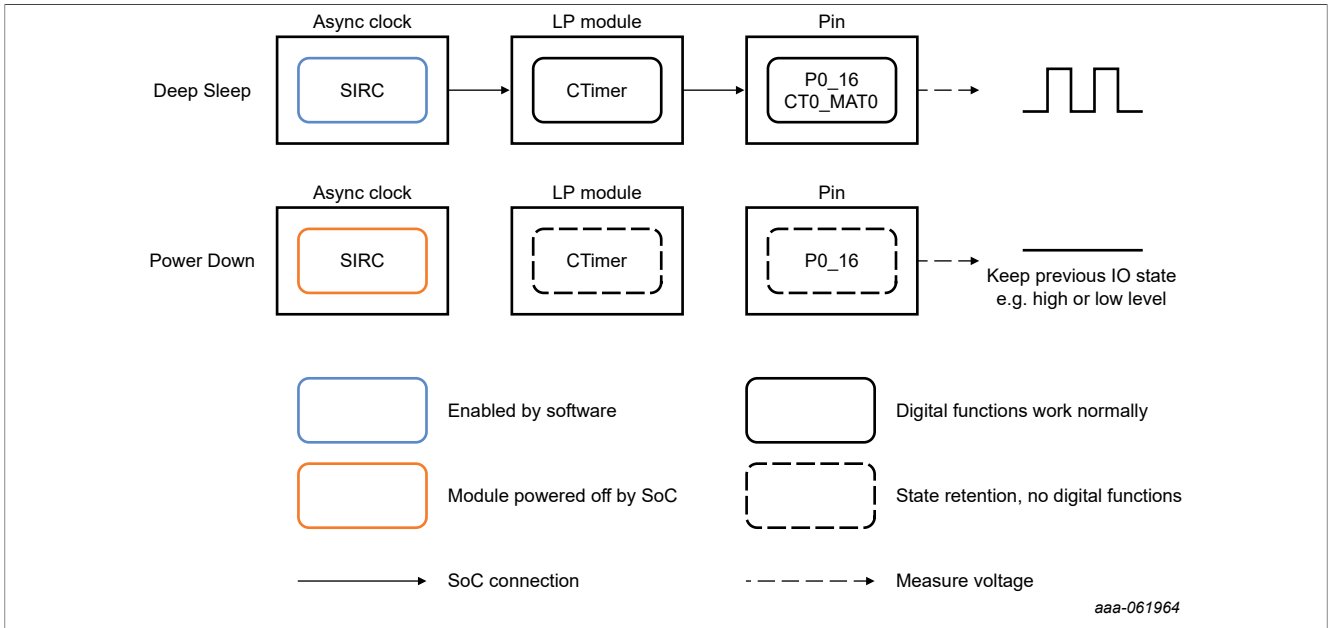

Figure 2. Differences in Deep Sleep and Power Down mode

IO state in power mode transition:

- Active → Power Down/Deep Power Down: IO state can be kept.

- Power Down → Active: IO state can be kept but not isolated. ISO_CLR=0; IO output can be configured.
- Deep Power Down → Active: IO state can be kept and is isolated. ISO_CLR=1; to configure IO, first write ISO_CLR.

The following sections introduce the features of different power modes.

3.1.1 Active

Active mode is the default mode after Reset operation. In this mode:

- Clocks to CPU, memories, and peripherals are enabled.
- CPU execution is possible.
- VDD_CORE is adjusted to the minimum possible value based on the required frequency to achieve optimal power consumption.

3.1.2 Sleep

The salient characteristics of Sleep mode are as follows:

- The CPU clock is disabled.
- The System and Bus clock remain enabled.
- Most modules can remain operational.
- ACTIVE_CFG register is used to control LDO_CORE voltage level and drive strength.

3.1.3 Deep Sleep

The salient characteristics of Deep Sleep mode are as follows:

- CPU clock, System clock, and Bus clock are disabled.
- SRAM is in static status (SRAM cannot be accessed, but the data is retained).
- To enable SOSC, SIRC, and FIRC, configure the corresponding STEN bit.
- Some modules can remain operational with low-power asynchronous clock sources.

3.1.4 Power Down

It is the lowest power mode that can retain all registers. The salient characteristics of Power Down mode are as follows:

- The CPU clock, System clock, and Bus clock are disabled.
- Flash memory is powered off.
- Place the CORE domain of the chip into the static state.
- Supports four SRAM retention switches and must retain at least one SRAM array. For details, refer to the on-chip regulators table in section "System Power Control (SPC)" of the *MCXA345/346 Reference Manual* (document MCXAP144M240F60RM).
- Configure the SPC LP_CFG[CORELDO_VDD_LVL] to 0000b (retention voltage).

3.1.5 Deep Power Down

The device wakes from Deep Power Down mode through the Reset routine. The salient characteristics of Deep Power Down mode:

- The CPU clock, System clock, and Bus clock are disabled.
- The flash memory is powered off.
- The CORE domain is powered off.

- The SYSTEM domain remains enabled.

This mode supports four SRAM retention switches and all SRAM arrays powered off. For details, refer to the on-chip regulators table in section "System Power Control (SPC)" of the *MCXA345/346 Reference Manual* (document MCXAP144M240F60RM).

3.2 Low power entry

The bit fields CKCTRL[CKMODE] and PMCTRLMAIN[LPMODE] control the power mode entry as shown in Table 5. The CKCTRL[CKMODE] field configures the amount of clock gating when the core enters a low power mode because of WFI or WFE.

Table 3 shows the functions corresponding to different CKMODE values.

- Configuring CKMODE greater than 0 requires the SLEEPDEEP field in the Arm core to become 1.
- Configuring PMCTRLMAIN[LPMODE] greater than 0 requires writing 1111b to CKMODE.

Table 3. Function of CKMODE field

CKCTRL[CKMODE]	Function
0000b	No clock gating
0001b	Core clock gated
1111b	Core, platform, and peripheral clocks are gated, and the core enters the low power mode

PMCTRLMAIN[LPMODE] selects the desired low power mode when a core executes a WFI or WFE instruction. If the protection level is not enabled using power mode protection (PMPROT), writes to this field are blocked.

Table 4 shows the functions corresponding to different LPMODE values.

Table 4. Function of the LPMODE bit field

PMCTRLMAIN[LPMODE]	Function
0000b	Active/Sleep
0001b	Deep Sleep
0011b	Power Down
1111b	Deep Power Down

Table 5 shows all the configurations of the device to enter the low power mode.

Table 5. Power mode entry

Power mode	CKCTRL[CKMODE]	PMPROT[LPMODE]	PMCTRLMAIN[LPMODE]
Active	0000b	0000b	0000b
Sleep	0000b	0000b	0000b
	0001b		
Deep Sleep	1111b	0001b	0001b
Power Down	1111b	0011b	0011b
Deep Power Down	1111b	1111b	1111b

4 Power configurations

This section describes the regulator and voltage detector configurations, low-power request (LPREQ) pin, and async DMA.

4.1 Regulator and voltage detectors configurations

Table 6 shows the power-related hardware configurations. ACTIVE_CFG and ACTIVE_CFG1 registers configure the hardware in Active mode and Sleep mode, such as LDO_CORE voltage level and drive strength.

Autonomous change to use LP_CFG and LP_CFG1 when in low power mode (Deep Sleep, Power Down, and Deep Power Down).

Table 6. Power-related hardware configurations

Register name	Function
ACTIVE_CFG LP_CFG	• Configures: – LDO_CORE voltage level – LDO_CORE drive strength • Enables: – HVDs, LVDs – Band gap, BG buffer – VDD voltage detect – Low-power current reference IREF
ACTIVE_CFG1 LP_CFG1	• Enables: – Analog modules (CMPs, CMP DACs, OPAMPs, and DAC)

4.2 LPREQ pin

The LPREQ pin asserts after low power entry and negates after low power wake-up.

SPC controls the state of the LPREQ pin according to the configuration specified in the low-power request configuration (LPREQ_CFG) register. You control the LPREQ pin in Active mode. SPC controls the pin when the chip transitions from Active to a low power mode, and after wake-up from these low power modes.

To use the LPREQ pin, perform the following steps:

1. Specify the pin polarity (LPREQ_CFG[LPREQPOL])
2. Enable the pin output (LPREQ_CFG[LPREQOE])
3. Configure the pin mux for the desired pin using the PORT PCR registers.

Figure 3 shows the waveform of the LPREQ pin, where the explanation of the waveform is listed below:

- TIMER_MATCH: Hardware toggles IO to indicate the wake-up event.
- LPREQ_PIN: LPREQ_CFG[LPREQPOL] = 1b, [LPREQOE] = 1b, which means that the pin becomes low after low power entry and high after wake-up.

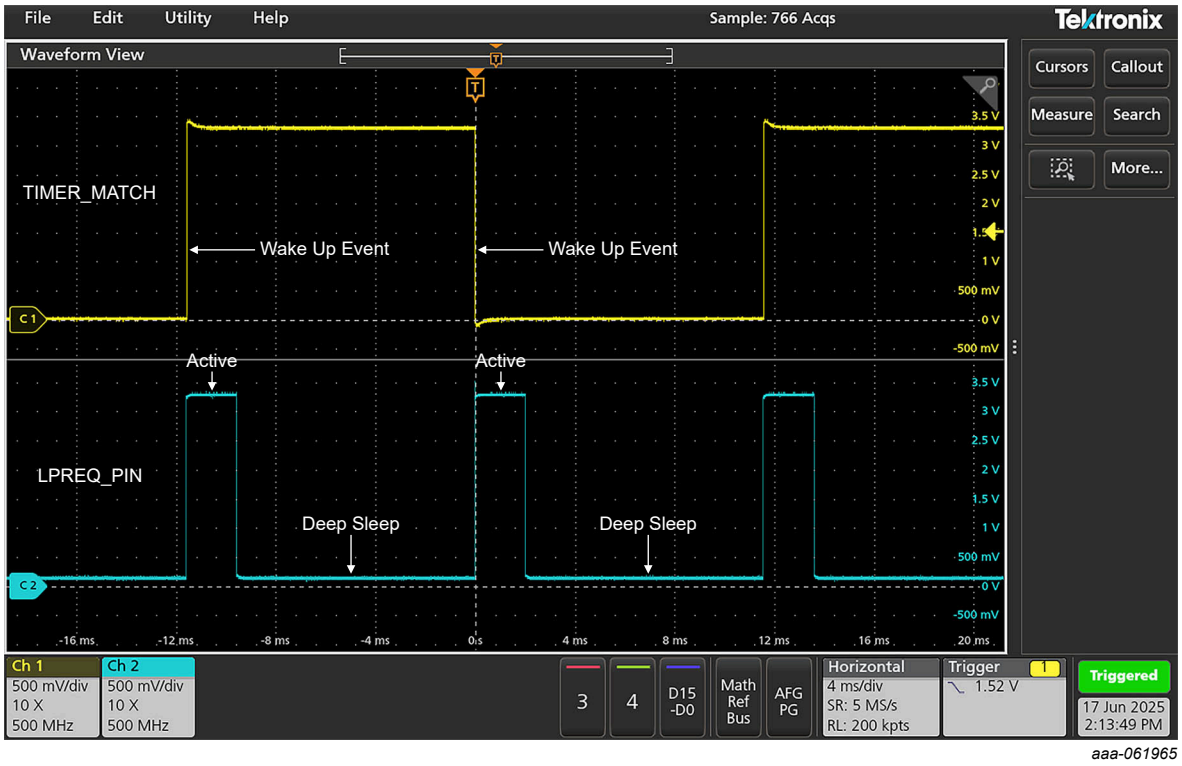

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Figure 3. Waveform of LPREQ pin

4.3 Async DMA

Deep Sleep mode and Power Down mode support the use of async DMA to wake up partially. The device automatically re-enters the low power mode after DMA completes its task.

Async DMA can be introduced as follows:

- Async DMA does not require CPU involvement. However, it still requires the bus clock, which wakes up the MCU from Deep Sleep or Power Down to Sleep mode.
- When async DMA must access the register of a peripheral, enable the Bus clock of the peripheral before entering low power mode by using the MRCC_GLB_CCx and MRCC_GLB_ACCx registers. When async DMA must access SRAM, the SRAM must not be set to retention state in Sleep mode.
- When async DMA is completed, that is, CHx_CSR[DONE] is set, the MCU automatically enters the original low power mode.
- Set CHx_CSR[ERQ] and CHx_CSR[EARQ].
- Table 7 lists all the hardware trigger sources of async DMA and the corresponding slot number. Only modules in LP status (not static status under Deep Sleep or Power Down modes) support async DMA. For example, FlexCAN is in static under Deep Sleep mode. Therefore, it cannot support async DMA.

Table 7. Async DMA configuration

Slot number	DMA request description	Module name
1	Wake up event	WUU0
3	Receive request	LPI2C2
4	Transmit request	LPI2C2
5	Receive request	LPI2C3

Table 7. Async DMA configuration*...continued*

Slot number	DMA request description	Module name
6	Transmit request	LPI2C3
11	Receive request	LPI2C0
12	Transmit request	LPI2C0
13	Receive request	LPI2C1
14	Transmit request	LPI2C1
15	Receive request	LPSPI0
16	Transmit request	LPSPI0
17	Receive request	LPSPI1
18	Transmit request	LPSPI1
21	Receive request	LPUART0
22	Transmit request	LPUART0
23	Receive request	LPUART1
24	Transmit request	LPUART1
25	Receive request	LPUART2
26	Transmit request	LPUART2
27	Receive request	LPUART3
28	Transmit request	LPUART3
29	Receive request	LPUART4
30	Transmit request	LPUART4
49	Counter match event	LPTMR0
51	FIFO request	ADC0
52	FIFO request	ADC1
53	DMA request	CMP0
54	DMA request	CMP1
55	DMA request	CMP2
56	FIFO request	DAC0
60	Pin event request 0	GPIO0
61	Pin event request 0	GPIO1
62	Pin event request 0	GPIO2
63	Pin event request 0	GPIO3
64	Pin event request 0	GPIO4
71	Shift Register 0 request	FlexIO0
72	Shift Register 1 request	FlexIO0
72	Shift Register 2 request	FlexIO0
74	Shift Register 3 request	FlexIO0
102	Receive request	LPUART5

Table 7. Async DMA configuration...*continued*

Slot number	DMA request description	Module name
103	Transmit request	LPUART5
123	FIFO request	ADC2
124	FIFO request	ADC3

5 Wake-up information

Table 8 displays the typical wake-up time and wake-up sources in different low power modes. Here the typical wake-up time values are taken from the *Mixed-signal Arm Cortex-M33 MCU with 180 MHz, up to 1024 KB Flash* (document MCXA345/346 data sheet).

Table 8. Wake-up information

Symbol	Description	Wake-up source	Typical wake-up time
tSLEEP	Sleep → Active	All peripherals	0.42 µs
tDSLEEP	Deep Sleep → Active	Async peripherals	9.01 µs
tPWDN	Power Down → Active	WUU, Reset pin	18.84 µs
tDPWDN	Deep Power Down → Active	WUU, Reset pin	1.57 ms

6 Low power and wake-up optimization

This section explains various methods for optimizing power consumption and factors to consider for wake-up optimization.

6.1 Power consumption optimization

Following are the different ways of optimizing power consumption:

- **Regulator**
  - Configure the appropriate voltage level and drive strength.
  - In Power Down mode, LDO_CORE can provide retention voltage to the CORE domain.
- **Peripherals**
  - Disable unused analog peripherals by configuring the ACTIVE_CFG1 and LP_CFG1 registers.
- **Memories**
  - Flash
    - Configure the FLASHCR register to place the flash memory in a low-power state.
  - SRAM
    - Use auto clock gating by configuring the RAM_CTRL register of SYSCON.
    - SRAM can be individually retained or powered down by using software in the Power Down and Deep Power Down mode.
- **Clocks**:
  - Select and configure the appropriate CPU_CLK/SYSTEM_CLK.
  - Disable unused clock sources.
  - Configure the MRCC_GLB_CC0/MRCC_GLB_CC1/MRCC_GLB_CC2/ MRCC_GLB_ACC0/MRCC_GLB_ACC1/MRCC_GLB_ACC2 registers to disable or enable automatic clock gating the clocks to modules.
- **Monitors**:
  - Disable unused voltage monitors (HVDs/LVDs).

- **I/O pins**
  - For unused I/O pins, use the default configuration (floating input) as it minimizes leakage current. With the default configuration, the input buffer and the internal pull resistor are disabled.
  - While using I/O pins, power consumption can be reduced by increasing the resistance of the external resistor appropriately.

6.2 Wake-up time consideration

Consider the following points relating to the wake-up time:

- SLOW_CLK frequency
  - The wake-up process is implemented through CMC.
  - SLOW_CLK is the clock source of CMC and its frequency is equal to 1/6 SYSTEM_CLK.
- Different VDD_CORE level
  - Recovery time required for different voltage levels. For details, refer to the “Low-power wake-up delay” table in the *MCX A345 and MCX A346 Reference Manual* (document MCXAP144M240F60RM).
- Longer time of clock recovery time and flash recovery time
- Interrupt latency

7 Demo operation

This section describes the steps, setup, and results for a demo to change the low power configurations and reproduce the typical power consumption and wake-up time data. For more information, see *Mixed-signal Arm Cortex-M33 MCU with 180 MHz, up to 1024 KB Flash* (document MCXA345/346 data sheet).

7.1 Hardware and software requirements

Table 9 describes the hardware and software requirements for running the demo.

Table 9. Hardware and software details

Category	Description	Comments
Hardware	• FRDM-MCXA346 board • One Type-C USB cable	***Note:*** • *To measure the power consumption, use the MCU-Link Pro or a multimeter to connect to JP1.* • *To measure the power consumption accurately, the rework is required:* – *Remove R52* – *Remove R26* • *To measure the wake-up time, use an oscilloscope or logic analyzer.* • *To measure the wake-up time accurately, the rework is recommended:* – *Remove C39*
Software	• MCUXpresso IDE v25.6 or later • SDK_25_06_00_FRDM-MCXA346	

7.2 Setup

The following sections describe the steps to perform the demo.

7.2.1 Hardware connection

To connect J15 of the FRDM-MCXA346 board and the USB port of the PC, use a Type-C USB cable.

7.2.2 Importing the project

To import the project, perform the steps as follows:

1. Open MCUXpresso IDE v25.6. In the **Quickstart Panel,**select**Import from Application Code Hub**, as shown in Figure 4.

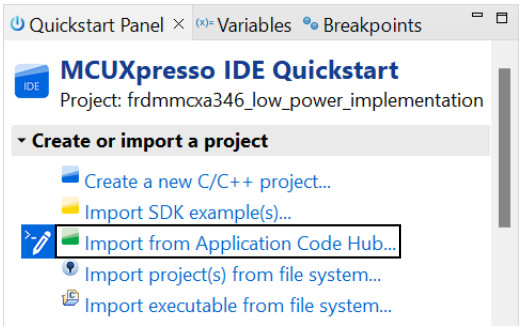

Figure 4. Import from Application Code Hub

2. Enter the demo name in the search bar, as shown in Figure 5.

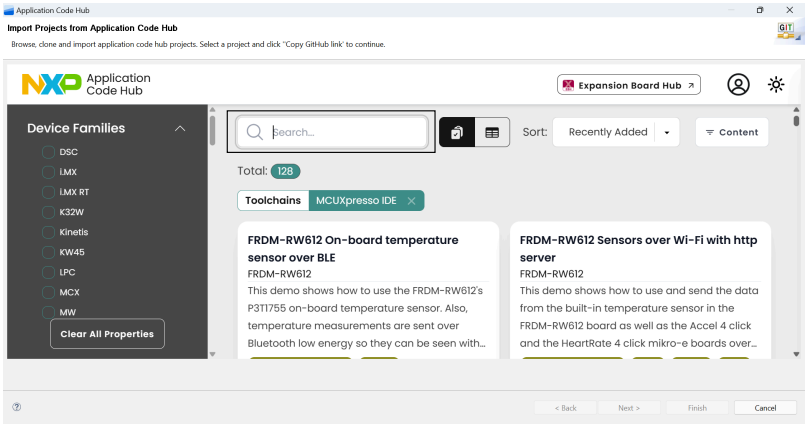

Figure 5. Search demo

3. Click the **GitHub link** icon, as shown in Figure 6. MCUXpresso IDE automatically retrieves project attributes. Then, click **Next**.

Figure 6. Copy GitHub link

4. Select the main branch and then click **Next**. Now, select the MCUXpresso project and then click the **Finish** button to complete the import.
   Note: *Install the SDK_25_06_00_FRDM-MCXA346 on your MCUXpresso IDE after performing the above steps.*

7.2.3 Building and flashing the project

To build and flash the project, perform the steps as follows:

1. Click **Build** button from the toolbar, then wait for the build to complete as shown in Figure 7.

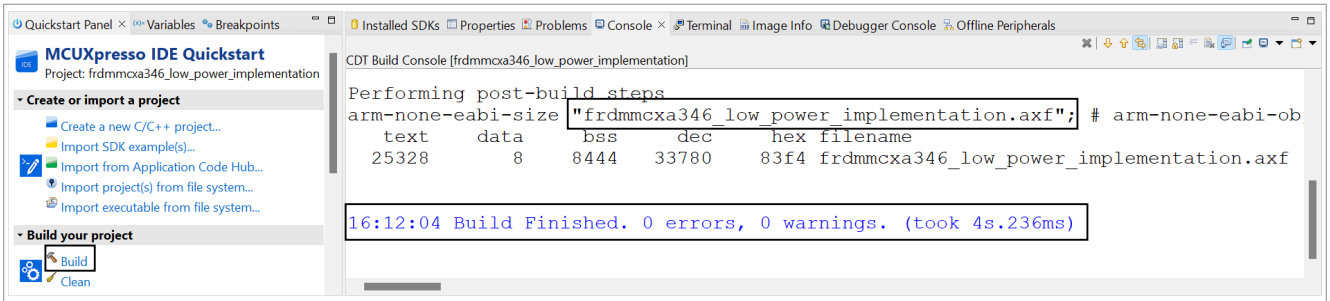

Figure 7. Build the project

2. To program the executable to the board, select the **GUI Flash Tool** from the toolbar as shown in Figure 8.

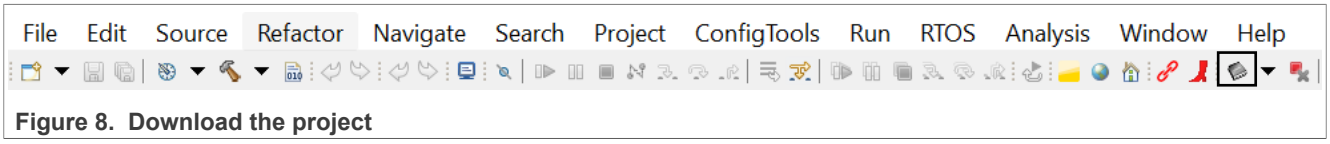

Figure 8. Download the project

7.2.4 Selecting the low power mode and the corresponding configurations

To select the low power mode and the corresponding configurations, perform the steps as follows:

1. Open a serial terminal with a 115,200 baud rate.
2. Follow the prompts as shown in Figure 9. To enter a different low power mode, enter one of the keys from A to E.

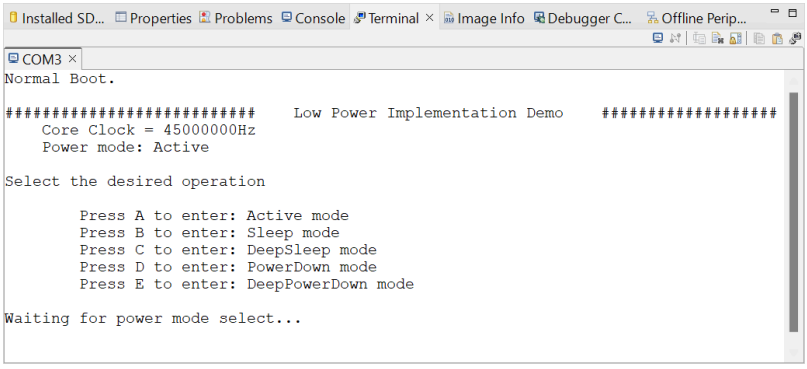

Figure 9. Select low power mode

3. Different low power modes provide different configurations. Therefore, you must select the corresponding configuration according to the prompts. Figure 10 shows the configurations provided in Deep Power Down mode.

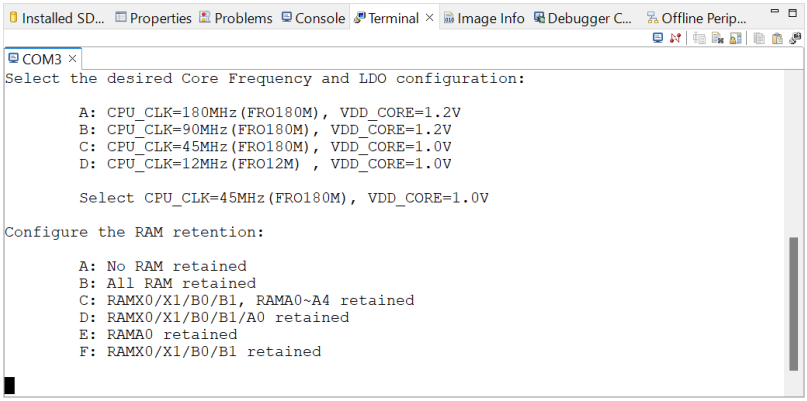

Figure 10. Select low power configurations

4. Figure 11 shows the entire configuration process. To wake up the MCU, press the **SW2** button on FRDM-MCXA346.
   Note: *Press the wake-up button only when the prompt message appears. Pressing it otherwise results in a wake-up failure.*

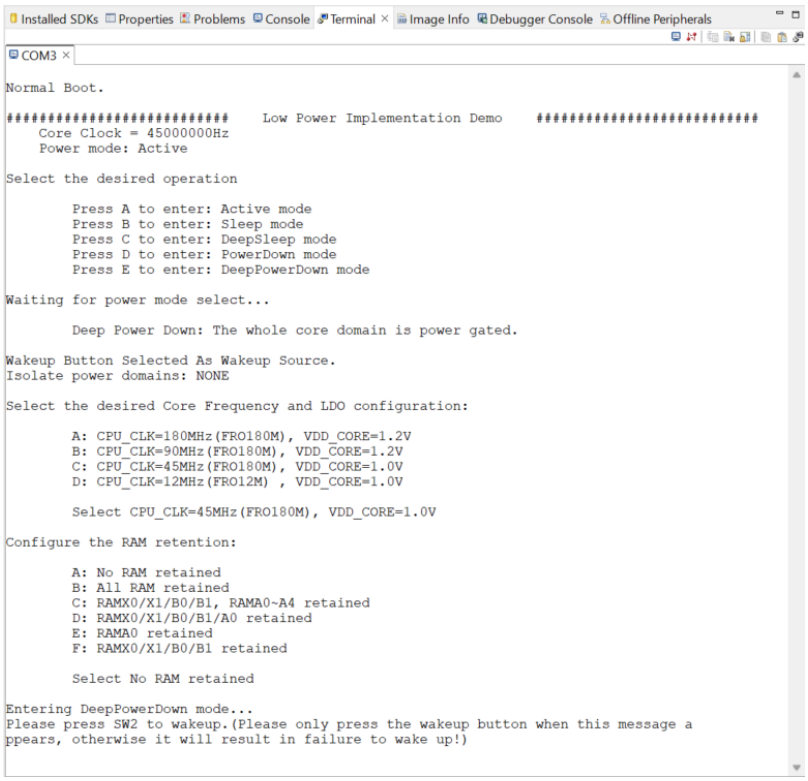

Figure 11. All prompts

7.2.5 Measuring power consumption

The following sections describe the steps for measuring power consumption on the FRDM-MCXA346 board.

7.2.5.1 Power consumption measurement using MCU-Link Pro and MCUXpresso IDE

To measure power consumption using MCU-Link Pro and MCUXpresso IDE, perform the steps as follows:

1. Connect MCU-Link Pro and FRDM-MCXA346 according to Table 10. Then, connect MCU-Link Pro and FRDM-MCXA346 to the host PC.

Table 10. MCU-Link Pro and FRDM-MCXA346 connection

MCU-Link Pro	FRDM-MCXA346
J9-1 (Current in)	JP1-1 (IDD_MCU in)
J9-3 (Current out)	JP1-2 (IDD_MCU out)
J9-2 (GND)	J3-14 (GND)

2. To measure the current using the MCUXpresso IDE, follow the steps in Figure 12.

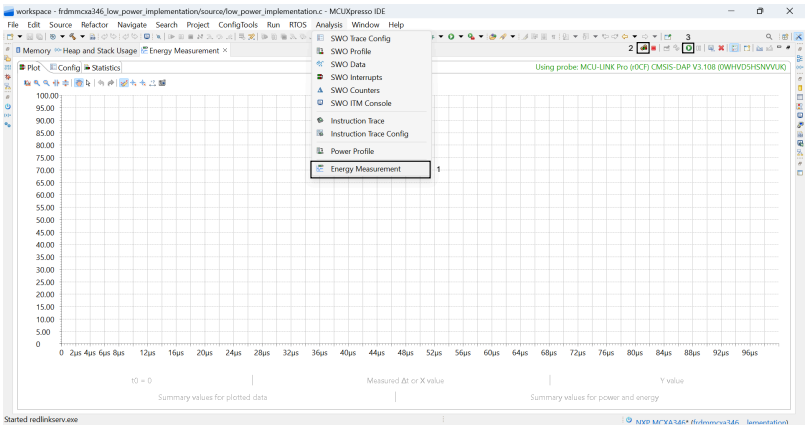

Figure 12. MCUXpresso energy measurement

7.2.5.2 Power consumption measurement using a multimeter

You can also use a multimeter to measure the current at the JP2 jumper of the FRDM-MCXA346 board.

7.2.6 Measuring wake-up time

As shown in Figure 13, determine the wake-up time by measuring the delay between the falling edges of J6-2 (P1_7) and J6-1 (P1_6) using an oscilloscope or logic analyzer.

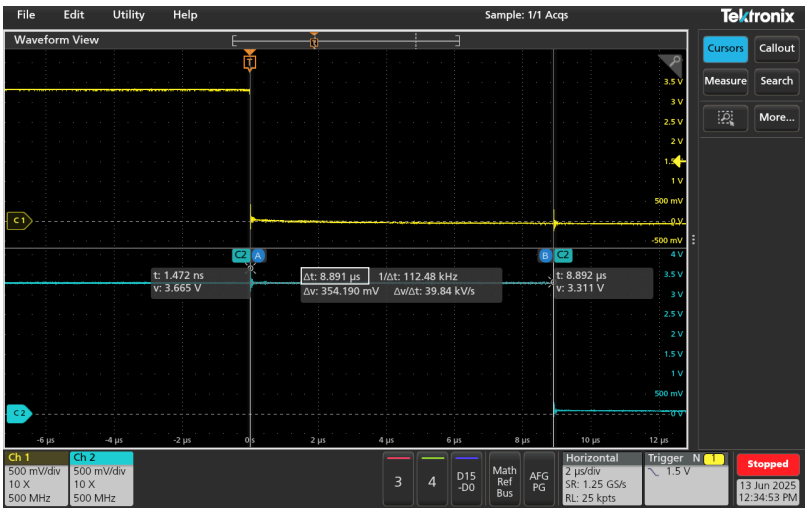

Figure 13. Measuring wake-up time

7.3 Reference results

Table 11 provides references for the power consumption and wake-up time.

Note:

- *Before test, rework the board as described in Section 7.1.*
- *Different samples, temperature, and measuring instruments affect test results.*
- *Before measuring each data, POR is recommended.*
- *This demo is not configured the same as the data sheet, so the test data can be slightly different.*
- *For information on wake-up time, refer to the "Power mode transition operating behaviors" table in the Mixed-signal Arm Cortex-M33 MCU with 180 MHz, up to 1024 KB Flash (document MCXA345/346 data sheet).*
- *For information on different power consumption data, refer to "Power consumption operating behaviors" section in the Mixed-signal Arm Cortex-M33 MCU with 180 MHz, up to 1024 KB Flash (document MCXA345/346 data sheet).*

Table 11. Reference results

Power mode	Description	Tested power consumption	Power consumption in data sheet	Tested wake-up time	Wake-up time in data sheet
Sleep	VDD_CORE = 1.2 V CPU_CLK = 180 MHz	8.36 mA	8.08 mA	0.13 µs	N/A
	VDD_CORE = 1.2 V CPU_CLK = 90 MHz	4.60 mA	N/A	0.24 µs	N/A
	VDD_CORE = 1.0 V CPU_CLK = 45 MHz	2.23 mA	2.16 mA	0.44 µs	0.42 µs
	VDD_CORE = 1.0 V CPU_CLK = 12 MHz	0.583 mA	0.579 mA	1.66 µs	N/A
Deep Sleep	VDD_CORE = 1.2 V CPU_CLK = 180 MHz FRO12M disabled	555.2 µA	542.27 µA	7.18 µs	N/A
	VDD_CORE = 1.2 V CPU_CLK = 90 MHz FRO12M disabled	555.0 µA	N/A	7.74 µs	N/A
	VDD_CORE = 1.0 V CPU_CLK = 45 MHz FRO12M disabled	92.43 µA	96.02 µA	8.89 µs	9.01 µs
	VDD_CORE = 1.0 V CPU_CLK = 45 MHz FRO12M enabled	160.86 µA	155.29 µA	8.89 µs	N/A
	VDD_CORE = 1.0 V CPU_CLK = 12 MHz FRO12M disabled	92.34 µA	N/A	17.23 µs	N/A
Power Down	VDD_CORE = 1.2 V CPU_CLK = 180 MHz All RAM retained	553.5 µA	N/A	8.14 µs	N/A
	VDD_CORE = 1.2 V CPU_CLK = 90 MHz	553.3 µA	N/A	8.69 µs	N/A

Table 11. Reference results*...continued*

Power mode	Description	Tested power consumption	Power consumption in data sheet	Tested wake-up time	Wake-up time in data sheet
	All RAM retained				
	VDD_CORE = retention voltage CPU_CLK = 45 MHz All RAM retained	32.62 µA	31.95 µA	18.45 µs	18.84 µs
	VDD_CORE = retention voltage CPU_CLK = 45 MHz RAM X0/X1/B0/B1/A0 retained	30.49 µA	N/A	18.45 µs	N/A
	VDD_CORE = retention voltage CPU_CLK = 12 MHz All RAM retained	32.59 µA	N/A	26.70 µs	N/A
Deep Power Down	VDD_CORE = 1.0 V CPU_CLK = 45 MHz All RAM disabled Wake timer enabled FRO16K enabled	0.68 µA	0.646 µA	1.57 ms	1.57 ms
	VDD_CORE = 1.0 V CPU_CLK = 45 MHz All RAM retained Wake timer enabled FRO16K enabled	3.84 µA	3.4 µA	1.57 ms	N/A
	VDD_CORE = 1.0 V CPU_CLK = 45 MHz RAM X0/X1/B0/B1, A0~A4 retained Wake timer enabled FRO16K enabled	2.57 µA	2.29 µA	1.57 ms	N/A
	VDD_CORE = 1.0 V CPU_CLK = 45 MHz RAM X0/X1/B0/B1/A0 retained Wake timer enabled FRO16K enabled	1.84 µA	1.66 µA	1.57 ms	N/A
	VDD_CORE = 1.0 V CPU_CLK = 45 MHz RAM A0 retained Wake timer enabled FRO16K enabled	0.89 µA	0.849 µA	1.57 ms	N/A
	VDD_CORE = 1.0 V CPU_CLK = 45 MHz RAM X0/X1/B0/B1 retained Wake timer enabled FRO16K enabled	1.73 µA	1.55 µA	1.57 ms	N/A

8 References

Table 12 lists the references used to supplement this document.

Table 12. References

Reference	Link/how to obtain
Mixed-signal Arm Cortex-M33 MCU with 180 MHz, up to 1024 KB Flash (document MCXA345/346 data sheet)	https://www.nxp.com/doc/MCXAP144M240F60
MCX A345 and MCX A346 Reference Manual (document MCXAP144M240F60RM)	https://www.nxp.com/doc/MCXAP144M240F60RM
MCX A34 Mixed-Signal, Optimized for Motor Control and High-Performance Analog Peripherals	https://www.nxp.com/products/MCX-A345-A346
MCX A series microcontrollers	https://www.nxp.com/products/processors-and-microcontrollers/arm-microcontrollers/general-purpose-mcus/mcx-arm-cortex-m/mcx-a-series-microcontrollers:MCX-A-SERIES
FRDM Development Board for MCX A345 and MCX A346 MCUs	https://www.nxp.com/design/design-center/development-boards-and-designs/FRDM-MCXA346
MCU-Link Pro Debug Probe	https://www.nxp.com/design/design-center/software/software-library/mcu-link-pro-debug-probe:MCU-LINK-PRO
MCUXpresso Integrated Development Environment (IDE)	https://www.nxp.com/design/design-center/software/development-software/mcuxpresso-software-and-tools-/mcuxpresso-integrated-development-environment-ide:MCUXpresso-IDE

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10 Revision history

Table 13 summarizes the revisions to this document.

Table 13. Revision history

Document ID	Release date	Description
AN14765 v.1.0	22 August 2025	Initial public release

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