AN14687

Ease CRA Compliance with MCX N

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Document information

Information	Content
Keywords	AN14687, MCXN, security compliance, CRA
Abstract	This document addresses OEMs who want to understand how MCX N facilitates the implementation of CRA requirements.

1 Introduction

The potential risk from cyberattacks increases as the number of connected devices, machines, and sensors keeps growing. It is predicted that in 2025, there will be 75 billion connected devices worldwide. With the number of devices and the size of the attack surface increasing, in 2025, there will be an estimated 10.5 trillion dollars in damages from cybercrime[1].

Security is a critical element in the development of products against intentional or unintentional threats. These threats include unauthorized access, installation of malware, ransomware, spyware, or loss of data with the corresponding privacy breach. They can have impact of a secondary nature, such as personal injury, equipment damage, supply chain downtime, environmental impact, loss of production, or violation of regulatory requirements.

To improve cyber resilience in the European Union, in 2024, the European Parliament adopted the Cyber Resilience Act[2] (CRA) to ensure the cybersecurity of products and software with digital elements. It covers anything from hard disks and chips to firewalls and robots. The CRA describes the requirements (technical and process) and obligations of manufacturers, importers, distributors, and third parties that supply their products to the European market.

The CRA was published in the European Official Journal as Regulation (EU) 2024/2847. It will be fully enforced from December 11th, 2027. From that date, all products with digital elements introduced in the European market must comply with the regulation. Products operating on markets and applications with similar security requirements are not required to comply with the CRA (for example certain vehicle types, medical, aeronautic equipment and planes, as well maritime equipment).

For NXP, the impact is twofold. Firstly, NXP products are digital elements that must comply with CRA. Secondly, NXP products are integrated into OEM devices and machines that must comply with CRA.

Manufacturers of products with digital elements must comply with the essential requirements of the CRA. This requires manufacturers to "own" the product's cybersecurity risk, mitigate such risk, and communicate it to the users. Only when compliant, a manufacturer is allowed to affix the CE mark to its products. This mark is mandatory for access to the EU market.

Penalties for noncompliance with the essential requirements of the CRA amount to up to 15 million euros, or 2.5 % of the annual turnover, whichever is higher. Those surveillance-authorized are empowered to issue product recalls or, in extreme circumstances, withdrawal from the European market in cases of nonconformance. Therefore, the consequences of the CRA have a particularly large impact.

2 How to use this document

This document addresses OEMs who want to understand how the MCX N series can facilitate the implementation of CRA requirements. While the MCX N series provides core security capabilities that can be mapped to the cybersecurity requirements of the CRA, the OEM must fill the remaining compliance gap by performing additional actions. This document provides guidance and supporting evidence from the MCX N security capabilities toward the developer's CRA conformance claims.

Throughout this document, the requirements and text of the CRA is condensed or simplified to summarize the ease of reading or highlight the applicability to the embedded context. For compliance, always consult the full text of the CRA. The applicability of this application note cannot guarantee the legal certainty required by the CRA conformance. Use it only as a guidance for manufacturers addressing conformance requirements rather than the attestation of conformance to the CRA.

1 https://cybersecurityventures.com/cybercrime-damage-costs-10-trillion-by-2025/
2 https://eur-lex.europa.eu/eli/reg/2024/2847/oj

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3 Cyber Resilience Act overview

The Cyber Resilience Act (CRA) sets common security requirements for products with digital elements sold in the EU. This addresses the issue that many products on the market are currently not secure and that it is difficult to ascertain which of the products are secure or how to utilize them securely. The main CRA document consists of 8 chapters and another 8 annexes to provide additional details. The CRA’s goal is to guarantee[3]:

- Harmonized rules when bringing products or software with digital components to market
- A framework of cybersecurity requirements governing the planning, design, development, and maintenance of such products, with obligations at every stage of the value chain
- Obligation to provide a duty of care for the entire life cycle of such products

The requirements listed throughout the act are as follows:

- **Cybersecurity by design and by default:** Cybersecurity must be considered during product design from the start. CRA defines what kind of information and documentation to create and gather as well as depending on the product’s security category, what kind of conformity assessments it must go through.
- **Essential cybersecurity and vulnerability handling requirements, including reporting obligations:** CRA sets technical cybersecurity requirements on the products to reduce the attack surface as much as possible. It also sets vulnerability handling requirements for vulnerabilities appearing after production.
- **Conformity assessment and compliance:** Digital products are subjected to a specified conformance assessment, depending on their security category.
- **Fines:** CRA enforces compliance with the penalty of fines for noncompliant manufacturers, importers, or distributors.
- **The interplay between conformity assessment procedure and existing or upcoming cybersecurity legislation:** CRA aims to complement and harmonize with existing and upcoming legislation, such as the EU Cybersecurity Act.

The MCX N series can be of added value in meeting the requirements listed above. The security features of the MCX N can be leveraged by the OEM to implement security countermeasures in an efficient and reliable manner.

Products with Digital Elements (PDEs, also called plain products in this document) are classified into four categories in the Cyber Resilience Act:

- **Nonimportant PDEs**
- **Important PDEs: class I**
- **Important PDEs: class II**
- **Critical PDEs**

Products that are not security-important fall in the nonimportant category. Products that are security-important are classified in the remaining categories based on their functionality, intended use, and optional further criteria. A different standard of assessment/certification applies depending on which category each product has in the CRA Annex III and IV. In the default category, a security self-assessment suffices, whereas critical products

3 From: EU Cyber Resilience Act | Shaping Europe’s digital future

require a mandatory EU certification. The intention is that approximately 90 % of digital products falls into the default category.

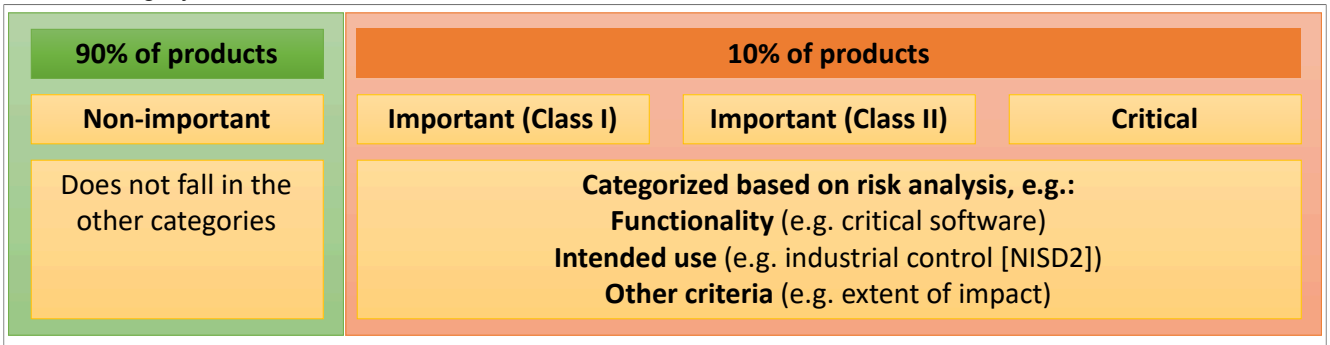

Figure 1. Cyber Resilience Act

Examples of each class are shown in Table 1. A more extensive list is in the CRA regulation[4]. Conformance-assessment criteria are in Article 32 of the regulation.

Table 1. Examples

Category	Examples
Nonimportant	• Hard drives • Smart speakers • Robot vacuum • Games and toys
Important (class I)	• Identity/network management systems • Microprocessors/controllers with security-related functionalities • Smart home products with security functionalities • Personal wearables for health monitoring
Important (class II)	• Hypervisors and container runtime systems • Firewalls, intrusion detection, and prevention systems • Tamper-resistant microprocessors • Tamper-resistant microcontrollers
Critical	• Hardware devices with security boxes • Smart meter gateways within smart metering systems • Devices for advanced security purposes, including secure crypto processing • Smartcards or similar devices, including secure elements

4 Leveraging the MCX N to meet Cyber Resilience Act requirements

The clearest contribution of NXP products, such as the MCX N, to the CRA compliance of an end-product it's integrates into lies in the MCX N security features that can be leveraged by the end-product. Annex I of the CRA lists the Essential Cybersecurity Requirements (ECRs) for products with digital elements (PDEs). This chapter describes how the MCX N can be leveraged to ease compliance with the requirements of Annex I (Part 1 and 2). The last section of this chapter provides additional support for the remaining requirements of the regulation.

Where possible, we use security terminology from the White-Paper Security Primitives: Common Nomenclature to Describe Security Requirements in (I)IoT Systems (see: https://www.nxp.com/securityprimitives).

4 https://eur-lex.europa.eu/eli/reg/2024/2847/oj

4.1 Cyber Resilience Act Annex I, Part 1

This part of the document covers security requirements relating to the properties of PDEs.

4.1.1 Requirement (1): Secure manufacturing

The first requirement in Annex I, Part 1, ties to the development process of the product: "Products with digital elements shall be designed, developed, and produced in such a way that they ensure an appropriate level of cybersecurity based on the risks." Starting from the design of a product to its production, at each level, make a risk-based analysis to apply the right level of cybersecurity.

At NXP, security is integral to the entire product life cycle. A dedicated team of security experts supports the product development to reduce the risk of critical vulnerabilities. The in-house EdgeLock Secure Assurance program supports the NXP Secure Manufacturing Process, as well as certifications like ISO/SAE 21434 and IEC 62443-4-1.

The MCX N supports the OEM with security features leveraged by the end-product to get the desired security capability. Independent third parties evaluate and certify those functionalities against EN 17927 (SESIP scheme) and PSA Certified, both at Level 3, equivalent to the AVA_VAN.3 level of assurance under ISO 15408 (common criteria). The SESIP certificate supports the OEM claims of the adequate level of security implementation (proportionality to the risk) by clearly identifying the security functionality provided by the MCX N, as well as its level of assurance.

4.1.2 Requirement (2): Cybersecurity requirements

The Requirement (2) of Annex I Part 1 lists 13 cybersecurity measures that a product must comply with. This section explains these one by one. The risk assessment referred to in Article 13(3) of the CRA states that the products with digital elements shall:

a. **Be available on the market without known exploitable vulnerabilities:**
   Security is at the core of the MCX N development cycle. Security-by-design is a part of the NXP (certified) cybersecurity engineering processes. The process increases the security maturity level of the device by having security experts perform reviews and assessments of the device’s security concept, architecture, design, and implementation.
   As part of the certification process under SESIP, the security evaluation and certification third parties perform a verification against known exploitable vulnerabilities in the MCX N.

b. **Be in a secure by default configuration and can reset the product to its original state:**
   The MCX N's secure boot mechanism ensures the secure initialization of the device at each power up and verifies the authenticity and integrity of the firmware.
   To reset to the original state, NXP recommends that OEM implement a secure backup and recovery mechanism. An over-the-air (OTA) update mechanism combined with the enablement of secure boot can verify independent validity and/or perform conformity checks for any newly downloaded firmware. Such checks should already be part of the OEM OTA implementation to ensure that the update was from a trusted source and not altered or corrupted during transmission. For MCX N, refer to *Dual Boot Secure Firmware Update using OTA HTTP Server* (document AN14475) for information about secure firmware update with dual image boot. MCX N supports restoring the OEM device to a secure-by-default configuration by ensuring the secure erasing of sensitive data when changing lifecycle state. This process includes zeroing the ELS keystore, PUF keystore, PKC block, and "RAM A" memory bank.
   The OEM should leverage the lifecycle management of the MCX N to close the relevant debug ports after manufacturing. This puts the device into the default state that prevents attacks that utilize the debug functionality of a product on the market.
   The MCX N has been assessed during the SESIP evaluation to a determined level of cybersecurity in a defined context of risks (AVA_VAN). This includes the verification of a secure-by-default configuration, unambiguous identification to the integrator that the certified version is secure to evaluate, and verification of all guidance and documentation.

c. **Ensure that vulnerabilities can be addressed through security updates:**

Even when carefully designed, unknown exploits can appear after a product enters the market. A secure update mechanism ensures that a product can be patched if it is within the physical capabilities of the device. NXP recommends that OEM OTA mechanisms implement independent validity and/or conformity checks for any newly downloaded firmware. Such checks should already be part of the OEM's OTA implementation to ensure that the update was from a trusted source and not altered or corrupted during transmission. For information about secure firmware update with dual image boot, see *Dual Boot Secure Firmware Update using OTA HTTP Server* (document AN14475). For information on how to ensure that the firmware is secure and authenticated during OTA via SB3 files, see *MCX N94x Over-The-Air (OTA) Update by Using SB3 File* (document AN14166).

For the MCX N family, during the secure update phase the firmware is encrypted using AES-128/256 and signed using ECDSA P-256/384, following the SB3.1 firmware image format. After updating the firmware image, the secure boot mechanism verifies the authenticity and integrity of the new firmware image, ensuring the Immutable RoT still safeguards the authenticity of the latest firmware. While at rest and during secure boot, the firmware image can be encrypted using PRINCE.

d. **Protects against unauthorized access by using mechanisms, such as authentication, identity, or access management systems, and reports possible unauthorized access:**

Authentication and access-control mechanisms relate to many cryptography and security functionalities. The software on the device should be from an authenticated source, access to data and functionality should be controlled, and cryptographic protocols should be available for the OEM to implement their own (PKI-based) access-management systems. We focus on the most important features of the MCX N that supports the OEM in their compliance with Requirement (2)(d).

The MCX N contains several mechanisms to ensure that sensitive data and operations can only be accessed by authorized processes. Firstly, the EdgeLock Enclave (ELE) Core Profile is an independent security domain that provides security services, which helps ensure key management and execution of cryptographic services within a secure environment. The ELE provides a secure environment that enables applications to execute secure cryptographic services.

Secondly, TrustZone-M (TZ-M) is enabled on the Cortex M33 cores of the MCX N. It enables Secure Isolation during runtime by providing four distinct levels of privilege: secure-privilege, secure-user, non-secure-privilege, non-secure-user. Every peripheral is equipped with a Peripheral Protection Checker (PPC) that can be programmed to control access to that peripheral, following the Arm TrustZone security principles. Every memory is equipped with a Memory Protection Checker (MPC) that can also be programmed in the same way as the PPC. The Secure AHB Controller is in charge of programming all PPC and MPC blocks and only when the highest level of privilege (secure-privilege) is enabled. This allows further protection of sensitive data from unauthorized processes.

Secure boot is a feature that ensures authenticity, integrity, and optional confidentiality of the device's bootloader, firmware, and other software during the boot process and ensures that the intended secure lifecycle state is reached. The authenticity of the boot code is established by the use of Cipher-based Message Authentication Code (CMAC) and Elliptic Curve Digital Signature Algorithm (ECDSA). Support is provided for up to four Root of Trust keys.

The MCX N is further supported by NXP's EdgeLock 2GO (EL2GO) service. This can provision device-unique credentials such as identity keypairs and certificates securely into the secure storage of the device. Such credentials are then used to verify the identity of the device when it connects to cloud or other systems.

The OEM must implement further logging and data protection. The MCX N can support OEM protection with its cryptographic acceleration options. For details, see Requirement (2)(e).

e. **Protect the confidentiality of stored, transmitted, or otherwise processed data by applying encryption to data at rest or in transit:**

As with Requirement (2)(d), the protection of confidentiality also relates to many security paradigms. The focus is on the most important MCX N features that can support the OEM in their compliance with Requirement (2)(e).

To support the OEM in securely storing data at rest in less secure memory, MCX N EdgeLock Enclave (ELE) can also encrypt information for secure storage.

On-the-fly encryption/decryption stores the encrypted application code or data in an internal flash memory using the NPX PRINCE mode or external flash memory using the Inline PRINCE Encrypt Decrypt (IPED) algorithm.

Note: *The external serial flash and IPED are only supported on MCX N products.*

For other applications that require encryption, like data in transit, the MCX N ELE supports the acceleration of cryptographic operations. Both symmetric and asymmetric crypto accelerators are included in the ELE to securely process keys and data for encrypted transmission (for example, by TLS). This includes:

- Symmetric cryptography: AES 128/192/256 in supported modes incl. ECB/CBC/CTR/GCM
- Asymmetric cryptography: ECC P-256, ECDSA P-256, ECDHE
- Hash functionality: SHA 224/256/384/512 (including HMAC and CMAC)

In addition to the cryptographic services by the ELE, MCX N includes a PKC accelerator in the hardware to implement accelerated ECC, RSA, or other public-key cryptographic operations.

The MCX N ELE supports key storage, including key attributes. These key attributes include identifier, key type, and both volatile and persistent keys. For non-volatile memory export, persistent keys are encrypted and encapsulated (with an IV generated by ELE). When required, the encapsulated keys are loaded into the internal ELE memory and decapsulated. Keys are stored in protected flash regions in the form of RFC3394 blobs.

f. **Protect the integrity of stored, transmitted, or otherwise processed data, commands, programs, and configuration against unauthorized modification and report on corruptions:**

After authenticity in Requirement (2)(d) and confidentiality in Requirement (2)(e), Requirement (2)(f) focuses on the integrity of data on the product. Again, the focus is on the most important MCX N aspects that support their compliance with this requirement.

As mentioned before, secure boot protects against the execution of unauthorized firmware. It works by checking the integrity of the software to ensure that the software that is going to be executed has not been modified to work differently than what was loaded by the manufacturer (either at the factory or as part of software upgrades). The authenticity of the boot code is established by the use of Cipher-based Message Authentication Code (CMAC) and Elliptic Curve Digital Signature Algorithm (ECDSA). Support is provided for up to four Root of Trust keys.

Additionally, MCX N's code watchdog (CDOG) has a secure counter and instruction timer that can detect unexpected changes to the code execution flow. This module can be configured to reset or interrupt the processor core when it detects a fault. The ELE can also encrypt information for secure storage in less secure memory. On MCXNx4x devices, on-the-fly encryption and decryption can be performed by the FlexSPI interface using PRINCE to store encrypted application code or data in an external flash device and helps ensure the integrity of that data. On all MCX N devices, on-the-fly encryption and decryption can be performed by the NPX interface using PRINCE to store encryption application code or data in internal flash.

The ELE supports symmetric crypto accelerators used to implement further integrity checks. For more on the supported cryptographic algorithms, refer to Requirement (2)(e).

For more information about the CRC hash function and how to test and compare its performance, refer to *CRC Calculation Features and Performance on MCX* (document AN14271).

g. **Process only data that are adequate, relevant, and limited to what is necessary in relation to the intended use of the product ("minimization of data"):**

The minimization of data ensures that a potential attacker has the least attack surface possible. The OEM must realize this requirement for its application data.

When using the MCX N with EL2GO, we support the OEM by minimizing the user data processed in the cloud. EL2GO does not profile on user data such as IP addresses and does not store this type of data for future use.

h. **Protect the availability of essential and basic functions, and be resilient against and able to mitigate denial-of-service attacks:**

Requirement (2)(h) aims to mitigate attacks that attempt to make the product unavailable. This can be done by applying software isolation techniques to protect essential processes from external non-essential applications. Both the ELE and TrustZone offer software isolation and thereby mitigate against denial-of-service attacks.

TrustZone-M is enabled on the Cortex-M33 cores of the MCX N. It enables secure isolation during runtime by providing four distinct levels of privilege: secure-privilege, secure-user, non-secure-privilege, non-secure-user. Every peripheral is equipped with a Peripheral Protection Checker (PPC) that can be programmed to control access to that peripheral, following the Arm TrustZone security principles. Every memory is equipped with a Memory Protection Checker (MPC) that can also be programmed in the same way as the PPC. The Secure AHB Controller is in charge of programming all PPC and MPC blocks and only when the highest level of privilege (secure-privilege) is enabled. This allows further protection of sensitive data from unauthorized processes.

i. **Minimize the negative impact of by-products on the availability of services of others:**

The impact of an OEM’s product on other devices should be controlled in the OEM application.

j. **Be designed, developed, and produced to limit attack surfaces, including external interfaces:**

Limiting the attack surface gives malicious actors the least possibility to mount an attack. As was the case with the confidentiality, authenticity, and integrity of data, the attack surface of a device is reduced by the collaboration of many security components. The main feature of the MCX N series supports the OEM’s compliance with the CRA through its ability to control access throughout the chip lifecycle.

Trust provisioning is a process used for the creation of initial Device Identity keys, and its purpose is to provide a cryptographic proof of the device’s origin and to offer a set of tools to the OEM for secure provisioning of their own

assets. In MCX N, a device-unique key (DUK) is available in every chip. The DUK is derived from the chip PUF at every secure boot. At boot, the ROM derives other keys from the DUK using CKDF.

The lifecycle of MCX N is managed by its boot ROM. The lifecycle states progress from NXP manufacturing lifecycles to the OEM development and manufacturing states, to the in-field product state, and then finally to reopening up the chip successively from fully closed to partially closed to fully open again for silicon analysis in the case of a failure. The lifecycle state closes or restricts access to the appropriate test and debug port to limit the attack surface. If the device is in the Bricked state or any invalid lifecycle state, then the part is locked.

In the context of the SESIP certification, the attack surfaces are identified as part of the vulnerability analysis, and any unnecessary external interfaces are reported.

k. **Be designed, developed, and produced to reduce the impact of an incident:**

While Requirement (2)(j) focuses to reduce the chance of a security incident, Requirement (2)(k) aims to reduce the consequences (if they happen). One main technique in which the MCX N can support the OEM with compliance is the use of software isolation and extensive protection of cryptographic keys and certificates.

Both the ELE and TrustZone offer software isolation and mitigate the impact of attacks on the non-secure world. See also Requirement (2)(h).

There is an Intrusion and Tamper Response Controller (ITRC) available on MCX N devices which can configure the response action for an intrusion event detected by on-chip security sensors. NXP recommends that the ITRC is configured for secure and privileged access only to prevent unintentional or malicious modification of the system operation by nonsecure software. When the response is triggered, memory locations that contain cryptographic keys, passwords, or other critical assets can be zeroized.

Additionally, to reduce the impacts of incidents caused by the MCX N implementation above, its strength is supported by the vulnerability analysis (which provides an overall security status of the implementation) and verified during the SESIP certification.

l. **Provide security-related information by recording and/or monitoring relevant internal activity, with an opt-out mechanism for the user:**

The recording and monitoring on the application level must be implemented by the OEM. The OEM may use security services claimed by MCX N to support this requirement, for instance Root-of-Trust base, secure cryptography, or secure storage is needed, and so on. However, this is to be determined case by case.

m. **Provide the possibility for users to securely and easily purge all data and settings:**

Upon decommissioning or resale of a device, erase all information in the MCX N. The EdgeLock Enclave (ELE) supports secure provisioning. You can implement the erasure of this information in software, but you must undertake an explicit action in the decommissioning. The cryptographic support of the MCX N ELE can be used to port the settings and data to a backup before decommissioning. The bricked state or field return state support erasure of data in the device lifecycle management. This ensures that the device information cannot be read out after decommissioning.

4.2 Cyber Resilience Act Annex 1, Part 2

The second category of requirements in the Cyber Resilience Act focuses on the handling of vulnerabilities. NXP can support the requirements of Annex 1, Part 2 as follows.

NXP Product Security Incident Response Team (PSIRT) is committed to rapidly addressing material security vulnerabilities in NXP products by responding and documenting reported material vulnerabilities, and, where feasible and appropriate, providing customers with clear guidance on the impact, severity, and available mitigation measures.

These efforts extend beyond software vulnerabilities and cover:

- Security incidents in NXP products (hardware or software).
- Flaws in NXP documents regarding security information or recommendations (for example, datasheets and application notes).
- Security-sensitive NXP documents or security-relevant information regarding NXP found in places where they must not be.
- Security-sensitive NXP products are found in places where they should not be.

The security vulnerabilities in NXP products are actively and carefully managed through a reporting, evaluation, and communication process. This facilitates NXP customers in their compliance with requirements such as (see the full text in Annex 1):

- Facilitating the sharing of information about potential vulnerabilities in third-party components contained in their product including providing a contact address for the reporting of the vulnerabilities discovered in the product, with digital elements.
- Ensure that, where security patches or updates are available to address identified security issues, disseminate them without delay.

5 Beyond Annex 1

Lastly, outside of the product-security-requirements focused Annex 1, there are other process-related requirements where NXP offers support. This section highlights the most important facets.

5.1 Unique identification

Annex II of the CRA states that all products with digital elements are accompanied by the product name, type, and any additional information enabling the unique identification of the product. In the MCX N family, the EdgeLock Enclave's Trust Provisioning (TP) flow can provide a unique identity to each manufactured part. The OEM uses this to conform to this requirement of the CRA.

Also, the MCX N has a single physically unclonable function (PUF) module with four module slots, which can be configured for different privilege access. The PUF provides unique device secrets that are virtually impossible to duplicate, clone, or predict making them suitable for applications such as secure key generation and storage, device authentication, flexible key provisioning, and chip asset management.

5.2 Software Bill of Materials (SBOM)

The Software Bill of Material (SBOM) of a product lists the components in software and eases the traceability of vulnerabilities. The recital (78) of the CRA states that OEMs should draft an SBOM for their product (it does not have to be public). NXP can help OEMs in sharing the SBOM for NXP SDK software. It can be used by the OEM for their own SBOM creation and conform to this requirement of the CRA.

5.3 Security of the supply chain

The CRA emphasizes that the end product is more secure if its components and the supply chain are also well protected. NXP has extensive security expertise and addresses the security demands of its products by leveraging its heritage in highly advanced secure elements for smartcards, government e-passports, and automotive applications. The company rigorously tests its sites, systems, and processes. In addition to ensuring the integrity of its secure components, NXP has a security-conscious culture within its organization, making security part of its DNA. Choosing an NXP product to design takes the first step toward the supply chain security of the OEM product.

5.4 Manufacturer’s obligations on due diligence for integrated components

The MCX N family has been developed following a secure-by-design process with the in-house NXP EdgeLock Secure Assurance program. The MCX N has been evaluated and certified by independent third parties against EN 17927 (SESIP scheme) and PSA certified. The certificates and security target, explaining the details of the security claims in the scope of the certification, are public. All this supports OEMs with their CRA obligations, managing the risk of their supply chain, due diligence of integrated components, conformance of these components to the essential requirements, vulnerability management of the components and integration of technology functionality proportional to the specific OEM’s risk and use cases.

6 Acronyms

Table 2 lists the acronyms used in this document.

Table 2. Acronyms

Term	Definition
AES	Advanced encryption standard
CR	Component requirement
DES	Data encryption standard
ECC	Elliptic-curve cryptography
ECDH	Elliptic-curve Diffie-Hellman
ECDHE	Elliptic-curve Diffie-Hellman Ephemeral
EDR	Embedded device requirement
FR	Foundational requirement
HDR	Host device requirement
HTTP	Hypertext transfer protocol
IoT	Internet of Things
KDF	Key derivation function
MAC	Message authentication code
MQTT	Message queuing telemetry transport
NDR	Network device requirement
OEM	Original equipment manufacturer
OS	Operating system
PCR	Platform configuration register
PKI	Public key infrastructure
PRNG	Pseudo random number generator
SAR	Software application requirement
SCP	Secure channel protocol
SE	Secure element
SHA	Secure hash algorithm
SL	Security level
SP	Security primitive
TLS	Transport layer security
TRNG	True random number generator

7 Revision history

Table 3 summarizes the revisions to this document.

Table 3. Revision history

Document ID	Release date	Description
AN14687 v.1.0	20 June 2025	Initial public release

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