AN14619

One-Shunt FOC on MCX A

Rev. 2.0 — 4 December 2025

Application note

Document information

Information	Content
Keywords	AN14619, MCX A, Field-Oriented Control (FOC), Permanent Magnet Synchronous Motors (PMSM), one-shunt sample
Abstract	This application note describes the implementation of sensorless one-shunt FOC for three-phase PMSM on NXP MCX A series MCUs.

1 Introduction

This application note describes the implementation of sensorless one-shunt Field-Oriented Control (FOC) for three-phase Permanent Magnet Synchronous Motors (PMSM) on NXP MCX A series MCUs.

The MCX A series are general-purpose MCUs designed for a wide range of applications with scalable device options, low power, and intelligent peripherals. MCX A153, MCX A156, and MCX A346 represent three different MCX A series that demonstrate the one-shunt FOC methods.

This document describes the sample timing, current reconstruction, and phase shift theory. The solution is created using MCX A153, MCX A156, and MCX A346 MCU based NXP Freedom board, FRDM-MCXAxxx. It also uses another NXP Freedom board, FRDM-MC-LVPMSM, for motor control function. The document describes hardware-specific details of the PMSM FOC solution, including peripherals set up for different MCX A parts. This document also describes the demo setup and CPU loading performance.

This application note includes the demo setup for FRDM-MCXA153, FRDM-MCXA156, and FRDM-MCXA346 on NXP AppCodeHub.

- MCX A153
- MCX A156
- MCX A346

2 One-shunt FOC theory

The sensorless control software and general PMSM control theory are described in *Sensorless PMSM Field-Oriented Control* (document DRM148), including the motor mathematical model, coordinate transformation, Space Vector Pulse Width Modulation (SVPWM), and Back Electromotive Force (BEMF) observer-based sensorless algorithm. The detailed function descriptions of RTCESL for the MCX A series are available in CM33FGMCLIB and CM33FAMCLIB.

The one-shunt resistor sampling uses one sampling resistor to sample the bus current to reconstruct the motor phase current. As the sum of the three phase currents is zero, the three phase currents can be calculated using the Kirchhoff current law by sampling the bus current twice within one PWM cycle, which is suitable for cost sensitive applications.

Figure 1 shows the seven-segment SVPWM modulation method in different space-vector sectors respectively. In this method, the effective voltage vector acts symmetrically over the two PWM half-cycles and the zero vector acts on the middle and both sides of the PWM cycle.

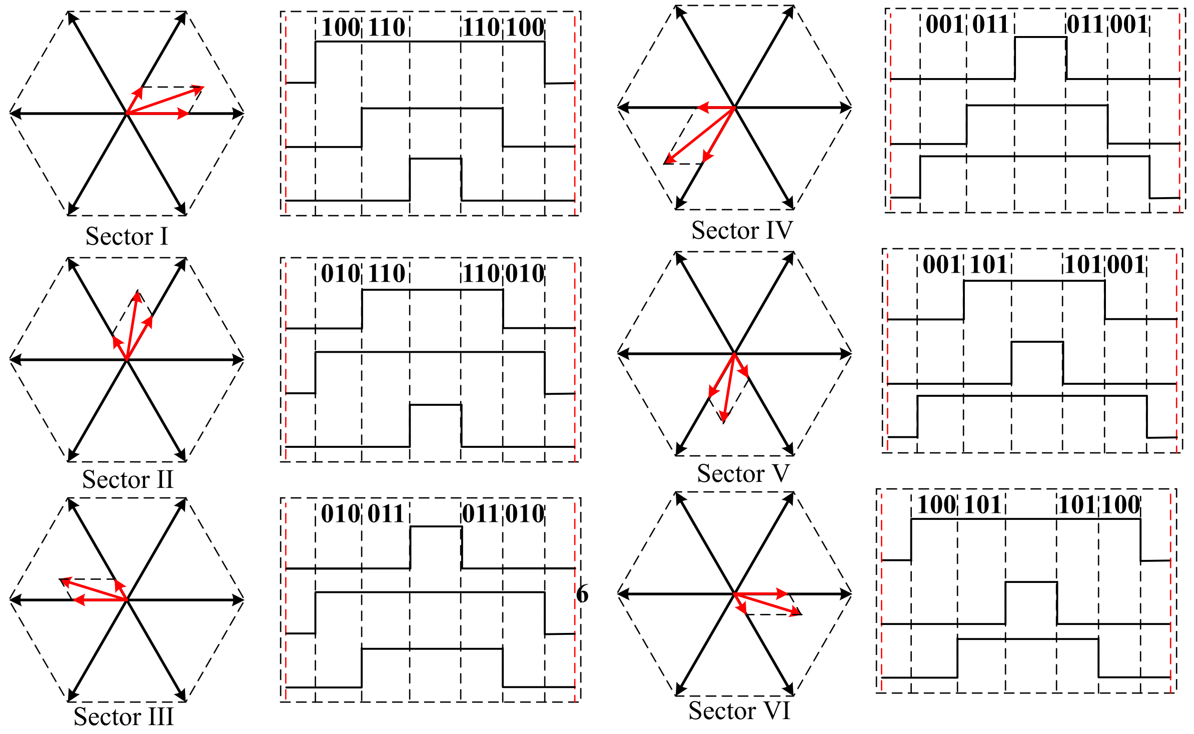

Figure 1. Seven-segment SVPWM method

Figure 2 shows the relationship between the bus current and the phase current sampled for different effective voltage vector action times.

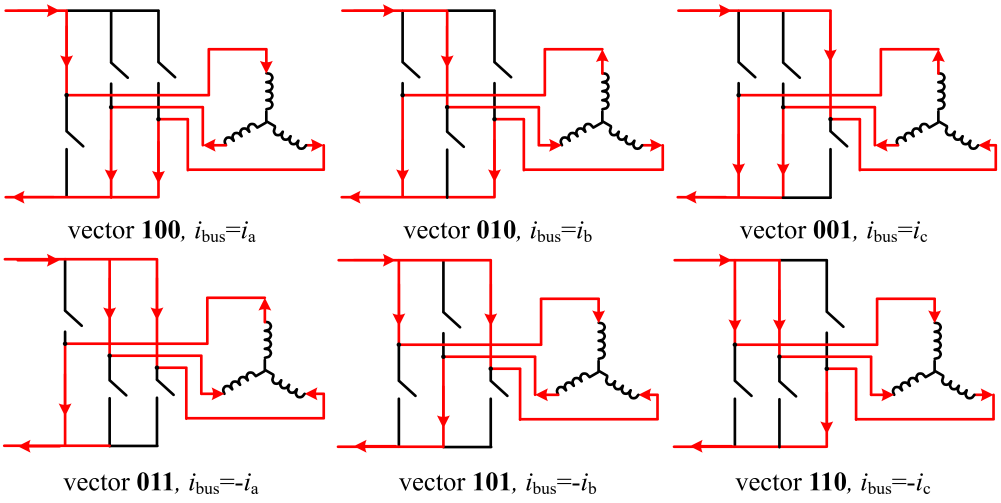
vector **100**, $i_{bus}=i_a$
vector **010**, $i_{bus}=i_b$
vector **001**, $i_{bus}=i_c$
vector **011**, $i_{bus}=-i_a$
vector **101**, $i_{bus}=-i_b$
vector **110**, $i_{bus}=-i_c$

Figure 2. Current reconstruction method in different effective voltage vector

Table 1 shows the current-reconstruction method in different sectors to reconstruct the three-phase current.

Table 1. Current reconstruction method

Sector	First current	Second current	Third current	Sector	First current	Second current	Third current
I	$i_a = i_{bus}$	$i_c = -i_{bus}$	$i_b = -i_a-i_c$	IV	$i_c = i_{bus}$	$i_a = -i_{bus}$	$i_b = -i_a-i_c$

Table 1. Current reconstruction method...*continued*

Sector	First current	Second current	Third current	Sector	First current	Second current	Third current
II	$i_b = i_{bus}$	$i_c = -i_{bus}$	$i_a = -i_b-i_c$	V	$i_c = i_{bus}$	$i_b = -i_{bus}$	$i_a = -i_b-i_c$
III	$i_b = i_{bus}$	$i_a = -i_{bus}$	$i_c = -i_a-i_b$	VI	$i_a = i_{bus}$	$i_b = -i_{bus}$	$i_c = -i_a-i_b$

When the voltage vector crosses the space-sector border or the modulation index is low, the two effective voltage vectors must be long enough for current sampling. In such situation, the shifted-PWM method is used. This method modifies the ON/OFF times of the PWM signals while preserving the duty cycles, ensuring the applied voltage vector remains unchanged.

Figure 3 takes sector 'I' as an example to show how to extend the sampling window of the voltage vector through phase shifting:

- Freezes the center PWM(PWMB).
- If needed, the edges of the PWM signals are moved away from the center, PWMA to the left and PWMC to the right.

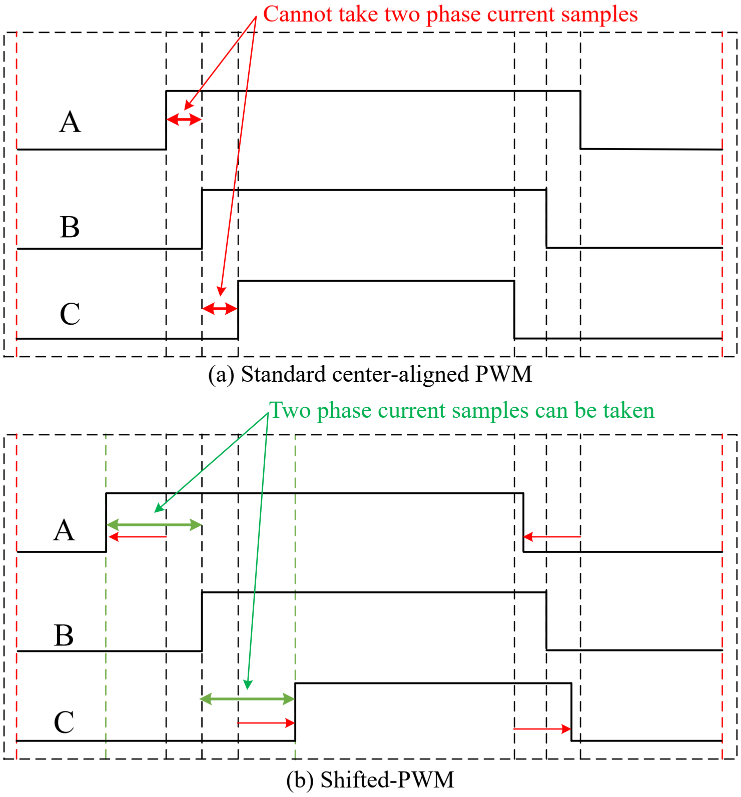
Cannot take two phase current samples
A
B
C
(a) Standard center-aligned PWM
Two phase current samples can be taken
A
B
C
(b) Shifted-PWM

Figure 3. PWM shifting principle

For more details, see the description of the GMCLIB_SvmStdShifted function in CM33FGMCLIB.

3 Hardware platform and MCU setup

The motor-control solution uses the following hardware platforms:

- FRDM-MCXAxxx board
- FRDM-MC-LVPMSM board

3.1 FRDM-MCXAxxx

The FRDM-MCXAxxx board is a design and evaluation platform based on the NXP MCX A MCU. The board is compatible with the Arduino UNO R3 boards. It can be used with a wide range of development tools, including NXP MCUXpresso IDE, IAR Embedded Workbench, and Arm Keil MDK.

To debug the MCX A MCU, the FRDM-MCXAxxx board uses an onboard (OB) debug probe, MCULink OB, which is based on another MCU.

3.2 FRDM-MC-LVPMSM board

The FRDM-MC-LVPMSM board adds motor-control capacities.

The FRDM-MC-LVPMSM board has a power supply input voltage of 24 V DC to 48 V DC with a reverse polarity protection circuitry. An auxiliary power supply of 5.5 V DC can provide power to the FRDM MCU boards. The output current reaches up to 5 A RMS. The inverter is implemented using the three-phase bridge MOSFET inverter and the three-phase MOSFET gate driver. This board measures the analog quantities (such as three-phase motor currents, DC-Bus voltage, and DC-Bus current).

3.3 Freedom motor-control development kit

Figure 4 shows a complete Freedom motor-control development.

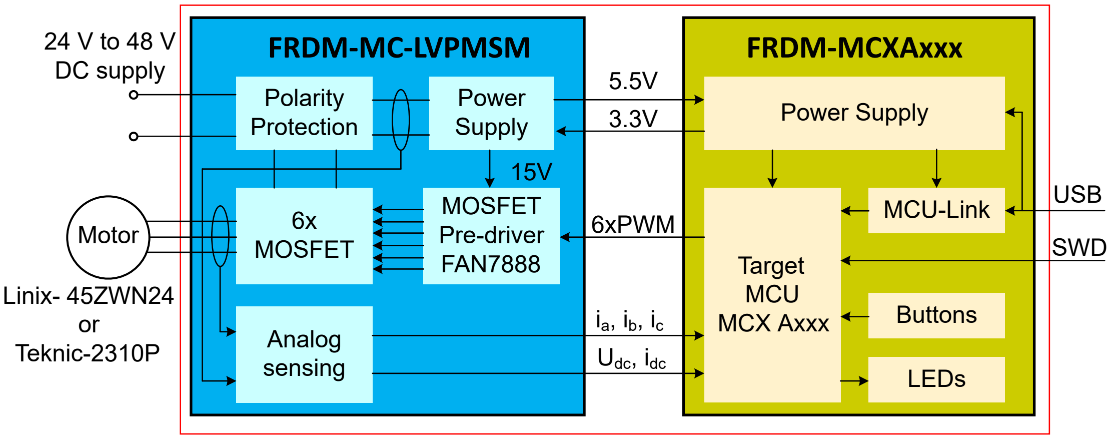

Figure 4. Freedom motor-control development platform block diagram

3.4 MCX A series device comparison

Table 2 shows the main differences in the motor-control features of different MCX A series devices.

Table 2. Differences between MCX A families

	MCX A153	MCX A156	MCX A346
Group	MCX A153, A152, A143, A142, A133, A132	MCX A156, A155, A154, A146, A145, A144	MCX A346, A345
Core	Cortex-M33 48 MHz (A14x) or 96 MHz (A15x, A13x) with 381 CoreMark (3.97 CoreMark/MHz), w/o FPU and DSP	Cortex-M33 48 MHz (A14x) or 96 MHz (A15x) with 396 CoreMark (4.12 CoreMark/MHz), with FPU and DSP	Cortex-M33 180 MHz with 741.6 CoreMark (4.12 CoreMark/MHz), with FPU and DSP

Table 2. Differences between MCX A families*...continued*

	MCX A153	MCX A156	MCX A346
Processing accelerators	No	No	MAU and SmartDMA

Memory	Up to 128 kB flash/32 kB SRAM;
	12 kB SRAMX;
	4 kB cache;
		Up to 1 MB flash/128 kB SRAM;
		12 kB SRAMX;
		4 kB cache;
			Up to 1 MB flash/256 kB SRAM;
			16 kB SRAMX;
			8 kB cache;

Advanced motor control	1*FlexPWM each with 3 submodules;
	1*eQDC;
	3*32-bit Ctimer;
	1*AOI;
		2*FlexPWM each with 3 submodules;
		2*eQDC;
		5*32-bit Ctimer;
		2*AOI;
			2*FlexPWM each with 4 submodules;
			2*eQDC;
			5*32-bit Ctimer;
			2*AOI;

Analog	1*16-bit SAR-ADC;
	2*LPCMP with 8-bit DAC;
		2*16-bit SAR-ADC;
		2*LPCMP with 8-bit DAC;
		1*12-bit DAC;
		1*OpAmp with PGA;
			4*16-bit SAR-ADC;
			3*LPCMP with 8-bit DAC;
			1*12-bit DAC;
			4*OpAmp w/o PGA;

4 Motor-control peripheral settings on MCX A series

The following section describes the peripheral settings and application timing for MCX A. A correct and precise timing is crucial in the motor-control applications. The motor-control-dedicated peripherals handle the timing and synchronization on the hardware layer. As the MCX A series MCUs use similar FlexPWM and Analog-to-Digital Converter (ADC) for motor control, the timing diagram is shown in Figure 5.

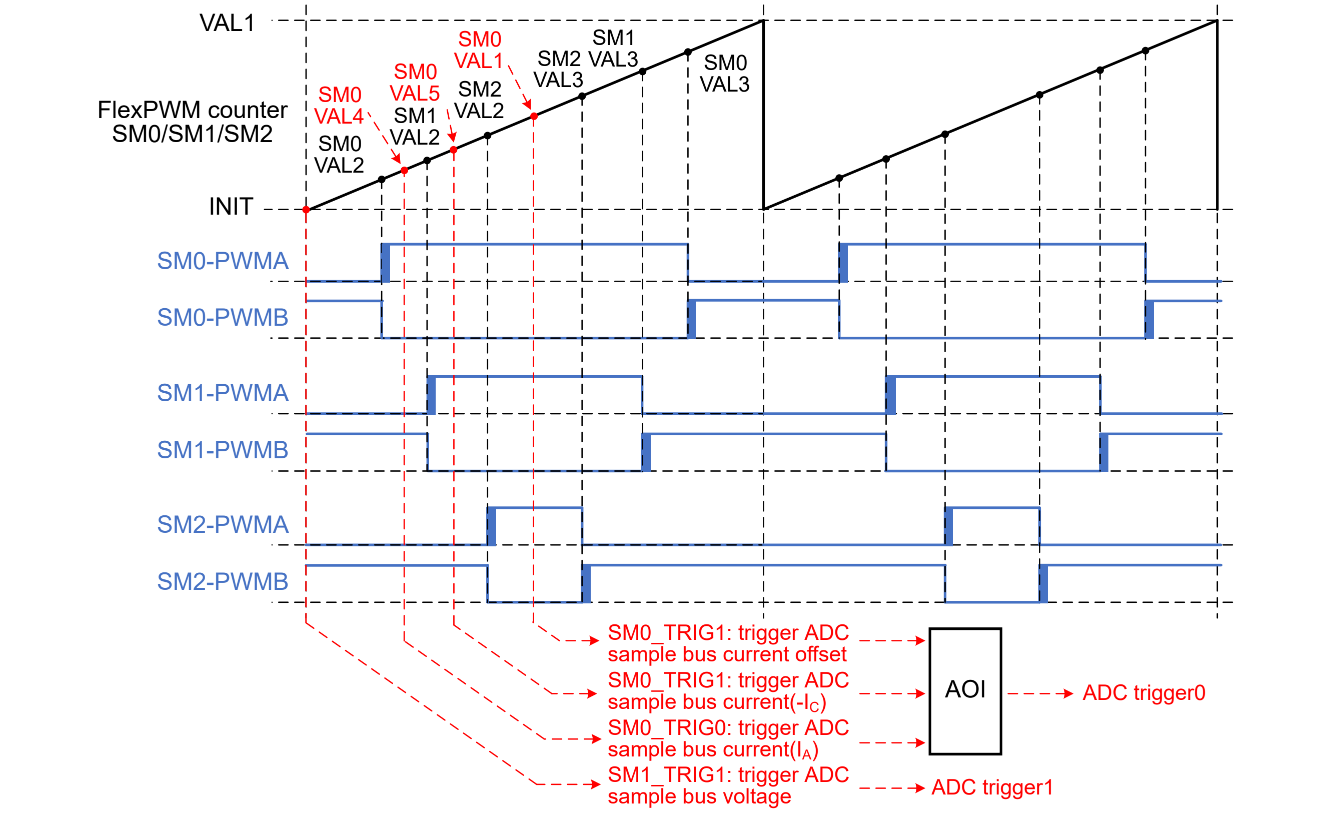
VAL1
FlexPWM counter
SM0/SM1/SM2
INIT
SM0 VAL4
SM0 VAL2
SM0 VAL5
SM1 VAL2
SM0 VAL1
SM2 VAL2
SM2 VAL3
SM1 VAL3
SM0 VAL3
SM0-PWMA
SM0-PWMB
SM1-PWMA
SM1-PWMB
SM2-PWMA
SM2-PWMB
SM0_TRIG1: trigger ADC sample bus current offset
SM0_TRIG1: trigger ADC sample bus current(-I_C)
SM0_TRIG0: trigger ADC sample bus current(I_A)
SM1_TRIG1: trigger ADC sample bus voltage
AOI
ADC trigger0
ADC trigger1

Figure 5. Hardware timing and synchronization on MCXA

The top signal shows the FlexPWM counter (SM0/SM1/SM2 counter). The dead time is inserted at the rising edge of both the top and bottom Pulse Width Modulations (PWMs). The SM0 submodule generates the master reload at every PWM cycle.

When the offset bus current sample conversion completes, it enters the ADC ISR (ADC interrupt). The FOC calculation is done in this interrupt.

4.1 Peripheral settings

The following evaluation boards are used for different MCX A device groups:

- FRDM-MCXA153 is the evaluation board for MCX A153, A152, A143, A142, A133, and A132 devices.
- FRDM-MCXA156 is the evaluation board for MCX A156, A155, A154, A146, A145, and A144 devices.
- FRDM-MCXA346 is the evaluation board for MCX A346 and A345 devices.

The subsections that follow describe the peripherals used for motor control on the MCX A. There are three submodules from the FlexPWM used for the 6-channel PWM generation. A 12-bit ADC is used for the phase current and DC-bus voltage measurement. The FlexPWM and ADC are synchronized using submodule 0 from the FlexPWM.

4.1.1 System Clock Generator (SCG)

The SCG generates and controls the clocks of various modules in the design of the MCX A series. This module uses the available clock sources to generate the clock roots.

Motor-control applications on the MCX A series rely on the Fast Internal Reference Clock (FIRC) as the primary clock source. The configuration varies slightly across device groups, as described below.

MCX A153 and MCX A156 devices

- The FIRC boots up to 192 MHz, enabling high-performance operation.
- The Arm core operates at a maximum frequency of 96 MHz.
- The FlexPWM module supports operation up to 192 MHz.

To set up clock, follow the steps below:

1. Boost the FIRC to a relatively low frequency.
2. Apply a suitable divider factor to boost the frequency gradually to 192 MHz, at which the Arm core can work normally.
3. Once the core clock is stabilized, set the other peripheral clock source divider factor.

MCX A346 device

- The FIRC boots up to 180 MHz.
- Both the Arm core and FlexPWM operate at the clock frequency of 180 MHz.

Table 3 shows the clock sources for the peripherals used for motor control.

Table 3. Clock source for motor-control peripherals

	MCX A153		**MCX A156**		**MCX A346**	
Module	Frequency/MHz	Source	Frequency/MHz	Source	Frequency/MHz	Source
fro_hf	192	FIRC	192	FIRC	180	FIRC
main clock	192	fro_hf	192	fro_hf	180	fro_hf
Core clock	96	main_clk/2	96	main_clk/2	180	main_clk
FlexPWM	192	main_clk	192	main_clk	180	main_clk
ADC	48	fro_hf/3	48	fro_hf/3	60	fro_hf/3
Ctimer	96	fro_hf/2	96	fro_hf/2	180	fro_hf
CMP	48	fro_hf/3	48	fro_hf/3	60	fro_hf/3
LUPART	12	fro_12m	12	fro_12m	12	fro_12m

4.1.2 PWM generation using eFlexPWM0

In motor-control applications on the MCX A series, the FlexPWM0 module is used to generate six PWM outputs from three submodules (SM0, SM1, and SM2) for 3-phase motor control. It is clocked from the system clock.

- Submodule synchronization: Submodule 0 generates the master reload signal for each PWM cycle. Submodules 1 and 2 receive their clocks from submodule 0. The counters at submodules 1 and 2 are synchronized with the master reload signal from submodule 0.
- PWM signal control: The match events of compare VAL2 (PWM23 on) and VAL3 (PWM23 off) control the rising and falling edges of PWMA in a submodule. PWMB is configured as the complementary output to PWMA.
- Dead time insertion: The dead time insertion is enabled. The user defines the dead time duration in the M1_PWM_DEADTIME macro.
- Trigger output: Each submodule can generate two trigger outputs, as shown in Figure 6:
  - TRIG0 is generated at the match event of compare VAL0, VAL2, and VAL4.
  - TRIG1 is generated at the match event of compare VAL1, VAL3, and VAL5.

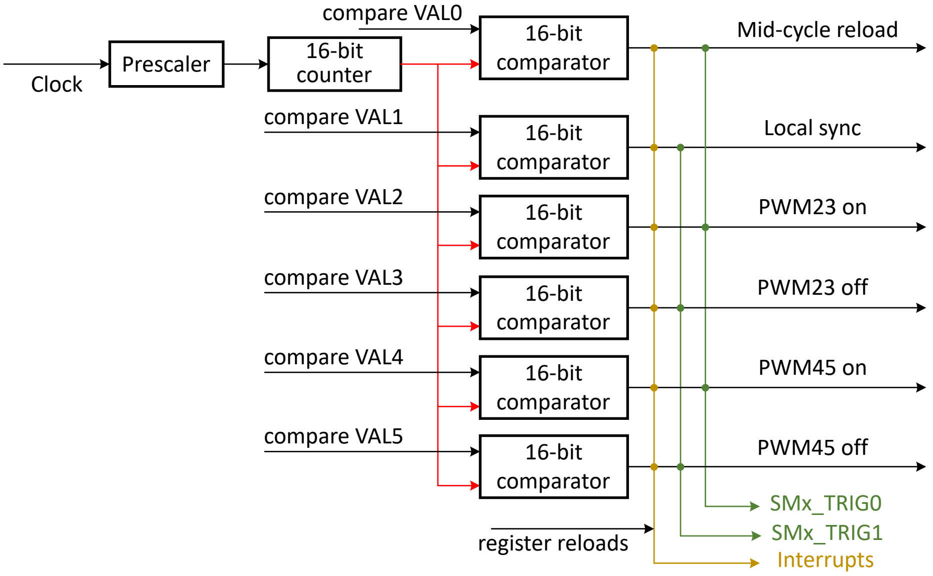

Figure 6. Match event in a submodule

- Fault handling: The fault mode is enabled for channels A and B at submodules 0, 1, and 2 with automatic fault clearing. The PWM outputs are reenabled at the first PWM reload, after the fault input is cleared.
- PWM period configuration: The PWM period is determined by the time that it takes the counter to count from INIT to VAL1.

4.1.3 AND-OR-Invert (AOI)

The AOI module supports the generation of a configurable number of EVENT signals. Each AOI instance has 4 channels, and each channel has:

- 4 associated AOI inputs - An, Bn, Cn, and Dn
- 1 EVENT output

Each channel has 4 product terms (PT0-PT3). There are 4 input configurations (PTx_AC, PTx_BC, PTx_CC, and PTx_DC) for 4 inputs of a channel (An, Bn, Cn, Dn) in a product term, respectively. The input configuration can select from force 0, force 1, pass input, and complement input as an output. The output of a product term is the logic AND result of 4 input configurations. The EVENT output of a channel is the logic OR result of 4 product terms of this channel. Figure 7 shows the detailed function diagram.

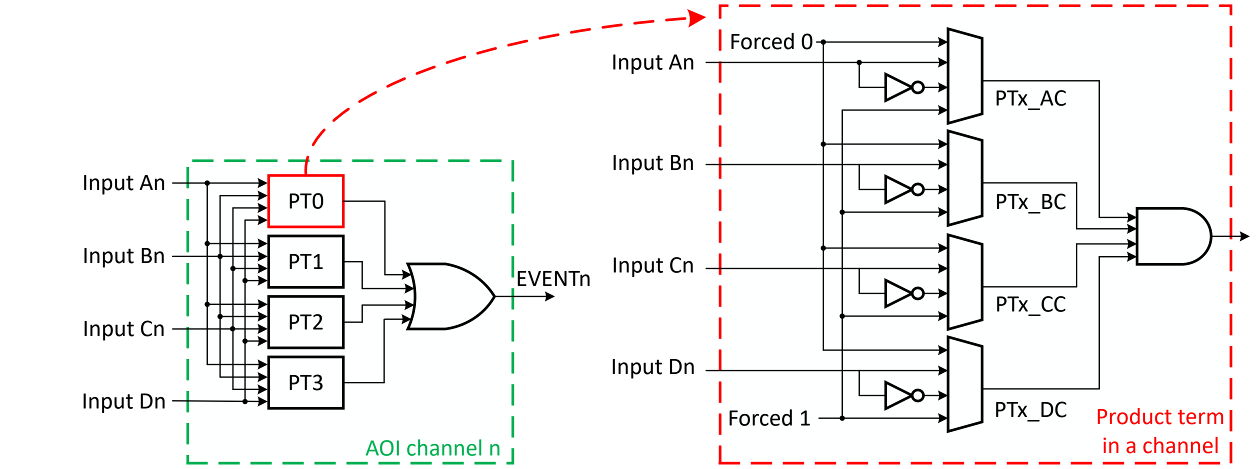

Figure 7. Function diagram of an AOI channel

The ADC channel used for the sample bus current must be triggered 3 times in a PWM cycle. The AOI channel 0 makes a logic OR result of PWM0_SM0_TRIG0 and PWM0_SM0_TRIG1 and triggers the ADC with the EVENT 0 output through INPUTMUX.

4.1.4 Peripheral trigger control - INPUTMUX

The Input Multiplexing (INPUTMUX) module provides signal routing options for internal peripherals. Some peripheral inputs are multiplexed to multiple input sources. The sources can be external pins, interrupts, output signals of other peripherals, or other internal signals.

In the context of motor-control applications, the following signal routing configurations are used:

- Select PWM0_SM0_OUT_TRIG0 as the source of AOI0_INPUT0.
- Select PWM0_SM0_OUT_TRIG1 as the source of AOI0_INPUT1.
- Select AOI0_OUT0 as the source of ADC0_TRIG0.
- Select PWM0_SM1_OUT_TRIG1 as the source of ADC0_TRIG1.
- Select CMP1_OUT to connect to PWM0_FAULT0.

4.1.5 Analog sensing - ADC0

The ADC0 module is used to sample the bus current and voltage. It operates as a 12 bit with the single-ended conversion and hardware trigger selected.

The following command buffers are configured in ADC0 to sample bus current during the PWM cycle:

- CMD2-CMD4 are used to sample the bus current for 3 timers at different points of a PWM cycle.
- CMD3 and CMD4 are configured to wait for the trigger assertion before execution.

Wait states are added before the command until the active trigger is asserted again. The trigger and command sequence is shown in Figure 8.

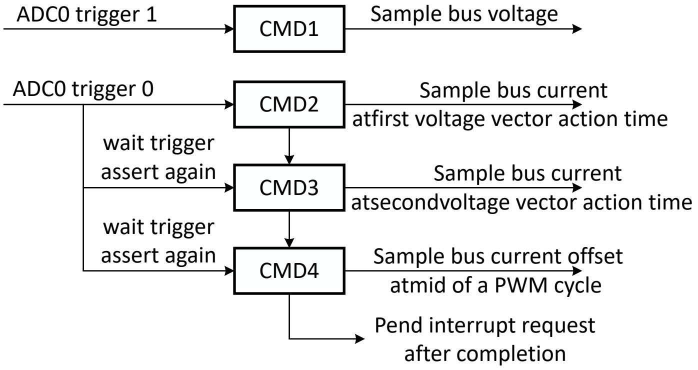

Figure 8. ADC trigger and CMD assignment

4.1.6 Slow-loop interrupt generation - CTIMER0

The Counter Timer0 (CTIMER0) module is used to generate the slow-loop interrupt. The slow loop is usually 10 times slower than the fast loop. The speed-loop frequency is set in the M1_SPEED_LOOP_FREQ macro and equals to 1000 Hz.

To configure the slow-loop interrupt, follow the steps below:

1. Set the match value register MATCH3 according to the slow-loop frequency.
2. When the counter value is equal to MATCH3, the counter initializes to 0, and generates an interrupt request.

4.1.7 Hardware protection - CMP0

The Comparator (CMP) module provides a circuit to compare the bus current sample signal with the internal 8-bit DAC output value. It generates a trigger to lock the PWM output if the bus current is high.

4.1.8 FreeMASTER communication - LPUART

The Low-Power Universal Asynchronous Receiver and Transmitter (LPUART) is used for the FreeMASTER communication between the MCU board and the PC. The baud rate is set to 115,200 bit/s. The receiver and transmitter are both enabled to support data transfer with FreeMASTER.

5 Demo setup and CPU loading performance

This section describes the operation and performance of the demo applications.

The LINIX 45ZWN24-40 motor is used in demos. The details about the motor parameters and the software structure are described in the following documents:

- *MCUXpresso SDK Field-Oriented Control of 3-Phase PMSM and BLDC Motors (FRDMMCXA153)* (document UG10245)
- *MCUXpresso SDK Field-Oriented Control of 3-Phase PMSM and BLDC Motors (FRDMMCXA156)* (document UG10247)
- *MCUXpresso SDK Field-Oriented Control of 3-Phase PMSM and BLDC Motors (FRDMMCXA346)* (document UG10248)

5.1 Demo setup

This section describes how to set up the demo.

5.1.1 Project setup in MCUXpresso IDE

You can clone the demo code from the Application Code Hub directly in the MCUXpresso IDE by performing the following steps:

1. Open the MCUXpresso IDE and select *Import from Application Code Hub* in the quick start panel.
2. Search for the desired demo by entering its name directly or by selecting the tags you are interested in. Open the project, click the *GitHub link*, and then click *Next*.
3. Select the *main* branch and then click *Next*.
4. Select your local path for the repository in the *Destination->Directory:* window. The MCUXpresso IDE then clones the repository to the path that you selected. Click *Next* after the clone process.
5. Select *Import existing Eclipse projects* in the wizard for the project import window and then click *Next*.
6. Select the project from the repository (only one project in this repository) and then click *Finish*.

The project contains two build configurations:

- *Debug*
- *Debug_SRAMX*

The *Debug_SRAMX* configuration has a standalone link script to allocate frequently called code in the SRAMX to improve performance.

To switch configurations, right-click the project name in the *Project Explorer* window and select *Properties* to open the properties window. Open *Manage Configurations*, select the desired configuration, and then click *Set Active*.

5.1.2 Hardware setup

To set up the hardware for running the demo, follow the steps below:

1. Connect the FRDM-MC-LVPMSM shield to the J1-J4 Arduino connectors on the FRDM-MCXAxxx board.
2. Connect the 3-phase motor wire to the J7 connector on the FRDM-MC-LVPMSM board according to the phase sequence: (white to wide-phase A, blue to wide-phase B, and green to wide-phase C).
3. Power the FRDM-MC-LVPMSM board using a 24-V adapter.
4. Use a USB-Type C cable to connect the PC to the FRDM-MCXAxxx board connector marked as MCU-Link.
5. Download the code using the debug button in the toolbar after the compiler.
6. In the *Debug As* dialog, select either CMSIS-DAP or J-Link, depending on the firmware installed on the onboard debugger.

5.1.3 Running the demo

To run or stop the motor, press the *SW2* button on the FRDM-MCXAxxx board.

Alternatively, you can also use the FreeMASTER project in the code package to control the motor, adjust the rotor speed, and obverse the speed or other values.

5.2 CPU loading performance of the demo

Table 4 compares CPU loading performance across different MCX devices and configurations:

Table 4. CPU loading performance of the demo

Fast-loop interval	125 µs/8 kHz		
Slow-loop interval	1000 µs/1 kHz		
	MCX A153	MCX A156	MCX A346

Table 4. CPU loading performance of the demo*...continued*

RTCESL	CM33NODSP_4.8_MCUX (Fixed-point fraction library)		CM33F_4.8.1_MCUX (Single-precision float library)		CM33F_4.8.1_MCUX (Single-precision float library)	
Core frequency/MHz	96		96		180	
Cache size/kB	4		4		8	
SRAMX0 size/kB	8		8		8	
Configuration	Debug	Debug_SRAMX	Debug	Debug_SRAMX	Debug	Debug_SRAMX
Fast loop cycles	2824	2043	2203	1509	2558	1481
Fast loop time/μs	29.4	21.3	22.9	15.7	14.2	8.2
Fast loop loading	23.5 %	17.0 %	18.4 %	12.6 %	11.4 %	6.6 %
Slow loop cycles	383	254	310	183	337	173
Slow loop time/μs	4.0	2.6	3.2	1.9	1.9	1.0
Slow loop loading	0.40 %	0.26 %	0.32 %	0.19 %	0.19 %	0.10 %

6 Acronyms

Table 5 lists the acronyms used in this document.

Table 5. Acronyms

Term	Description
ADC	Analog-to-Digital Converter
BEMF	Back Electromotive Force
AOI	AND-OR-Invert Logic
CMP	Comparator
CTIMER	Counter Timer
FIRC	Fast Internal Reference Clock
FOC	Field-Oriented Control
INPUTMUX	Input Multiplexing Module
ISR	Interrupt Service Routine
LPUART	Low-Power Universal Asynchronous Receiver/Transmitter
PMSM	Permanent Magnet Synchronous Motor
PWM	Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation

7 Related documentation

Table 6 lists the references used to supplement this document.

Table 6. Related documentation/resources

Document	Link/how to access
Sensorless PMSM Field-Oriented Control (document DRM148)	DRM148

Table 6. Related documentation/resources*...continued*

Document	Link/how to access
MCX A153, A152, A143, A142, A133, A132 Reference Manual (document MCXAP64M96FS3RM)	MCXAP64M96FS3RM
MCXA153, A152, A143, A142, A133, A132 Data Sheet (document MCXAP64M96FS3)	MCXAP64M96FS3
MCXA156, A155, A154, A146, A145, A144 Reference Manual (document MCXAP100M96FS6RM)	MCXAP100M96FS6RM
MCXA156, A155, A154, A146, A145, A144 Data Sheet (document MCXAP100M96FS6)	MCXAP100M96FS6
MCX A345 and MCX A346 Reference Manual [document MCXAP144M240F60RM]	MCXAP144M240F60RM
Mixed-signal Arm Cortex-M33 MCU with 180 MHz, up to 1024 KB Flash (document MCXA345/346 Product Data Sheet)	MCXA345/346 Product Data Sheet
FRDM-MCXA153 Board User Manual (document UM12286)	UM12286
FRDM-MCXA156 Board User Manual (document UM12121)	UM12121
FRDM-MCXA346 Board User Manual (document UM12348)	UM12348
For software information, refer the following:	
MCUXpresso SDK Field-Oriented Control of 3-Phase PMSM and BLDC Motors (FRDMMCXA153) (document UG10245)	UG10245
MCUXpresso SDK Field-Oriented Control of 3-Phase PMSM and BLDC Motors (FRDMMCXA156) (document UG10247)	UG10247
For more information about the FRDM-MC-LVPMSM board, refer the following:	
MCUXpresso SDK Field-Oriented Control of 3-Phase PMSM and BLDC Motors (FRDMMCXA346) (document UG10248)	UG10248
Freedom FRDM-MC-LVPMSM Development Platform User's Guide (document FRDMLVPMSMUG)	FRDMLVPMSMUG

Note: *Some of the documents listed above are available only under a Non-Disclosure Agreement (NDA). To access such documents, contact your local NXP Field Applications Engineer (FAE) or sales representative.*

8 Revision history

Table 7. Revision history

Document ID	Release date	Description
AN14619 v.2.0	4 December 2025	Made several technical and editorial changes
AN14619 v.1.0	28 May 2025	Initial version

Legal information

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