AN14518

Crystal Oscillator Design Guide

Rev. 4.0 — 9 September 2025 **Application note**

Document information

Information	Content
Keywords	Pierce oscillator, crystal oscillator, drive level, loading capacitors, negative resistance, XTAL, XTAL start-up
Abstract	This document covers the design process for the XTAL oscillator in NFC Reader circuits. In this context, design refers to the selection of the correct XTAL unit and its implementation into the user design.

1 Introduction

This document explains what considerations need to be made when designing and tuning the **crystal oscillator** (referred to as "**XTAL**") for NFC Design. It also provides instructions on how to check all important parameters which may influence the XTAL start-up and stability. The document also includes a list of recommended XTALs for each NXP product.

Choosing the correct XTAL is only one aspect to be considered. For proper functionality, the PCB layout and other factors such as load capacitance and drive level also have to be considered.

Note: *In this document, the acronym* ***NFCC*** *(NFC controller) is used to refer to an NFC Integrated Circuit (for example: PN7642).*

2 XTAL design – Flowchart

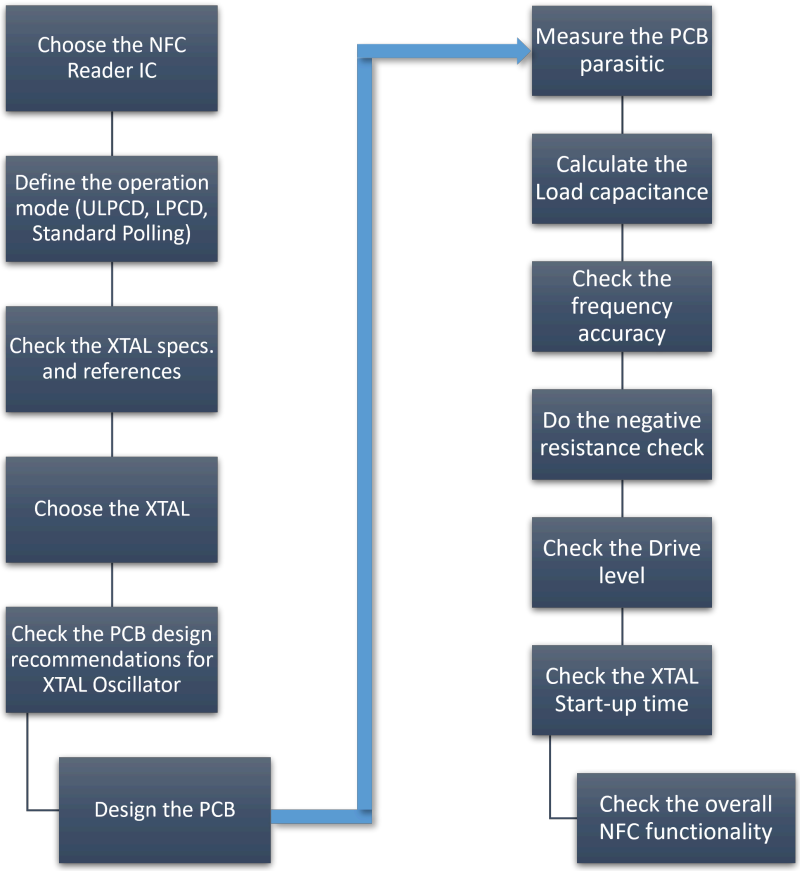

Figure 1. Simplified design flowchart

3 XTAL oscillator

3.1 Theory

NXP NFC controllers/frontends use a Pierce oscillator structure which consists of two parts: An active part which is inside the NFCC and a passive part which is connected externally. The active part is an inverter amplifier which is represented as transconductance "*gm*". The passive part consists of an XTAL oscillator (XTAL) and two loading capacitors (CL1 and CL2). Find the basic structure in Figure 2.

As shown in Figure 2, there are also parasitic capacitances which have to be considered during the PCB design and the load capacitance calculation (see Section 3.2 and Section 6).

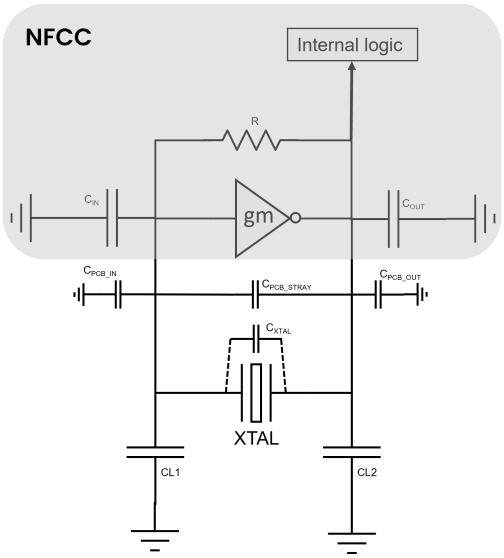

Figure 2. Pierce oscillator in NFC Controller

The crucial part of the Pierce oscillator is a quartz oscillator (XTAL) which contains a crystal element enabling oscillation at certain frequency. For NFC, the frequency is typically **27.12MHz.** The electrical model of the XTAL is shown in Figure 3:

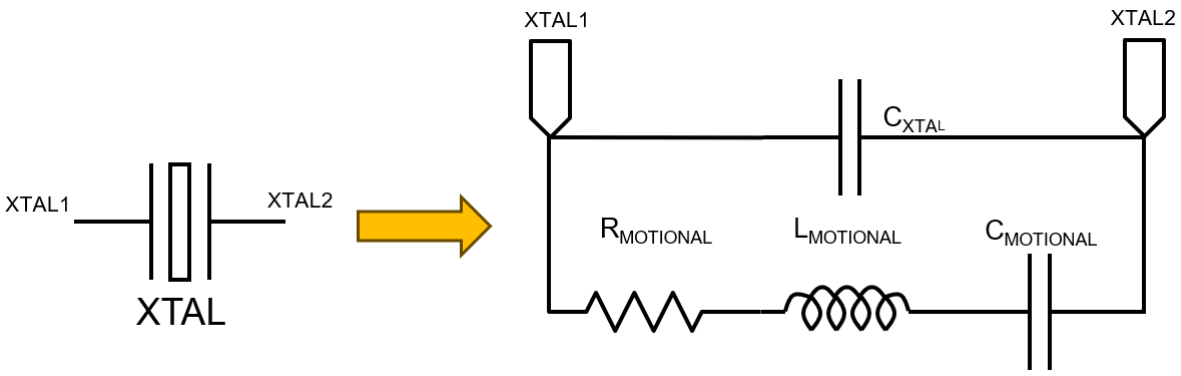

Figure 3. XTAL Model

- $R_{MOTIONAL}$ → Motional Resistance of the XTAL (Equivalent Series Resistance known as **ESR**)

- $L_{MOTIONAL}$ → Motional Inductance of the XTAL
- $C_{MOTIONAL}$ → Motional Capacitance of the XTAL
- C_{XTAL} → Shunt Capacitance of the XTAL

3.2 Load capacitance

The XTAL load capacitance is one of the crucial parameters in the oscillator design which defines the oscillation frequency. The goal is to match the overall capacitance of the design (including external load capacitors and all parasitic capacitances) to the nominal load capacitance defined by the XTAL manufacturer.

For example, if the nominal load capacitance of the XTAL defined by the manufacturer is 10 pF, then the PCB design and the selection of all external components should ideally be done in such way that the overall capacitance connected to the XTAL equals 10 pF.

See the “capacitive” Pierce oscillator model in Figure 4. This model includes all parasitics that might influence the final load capacitance connected to the XTAL.

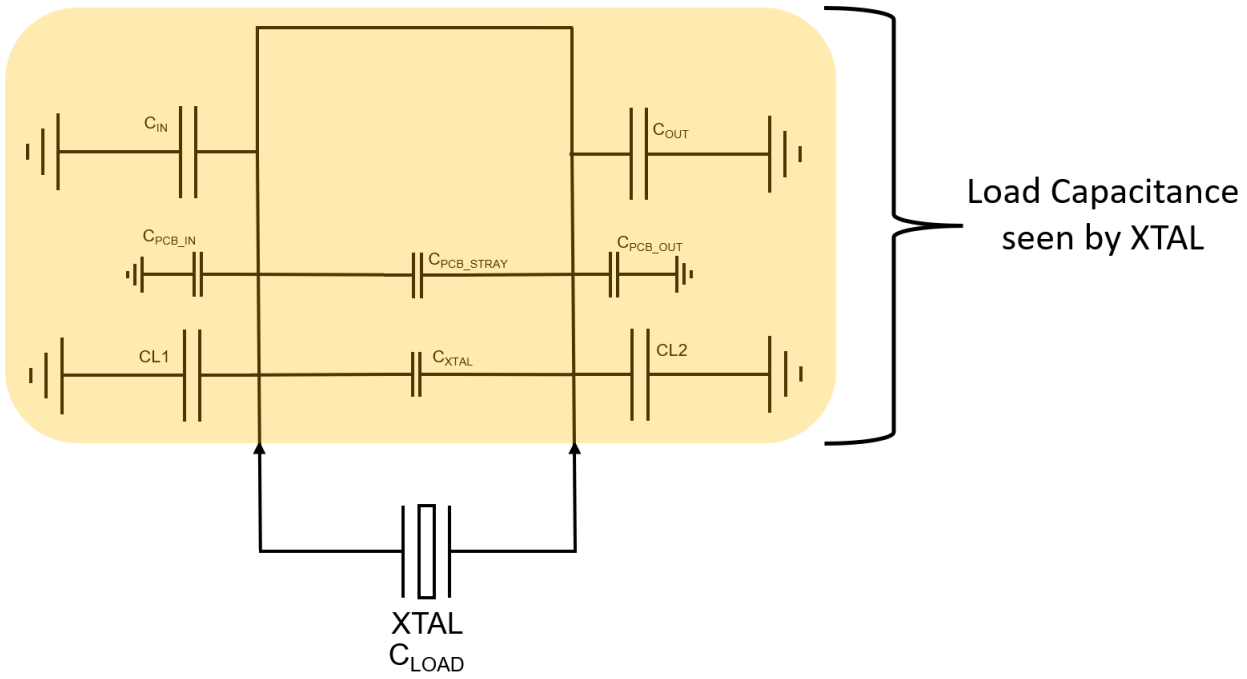

Figure 4. XTAL Load Capacitance model

- C_{LOAD} → Nominal Load Capacitance given by the XTAL manufacturer
- C_{L1} and C_{L2} → External loading capacitors
- C_{XTAL} → XTAL Shunt capacitance
- C_{PCB_STRAY} → Stray capacitance of the PCB
- C_{PCB_IN} and C_{PCB_OUT} → Parasitic capacitance of the input and output PCB traces
- C_{IN} and C_{OUT} → Capacitance of the NFC controller XTAL input and output pins

3.2.1 XTAL external load capacitors

For the adjustment of the load capacitance connected to XTAL, there are two external capacitors used, C_{L1} and C_{L2}. Their values can be calculated using the following formula:

$$C_{LOAD} = \frac{(C_{IN}+C_{PCB\_IN}+C_{L1})*(C_{OUT}+C_{PCB\_OUT}+C_{L2})}{(C_{IN}+C_{PCB\_IN}+C_{L1})+(C_{OUT}+C_{PCB\_OUT}+C_{L2})} + (C_{PCB\_STRAY} + C_{XTAL})\ (pF)$$

Figure 5. External load capacitance - formula

***Note**: The value of the external loading capacitors can be calculated using the NXP Crystal Oscillator Calculator (Section 4).*

The C_{LOAD} and C_{XTAL} can be extracted from the XTAL data sheet. The C_{IN} and C_{OUT} can be extracted from the NFC controller data sheet.

It is recommended to measure the remaining capacitance using a Vector Network Analyzer directly on the PCB. Find recommendations for the VNA settings below:

- Set the center frequency 27.12 MHz
- Set the span frequency 100kHz
- Set VNA power -10 dBm
- Use, for example, the "pin header" probe and calibration kit as shown in Figure 6.
  ***Note:** Do not touch the PCB and the GND of coax during the measurement.*
- Do the "corelation" test → Section 3.2.1.1.

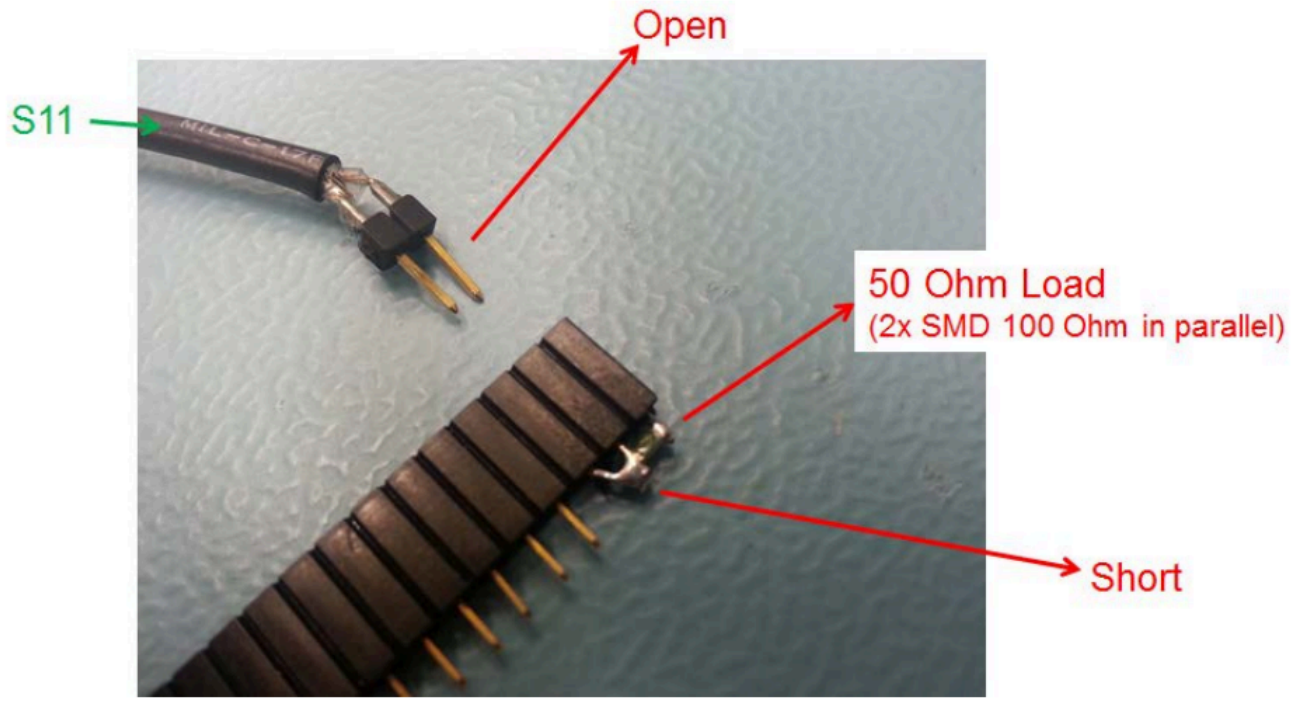

Figure 6. "Pin header" probe + calibration kit

- Measure the parasitic capacitance on the PCB as shown in Figure 7. For optimal measurement results, place the probes as close as possible to the XTAL pads.
- Based on the results obtained, the following parameters can be defined.
  - XTAL_CLK1 to GND → **C_{PCB_IN}**
    - **Note:***Probe the coax center conductor to XTAL_CLK1 and Coax GND to XTAL GND*
  - XTAL_CLK2 to GND → **C_{PCB_OUT}**
    - **Note:***Probe the coax center conductor to XTAL_CLK2 and Coax GND to XTAL GND*
  - XTAL_CLK1 to XTAL_CLK2 → **C_{PCB_STRAY}**

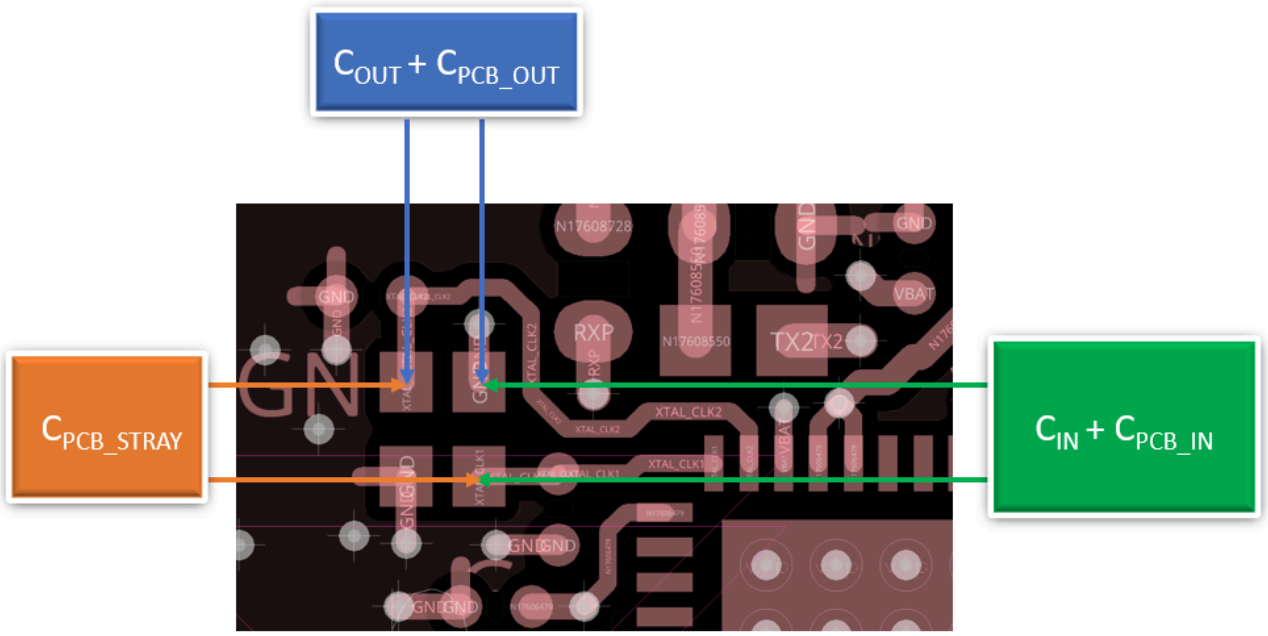

Figure 7. Parasitic capacitance measurement

For this measurement, the XTAL, NFC controller and external load capacitors have to be removed from the PCB. The PCB must not be powered.

3.2.1.1 Measurement of the known standard

Before the PCB measurements, it is recommended to measure a known standard, which is for example a 2.2 pF capacitor with a tolerance max. 2%. This helps to indicate a “delta” of used measurement setup.

See an example in Table 1.

Table 1. Measurement of the known standard

Nominal value of capacitor (pF)	2.2	2.2	2.2
Measured value of capacitor (pF)	1.73	1.63	1.78

Based on the measurements in Table 1. The delta between the nominal and measured value is approx. **0.49 pF**.

So, if the VNA shows the PCB capacintance, e.g., 0.5 pF. Then the real value is approx. **1 pF** (0.5 pF + 0.49 pF).

See the examples of two NXP PCBs in Section 3.2.1.2 and Section 3.2.1.3.

3.2.1.2 Parasitic measurement - PN7160 PCB (OM27160)

Table 2. Parasitic measurement - PN7160 EVK PCB

C_{PCB_IN} (pF)	C_{PCB_OUT} (pF)	C_{PCB_STRAY} (pF)
1.19	1.31	1.39

3.2.1.3 Parasitic measurement - PN7642 PCB (OM27642)

Table 3. Parasitic measurement - PN7642 EVK PCB

C_{PCB_IN} (pF)	C_{PCB_OUT} (pF)	C_{PCB_STRAY} (pF)
1.13	1.29	1.12

3.3 Frequency accuracy

In NFC systems, the carrier frequency is 13.56 MHz. The carrier frequency is based on the clock signal generated by the XTAL oscillator. Therefore, If the carrier frequency is **13.56 MHz**, the XTAL oscillator should generate exactly **27.12 MHz**. The signal is then divided by two and directly used for the carrier wave generation of the NFCC TX driver.

As the XTAL is a sensitive component, its output frequency can be influenced by temperature changes and the tolerances of every component in the PCB design. Therefore, regulatory authorities such as the FCC, ETSI, KCC, and ISO, allow an offset to the carrier frequency in *ppm* (parts per million). Find some examples below:

- FCC → ± 100ppm
- KCC → ± 100ppm
- ISO 14443 → ± 516 ppm
- FeliCa global → ± 50 ppm

Note: *Always check with a standardization expert for the actual limits.*

3.3.1 Frequency accuracy - check

The frequency accuracy (pullability) is given in ppm. Ideally, if the capacitance connected to the XTAL matches with the nominal XTAL capacitance, the ppm value is 0.

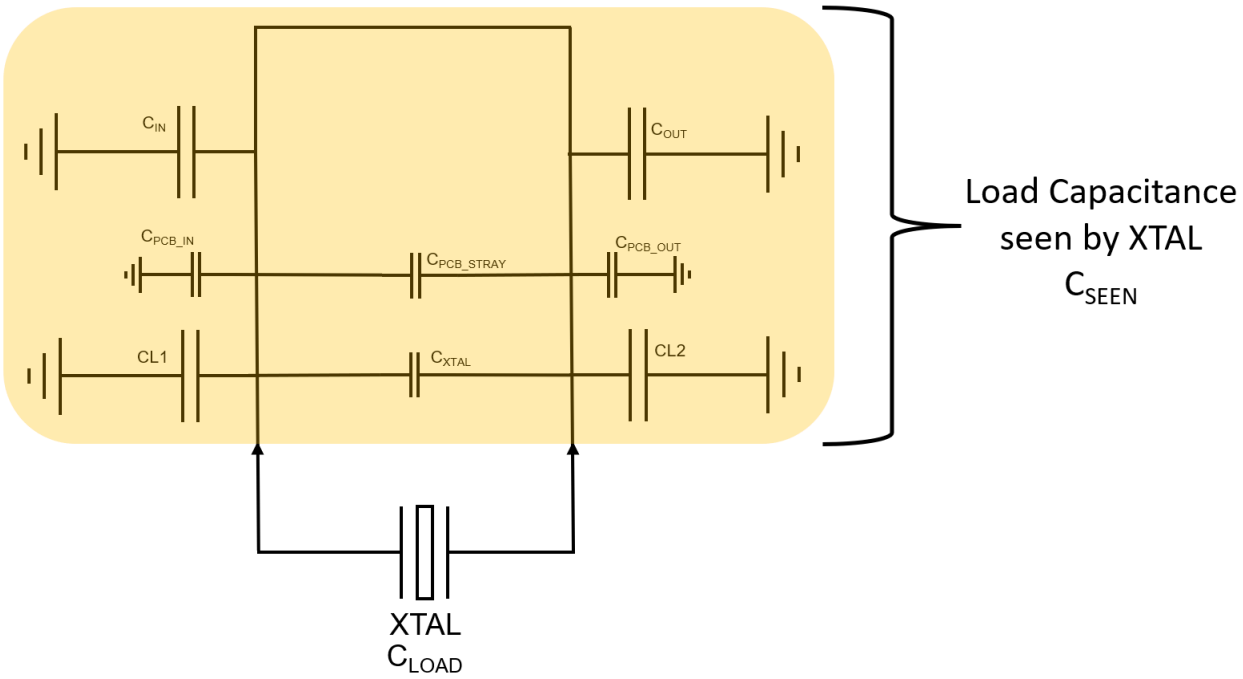

Figure 8. Load capacitance connected to the XTAL

The target is $\mathbf{C_{LOAD} = C_{SEEN}}$, but sometimes, for example, due to faster start-up time or an increase of the negative resistance absolute value, it can be necessary to slightly detune the XTAL,

The pullability can be calculated with the following formula:

$$ppm = \frac{C_m*(C_{LOAD}-C_{SEEN})}{2*C_{LOAD}*C_{SEEN}} * 10^6$$

Figure 9. XTAL pullability - formula

***Note**: The value of the pullability can be calculated using the NXP Crystal Oscillator Calculator (Section 4).*

See an example of the ppm and loading capacitance connected to the XTAL in Figure 10. The calculation has performed for an XTAL with nominal C_{LOAD} = 10 pF.

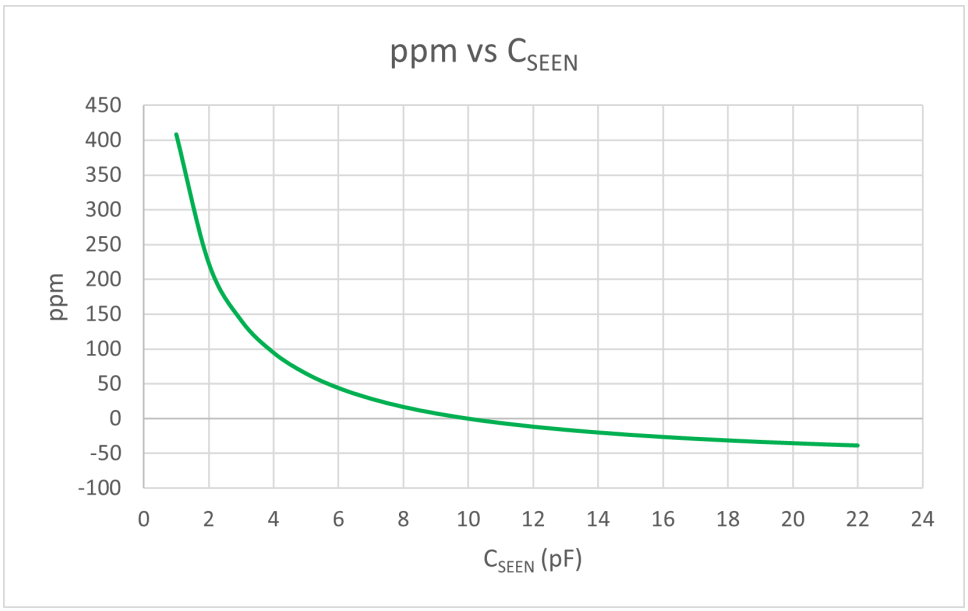

Figure 10. ppm over loading capacitance connected to the XTAL

The direct measurement of the XTAL frequency might not be accurate when a probe of a scope or spectrum analyzer is connected to the oscillator circuit as it adds an additional load. To minimize the inaccuracy of the measurement, an "indirect" measurement approach can be used for the RF carrier frequency .

Theoretically, the **frequency of the RF Carrier wave is half of the XTAL Oscillator loaded frequency** → 2 * $f_c = f_{xtal}$. Therefore, users can perform a simple test with a scope or spectrum analyzer to check the RF Field and its frequency. The carrier frequency shall be within in the limits and tolerances described in Section 3.3.

The measurement can be performed with either:

- a suitable scope with a high sample rate and FFT support, or
- a spectrum analyzer.

Find the measurement setup in Figure 11.

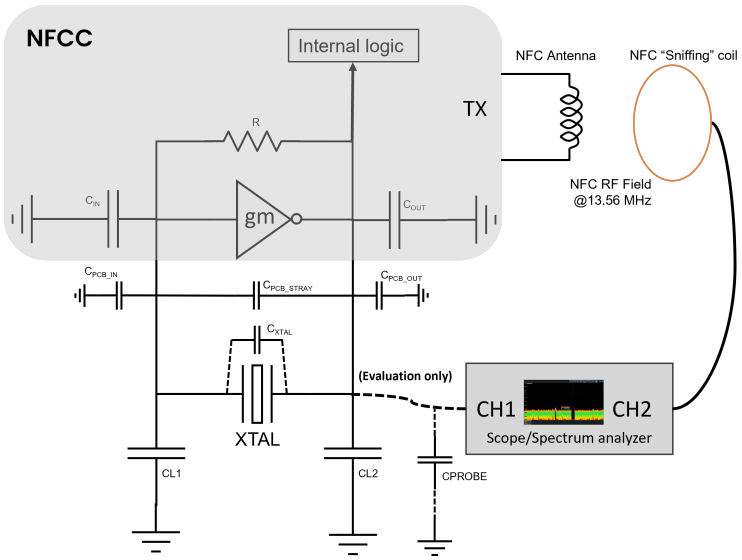

Figure 11. Measurement setup - Block diagram

Note: *For the final measurement, the CH1 must be disconnected.*

For the RF signal sniffing, a basic loop from the scope probe can be used as shown in Figure 12.

Figure 12. Measurement setup

The measurement is performed with a continuous RF_ON signal. The frequency of the radiated carrier frequency is measured.

See an example of the measurement in Figure 13, the following FFT settings were used:

- Center frequency → 13.56 MHz
- Frequency span → 50 kHz
- Resolution BW → 500 Hz
- Window type → Blackman Harris

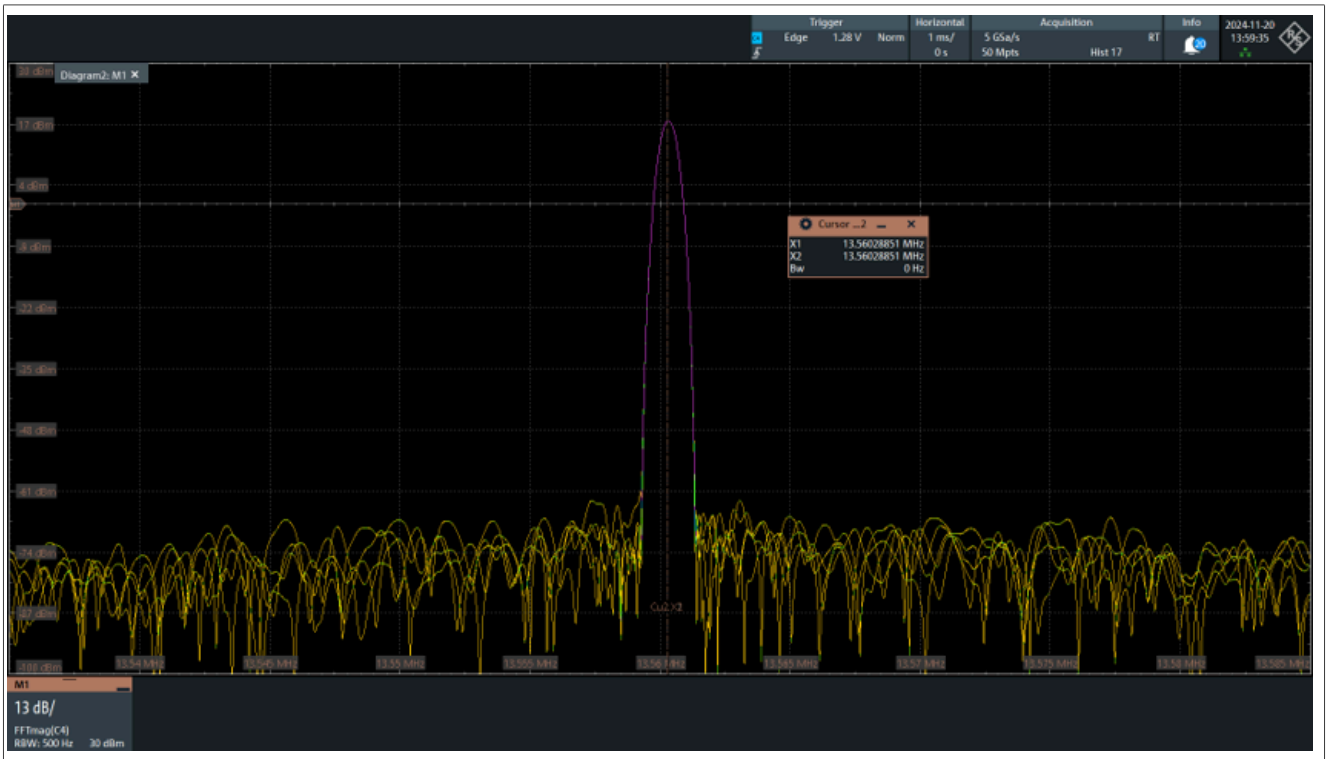

Figure 13. CL1 & CL2 = 10 pF

Find the results in the table below.

Table 4. Measurement results for different load capacitances

CL1 and CL2 (pF)	Measured frequency (Hz)	Offset from 13.56 MHz (ppm)
10	13 560 289	+21
12	13 560 136	+10
15	13 559 983	-1.25

If the frequency offset is too high, the load capacitors must be adjusted accordingly.

3.4 Negative resistance

Negative resistance of the oscillator (**-R**) is an important parameter which defines the oscillation stability and reliable start of the oscillator. The negative resistance "compensates" the losses in the oscillator circuit caused by XTAL Equivalent Series Resistance (**ESR**).

The theoretical condition for XTAL oscillation is $|-R|$ **= ESR**. There is no margin for this condition, and even a small change in the circuit (for example, due to the component tolerances, changes in temperature or humidity), the XTAL might not perform properly. Therefore, it is recommended to have the negative resistance 5 times higher than the ESR of the XTAL to allow for all operating conditions.

$$|-R| \geq 5 * ESR$$

The negative resistance is defined by the following parameters:

- **gm** → Transconductance of the inverter amplifier
- $\mathbf{C_{L1}}$ and $\mathbf{C_{L2}}$ → External loading capacitors
- $\mathbf{C_{XTAL}}$ → XTAL Shunt capacitance
- $\mathbf{C_{PCB\_STRAY}}$ → Stray capacitance of the PCB
- $\mathbf{C_{PCB\_IN}}$ and $\mathbf{C_{PCB\_OUT}}$ → Parasitic capacitance of the input and output PCB traces
- $\mathbf{C_{IN}}$ and $\mathbf{C_{OUT}}$ → Capacitance of the XTAL input and output pins

The applied negative resistance against the ESR of the XTAL can be calculated using the following formula:

$$Re(Z) = \frac{-\{g_m*(C_{L1}+C_{IN}+C_{PCB\_IN})*(C_{L2}+C_{OUT}+C_{PCB\_OUT})\}}{\left\{\omega^2*\left[(C_{L1}+C_{IN}+C_{PCB_{IN}})*(C_{L2}+C_{OUT}+C_{PCB_{OUT}})+(C_{L1}+C_{IN}+C_{PCB_{IN}})*(C_{XTAL}+C_{PCB_{STRAY}})+(C_{L2}+C_{OUT}+C_{PCB_{OUT}})*(C_{XTAL}+C_{PCB_{STRAY}})\right]^2+\left[g_m*(C_{XTAL}+C_{PCB_{STRAY}})\right]^2\right\}} \ (\Omega)$$

Figure 14. Applied negative resistance formula

***Note**: The value of the negative resistance can approximately be calculated using the NXP Crystal Oscillator Calculator (Section 4).*

See examples of the negative resistance and load capacitances for different oscillator parameters below.

Figure 15 shows the influence of the PCB stray capacitance on the negative resistance value applied against the ESR of the XTAL. As shown in the figure, lower PCB stray capacitance leads to higher achievable absolute negative resistance.

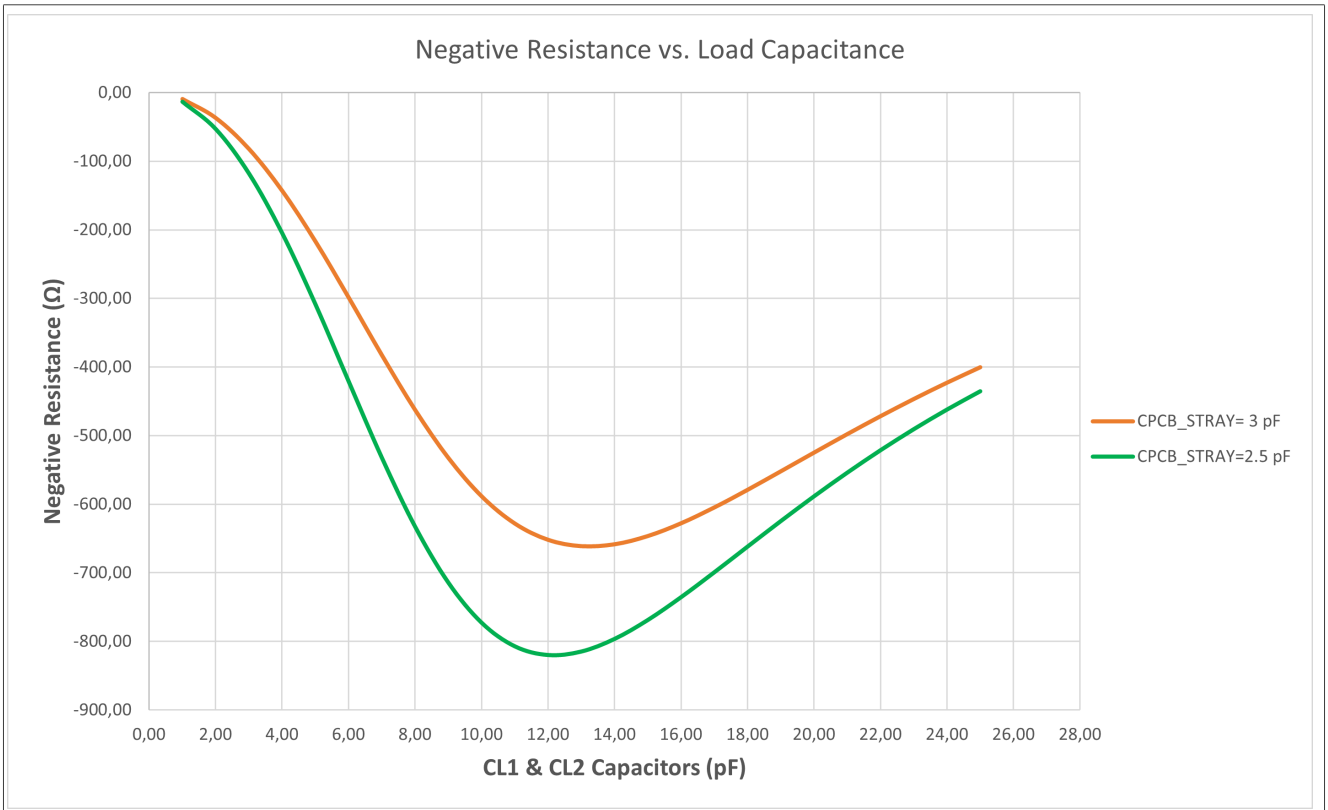

Figure 15. Negative Resistance vs. Load Capacitance, different C_{PCB_STRAY}

The same applies for the C_{XTAL} (XTAL Shunt capacitance) shown in Figure 16. Lower XTAL stray capacitance leads to higher achievable absolute negative resistance.

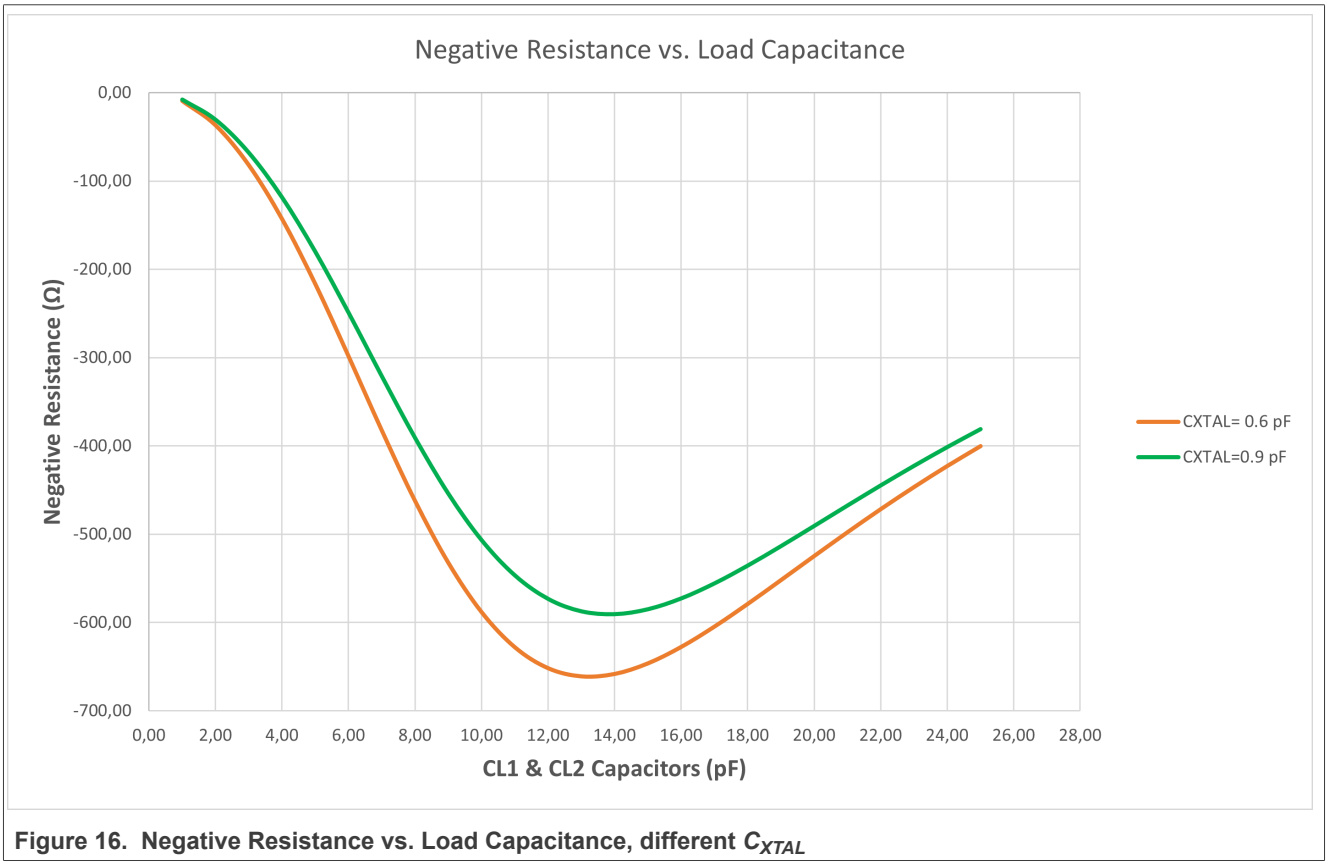

Figure 16. Negative Resistance vs. Load Capacitance, different C_{XTAL}

Figure 17 shows the behavior of the negative resistance over load capacitance for different values of the inverter transconductance "*gm*". The transconductance depends on the type of the inverter used (for example, a different NFC controller) and its supply voltage. The value may slightly vary for different ambient temperatures.

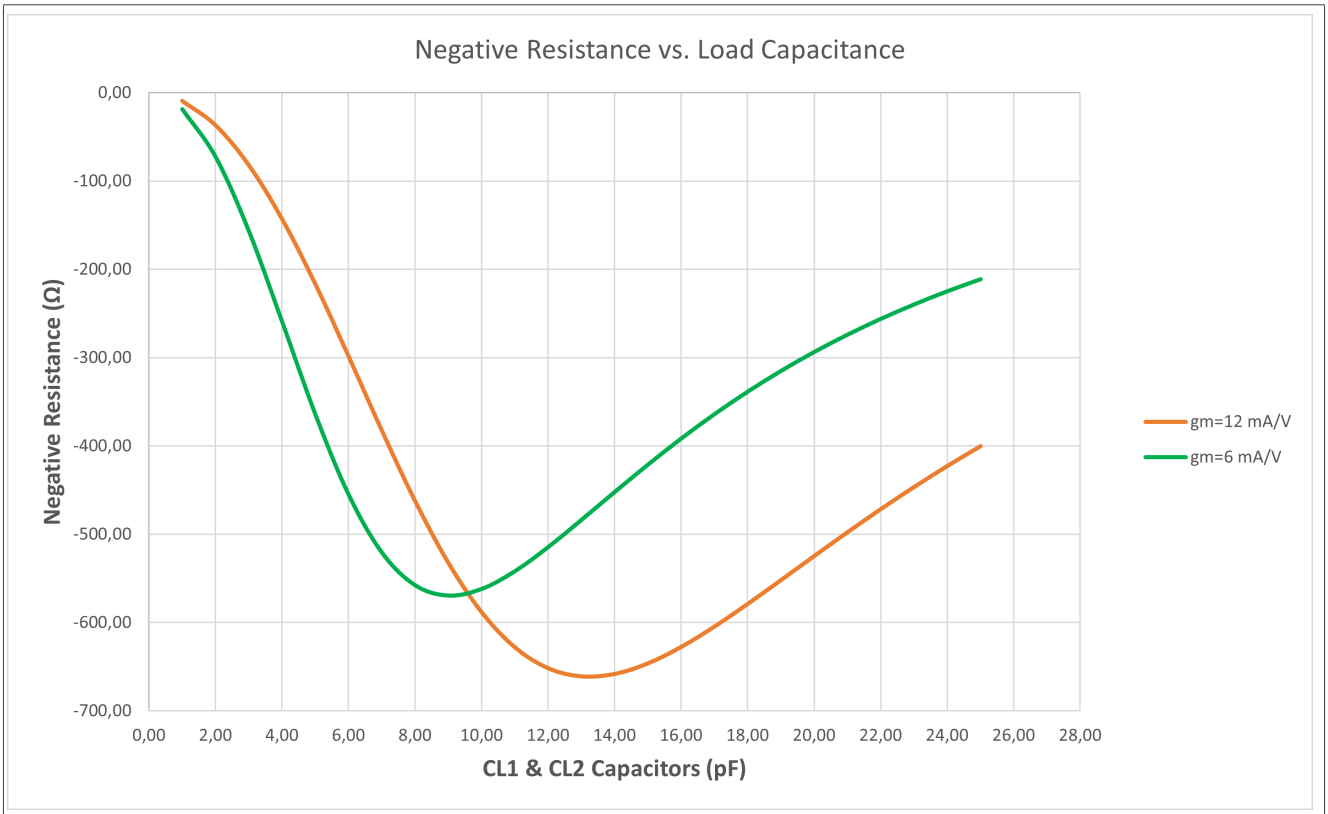

Figure 17. Negative Resistance vs. Load Capacitance, different *gm*

3.4.1 Negative resistance - check

For a quick check if the design has enough negative resistance compared to the ESR of the XTAL in use, a simple test can be performed. Follow the steps below:

- Check the ESR_{max} of the used XTAL in the data sheet
- Connect a resistor R_{TEST} which is approximately 5 times higher than ESR_{max}
  - for example, If ESR_{max} = 100 Ω, then R_{TEST} = 510 Ω
- Check if the XTAL starts to oscillate
  - Check for the minimum and maximum required operating temperature
  - Check for a different ICs

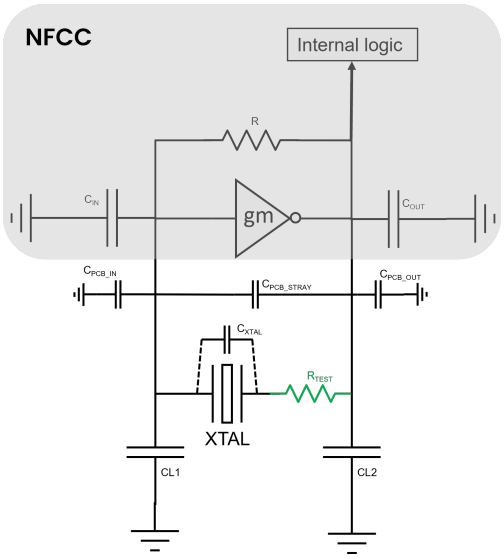

Figure 18. Negative resistance test

If the XTAL does not start to oscillate or the oscillation is not stable enough, the following measures have to be considered:

- Increasing the "*gm*" value of the NFCC inverter block
- Using a different XTAL with a lower ESR
- Adjusting the CL1 and CL2 capacitors (typically, increasing their value)
  - This might be at the cost of frequency accuracy.
- Reducing the C_{PCB_STRAY} capacitance of the PCB
  - Lower C_{PCB_STRAY} leads to higher negative resistance absolute value.

3.4.2 Transconductance "gm" values

The table below shows indicative values of transconductance for some NXP products. These values can be used for the negative resistance calculation.

Table 5. Indicative values of transdunctance

Product	gm (mA/V)	Comment
PN7642	33	Normal mode and LPCD/ULPCD
PN7220/1	33	Normal mode and LPCD
PN5190	33	Normal mode and LPCD/ULPCD
PN7160	12	Normal mode and LPCD

3.5 Drive level

The XTAL drive level (**DL**) defines the power dissipation of the XTAL unit. This value is typically in the range of tens to hundreds of µW and is defined by the XTAL manufacturer in the data sheet.

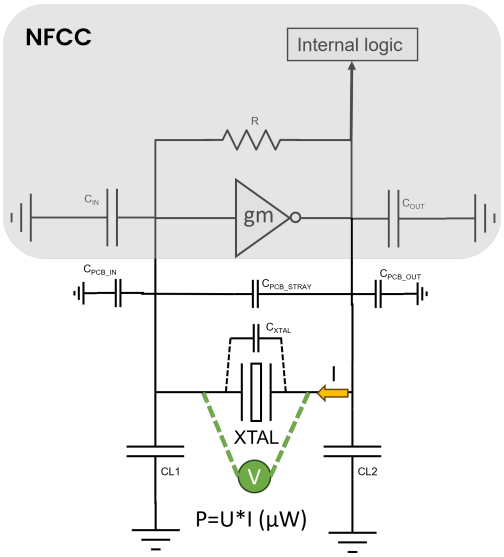

Figure 19. XTAL drive level

It is important to check the XTAL drive level during oscillation. Make sure that the value is under the maximum value specified in the XTAL data sheet.

Note: *For Drive Level evaluation, it is advisable to collaborate closely with the crystal supplier and consider utilizing the circuit evaluation services they typically offer.*

3.5.1 Drive level - Based on the crystal current

This measurement requires a current probe and information about the XTAL ESR. The current is measured directly in front of the crystal unit as shown in Figure 20.

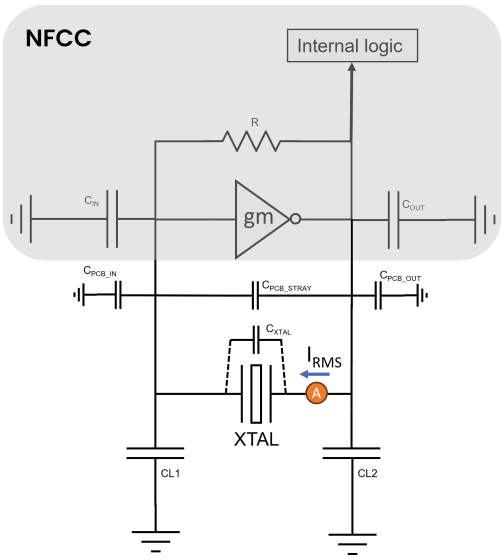

Figure 20. Crystal "DL" measurement - Current measurement approach

The drive level the XTAL can be calculated based on the following formula:

$$Drive\ Level\ (DL) = \mathrm{ESR} * {I_{RMS}}^2$$

Figure 21. Drive Level - Calculation based on current

Where:

- **ESR** - Equivalent Series Resistance of the XTAL (Typically the "max" value is considered as the worst case)
- I_{RMS} - XTAL current (RMS value)

3.5.2 Drive level - Based on the crystal voltage

The current probe might not always be available. However, if the resistance (ESR) of the XTAL is known, the voltage on the XTAL can be measured and the drive level calculated accordingly as shown in Figure 22.

For the voltage measurement, it is recommended to use a Differential Active Probe with low capacitance (max.1pF).

$$Drive\ Level\ (DL) = \mathrm{ESR} * \left(\pi * f * \frac{V_{pp}}{\sqrt{2}} * (C_{LOAD} + C_{PROBE}) \right)^2$$

Figure 22. Drive level - Formula

Note: *The value of the Drive Level can be calculated using the NXP Crystal Oscillator Calculator (Section 4).*

Where:

- **ESR** - Equivalent Series Resistance of the XTAL (Typically the "max" value is considered as the worst case)
- **Vpp** - Measured peak-to-peak voltage
- **C_{LOAD}** - XTAL load capacitance → Figure 5
- **C_{PROBE}** - Parasitic capacitance of the scope probe
- **f** - Oscillation frequency

If the resulting drive level is too high, a damping resistor ($R_{DAMPING}$) can be used to reduce the drive power (see Figure 23).

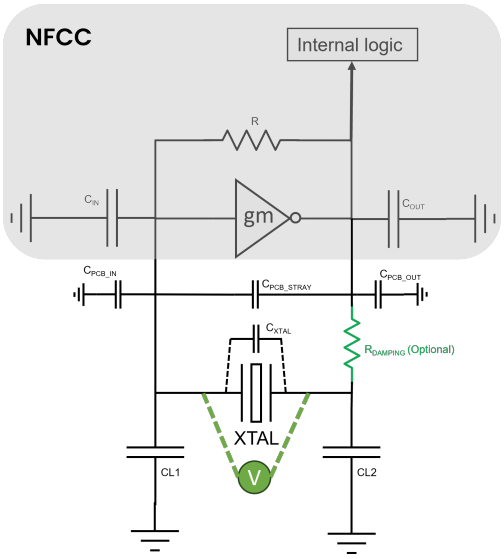

Figure 23. $R_{DAMPING}$ in placement

4 NXP crystal oscillator calculator

NXP provides a simplified crystal oscillator calculator in excel (see Figure 24). The calculator provides customers with initial values for their design which can be a good starting point.

Note: *It is recommended to measure each parameter and potentially cooperate with the XTAL manufacturer during the design phase of a product.*

The calculator is available under **Design Resources** on the NXP product pages (PN7160/PN7161, CLRC663, PN5180, PN7462, PN7642, PN5190, PN7220).

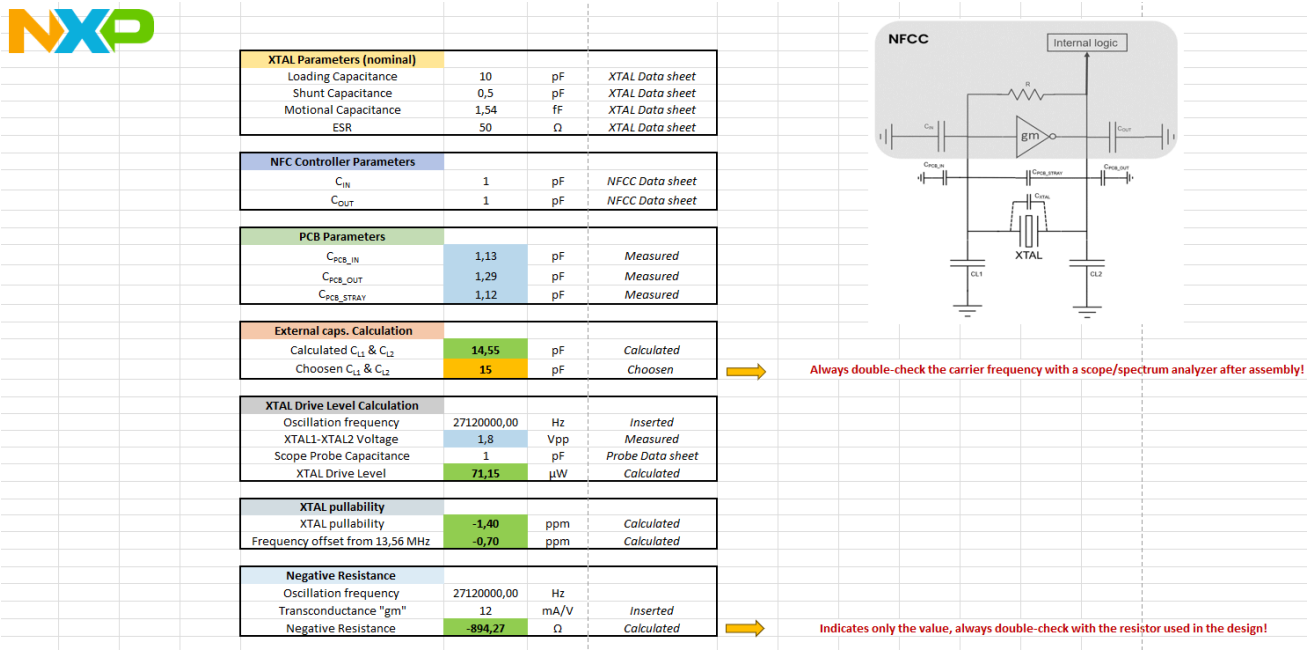

Figure 24. NXP_Crystal_Oscillator_Calculator.xlsx

5 XTAL start-up

The XTAL start-up is defined as the time between an oscillator being turned on and reaching a certain oscillation amplitude (for example, 90%). However, the NXP NFC controllers can typically detect at lower levels than 90%. Therefore, the start-up time can be defined as the time between an oscillator being first turned on and the NFC controller detecting the clock signal using its "clock detection" mechanism. In this context, the correct term would be "**clock detection time**".

The required time can differ depending on the NFC Controller and the operation mode in use (ULPCD, LPCD, Standard "digital" Polling).

- For the PN7160/PN7161, the XTAL start-up time is maximum **3 ms**, typically around **1 ms**.
- For the PN5190/PN7642/PN7220, the XTAL start-up time is typically **1 ms** for normal operation and ideally **400 µs** for Ultra Low-Power Card Detection (ULPCD)

Figure 25 shows an example of XTAL start-up waveform showing different between XTAL start-up time and "Clock detection time".

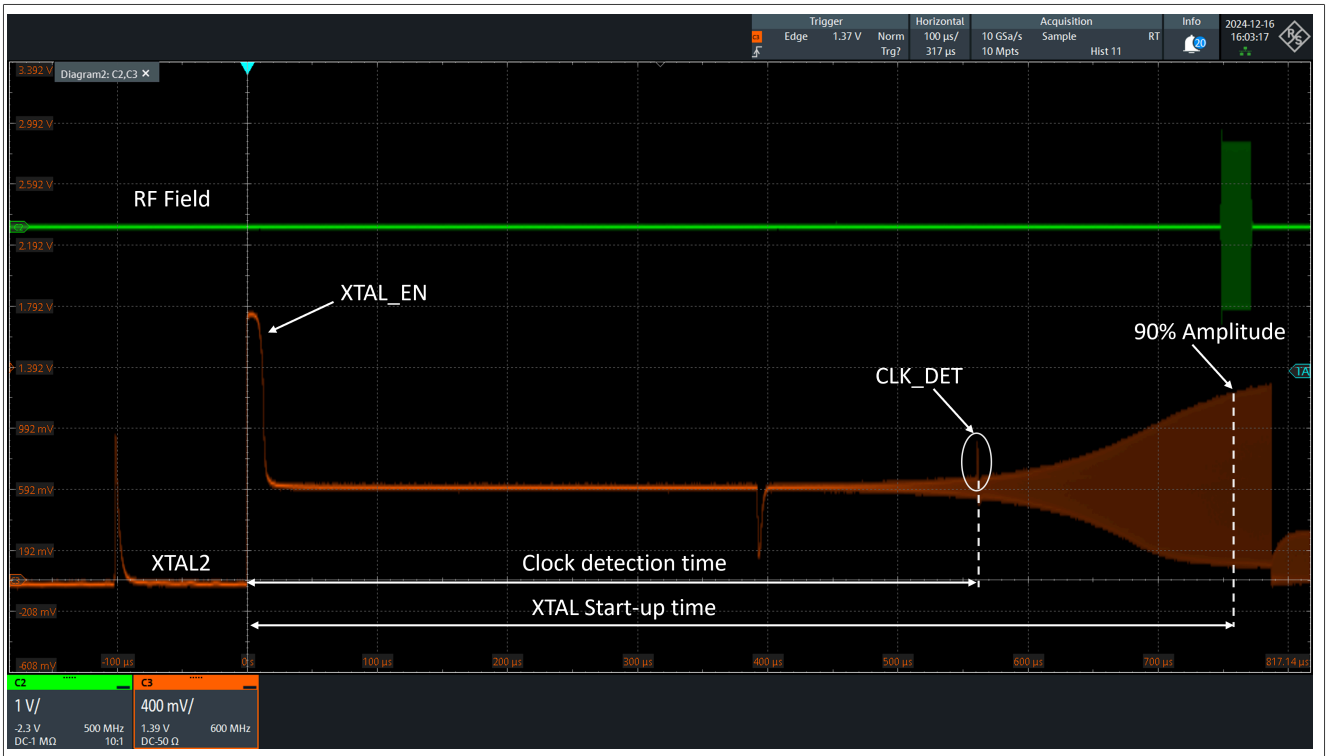

Figure 25. XTAL start-up

Note: *The start-up waveform might look differently depending on the XTAL type or NFC controller in use.*

The start-up time is influenced by multiple factors. For example, it can be reduced by:

- XTAL parameters:
  - Low $\mathbf{C_{XTAL}}$ shunt capacitance
  - High $\mathbf{C_{MOTIONAL}}$
  - Low $\mathbf{C_{LOAD}}$
- PCB parameters:
  - Low $\mathbf{C_{PCB\_STRAY}}$
- NFC controller parameters:
  - High "**gm**" transconductance of the internal inverted block

The effect of each parameter listed above has been simulated and compared. See the results in Section 8.

5.1 Direct start-up measurement

The XTAL start-up can be measured directly by probing the XTAL2 pin (XTAL oscillator output) and sniffing the generated RF Field as shown in Figure 26. For this measurement, it is recommended to use **an active low capacitance single-ended probe** (max. 1pF) or a "buffer board" to minimize the measurement uncertainties as much as possible.

For this measurement, ensure that only the measured NFC device is connected to the power supply or PC. If multiple NFC devices are connected to one source with the same GND (for example, a PC), the start-up time measurement can be inaccurate.

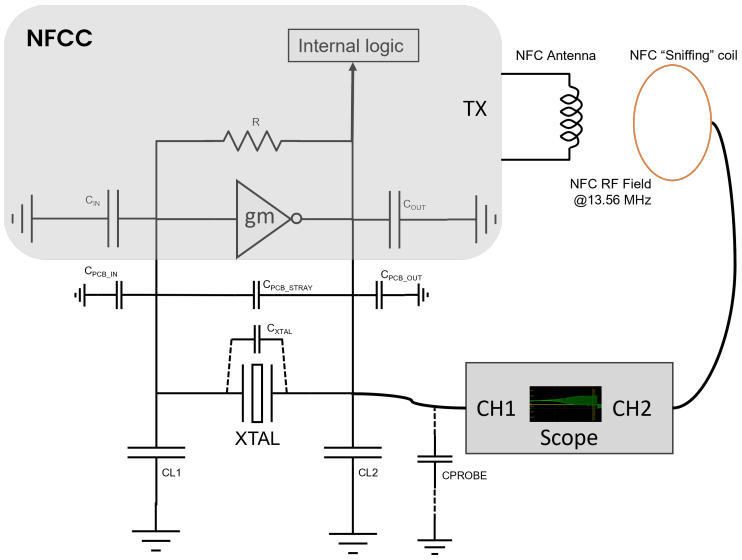

Figure 26. Direct start-up measurement

5.2 NFC Cockpit measurement for ULPCD with PN5190 and PN7642

This chapter describes how to evaluate the XTAL start-up time from the measured waveform for PN5190 and PN7642 products.

PN7642 also offers a test signals which enable more convenient XTAL and ULPCD measurements without "high-end" equipment (see Section 5.3). The start-up time measurement in ULPCD mode can be performed with the help of the NFC Cockpit Tool and the ULPCD test bench which is part of it.

See the NFC Cockpit interface in Figure 27.

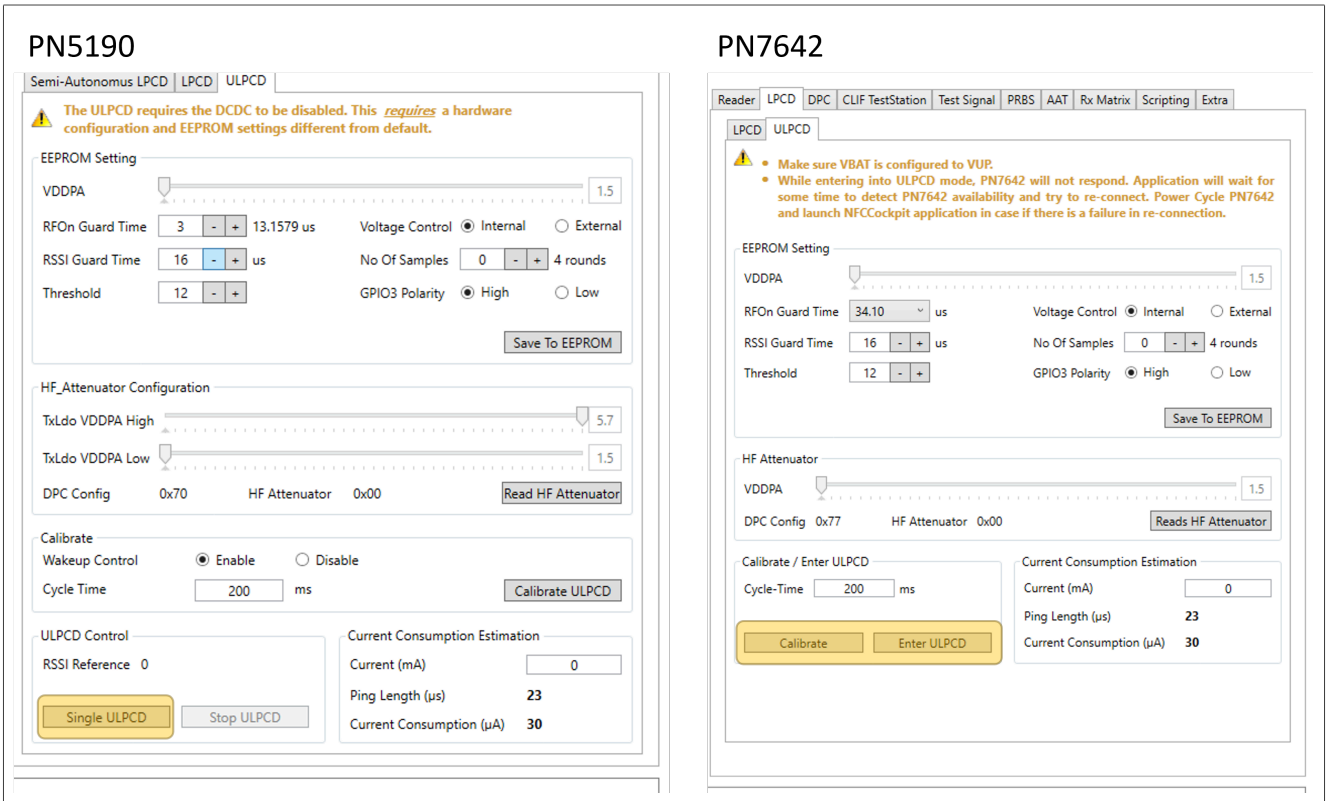

Figure 27. NFC Cockpit → ULPCD Test bench for PN5190 and PN7642

Figure 28 shows the logic of the XTAL start-up in ULPCD mode.

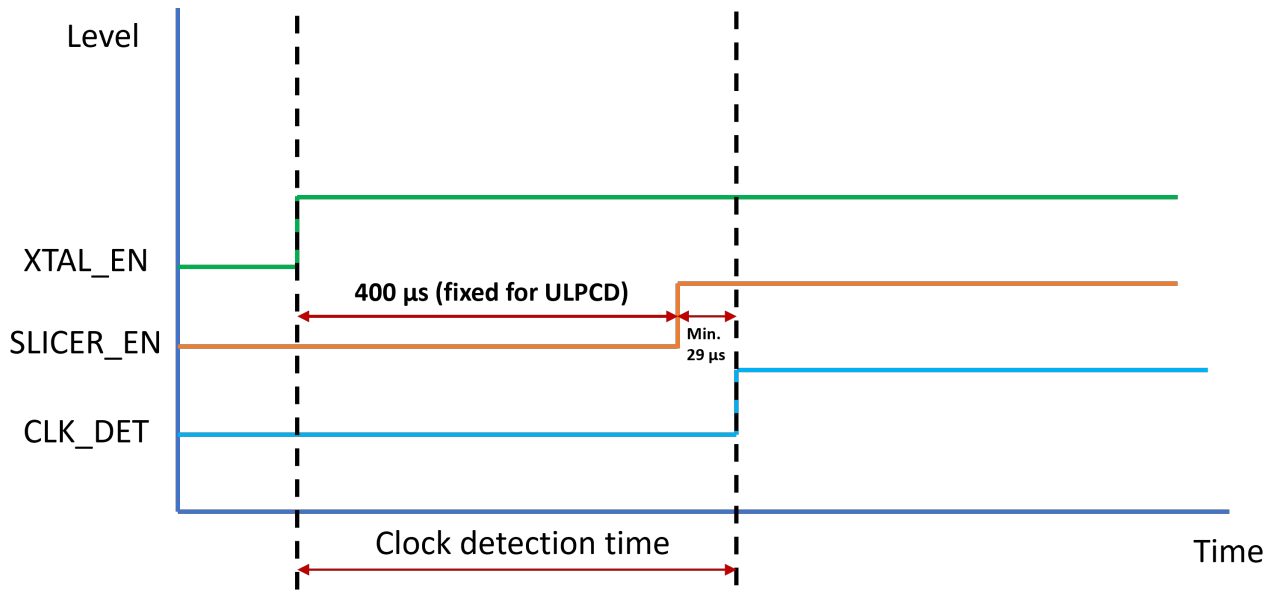

Figure 28. XTAL start-up in ULPCD - Logic

Where:

- **XTAL_EN** → XTAL enabled signal (Kick of the XTAL)
- **SLICER_EN** → SLICER enabled signal (SLICER block converts the 27.12 MHz sine signal to a 27.12 MHz rectangular signal)
- **CLK_DET** → CLK detection indicates that the clock signal was successfully detected by the NFC controller

In ULPCD, the SLICER_EN is always enabled after **400 µs**. At this point, the XTAL amplitude should be high enough (min. around **100 mVpp** on XTAL2) for the slicer to generate a proper clock signal.

- If the XTAL amplitude is high enough when SLICER is enabled: The CLK_DET goes high in about **29 µs**. See Section 5.2.2 and Section 5.2.2.1.
- If the amplitude is too low or completely missing when SLICER is enabled: The CLK_DET goes high when enough amplitude is reached (**>29 µs**). See Section 5.2.1.

The signals described above can be observed in the measured XTAL2 analog waveform, see Figure 29.

The point when the clock was detected by the IC (CLK_DET) can be determined from the "spike" seen in the XTAL2 waveform.

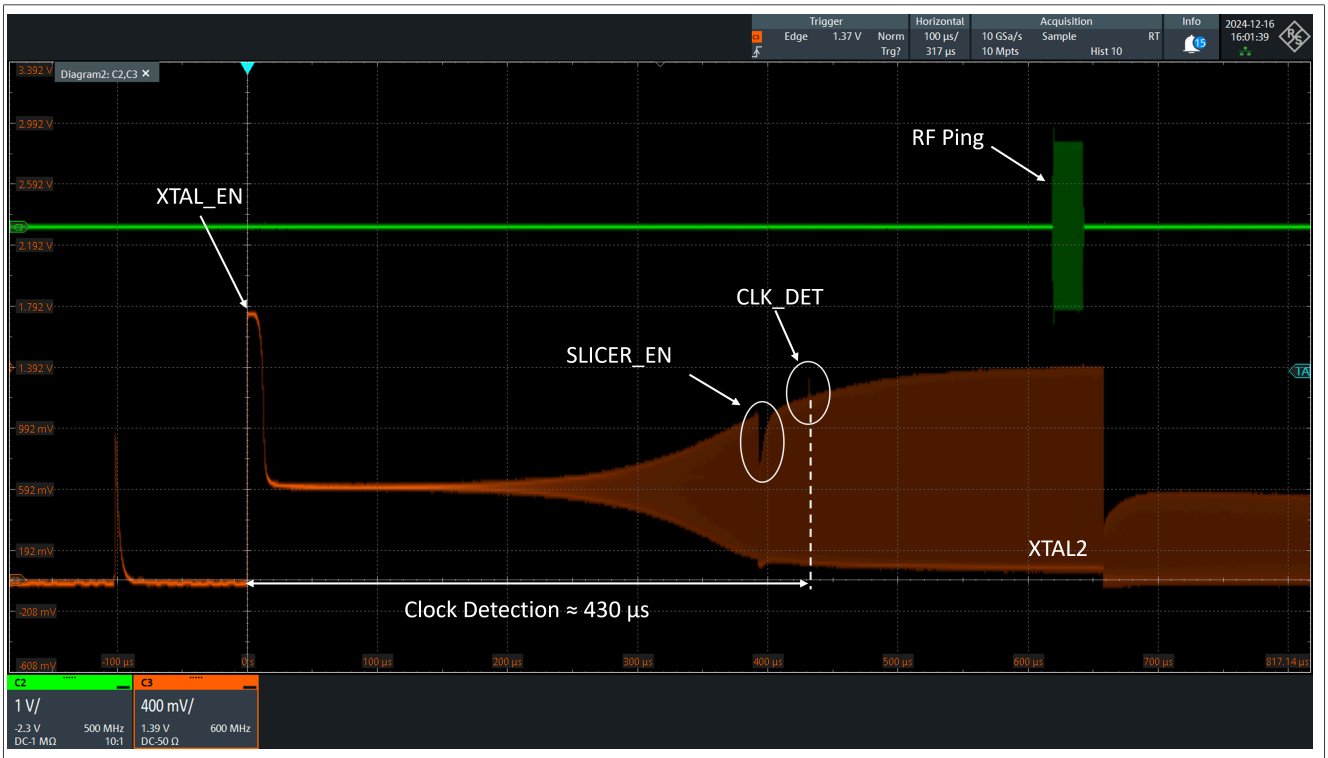

Figure 29. XTAL start-up measurement

Note: *If the XTAL start-up is too long, the ULPCD takes longer and this leads to a higher-than-average current consumption.*

5.2.1 Example of slow XTAL start-up

In this example, the XTAL starts to oscillate late. There is not enough XTAL amplitude when SLICER is enabled (**400 µs**). Therefore, the CLK_DET takes more time and it is detected in **560 µs.**

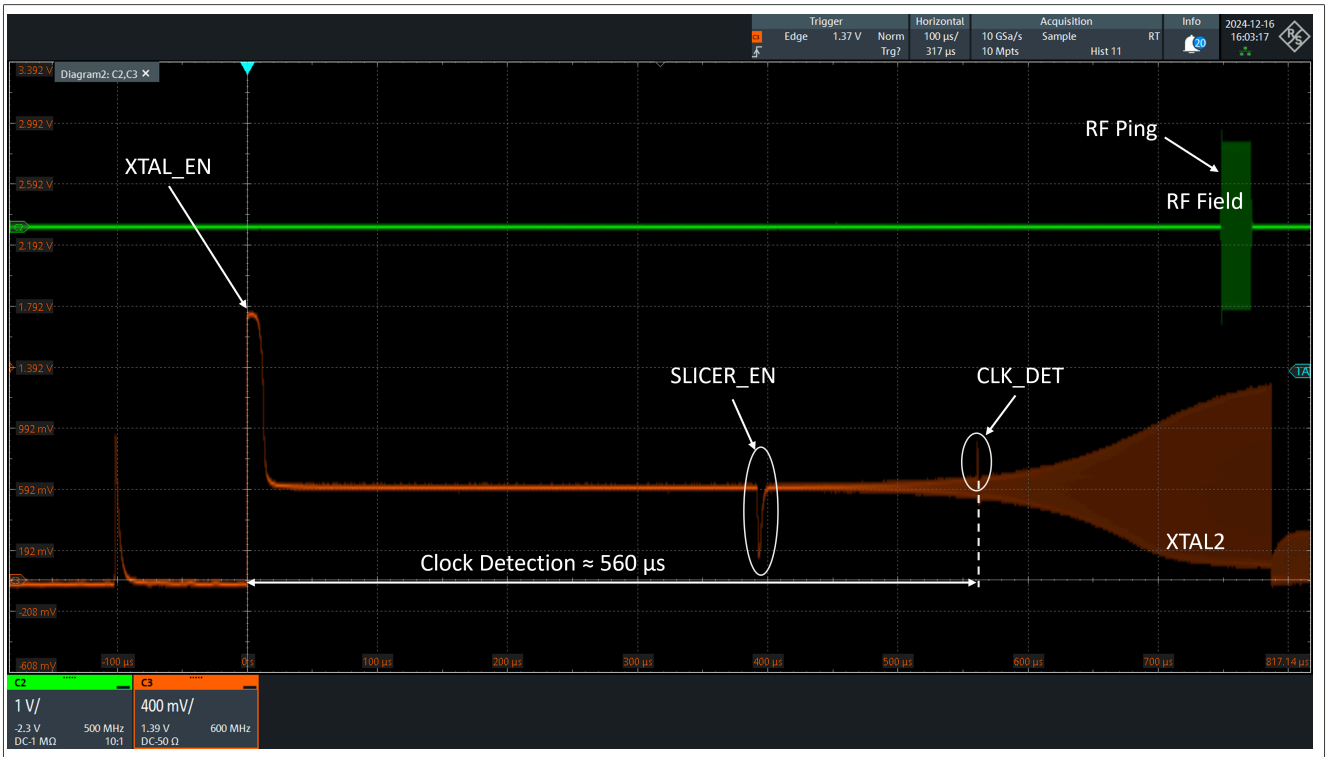

Figure 30. Measured waveform for slow XTAL start-up in ULPCD

Note: *This XTAL also works for ULPCD, but ULPCD takes longer and the system may consume a few µA more.*

5.2.2 Example of fast XTAL start-up

In this example, the XTAL starts to oscillate already before the SLICER is enabled. When the SLICER is enabled (**400 µs**), there is a sufficient amplitude and the CLK_DET is immediately triggered (with **29 µs** delay). In this case, the clock detection takes **429 µs**.

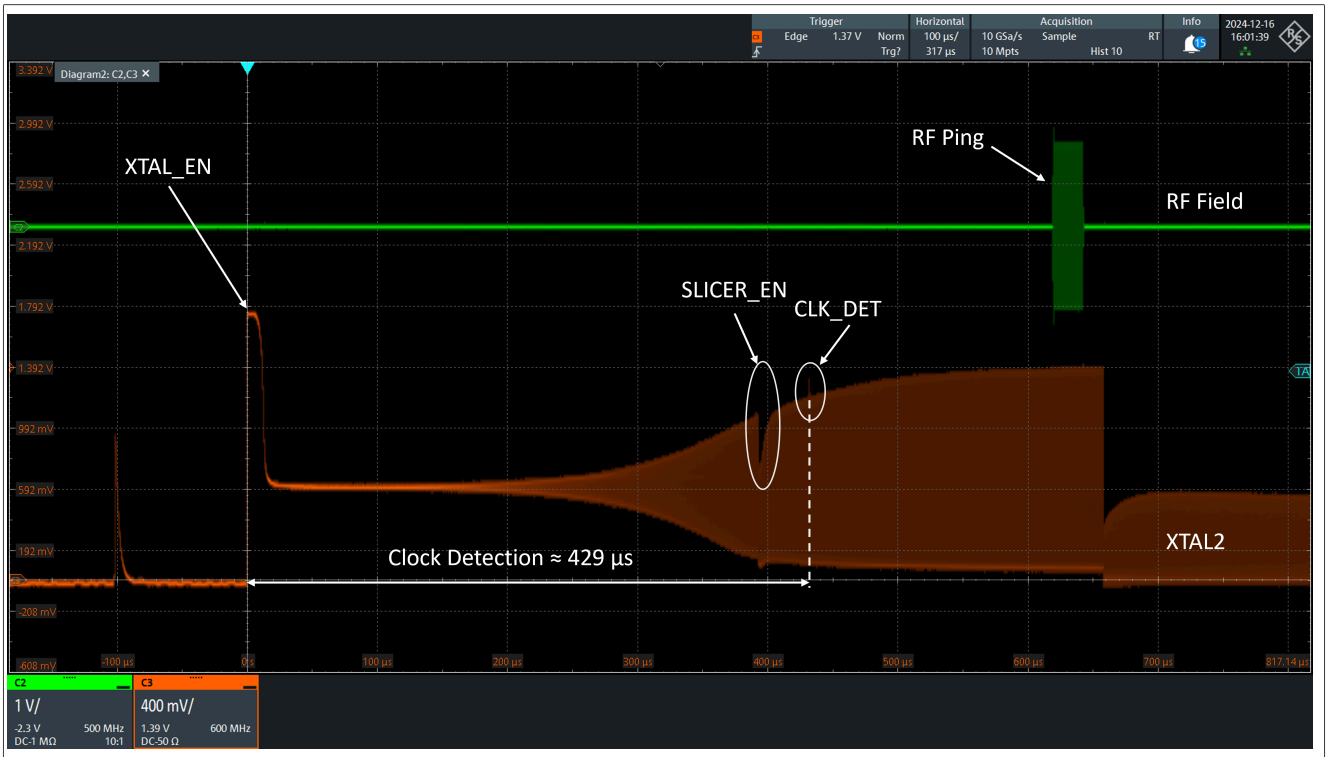

Figure 31. Measured waveform for "Fast" XTAL start-up in ULPCD

5.2.2.1 Full amplitude reached before SLICER is enabled

In this special example, the XTAL has already reached its full amplitude before the SLICER is enabled. Therefore, the CLK_DET is immediately triggered (with **29 µs** delay).

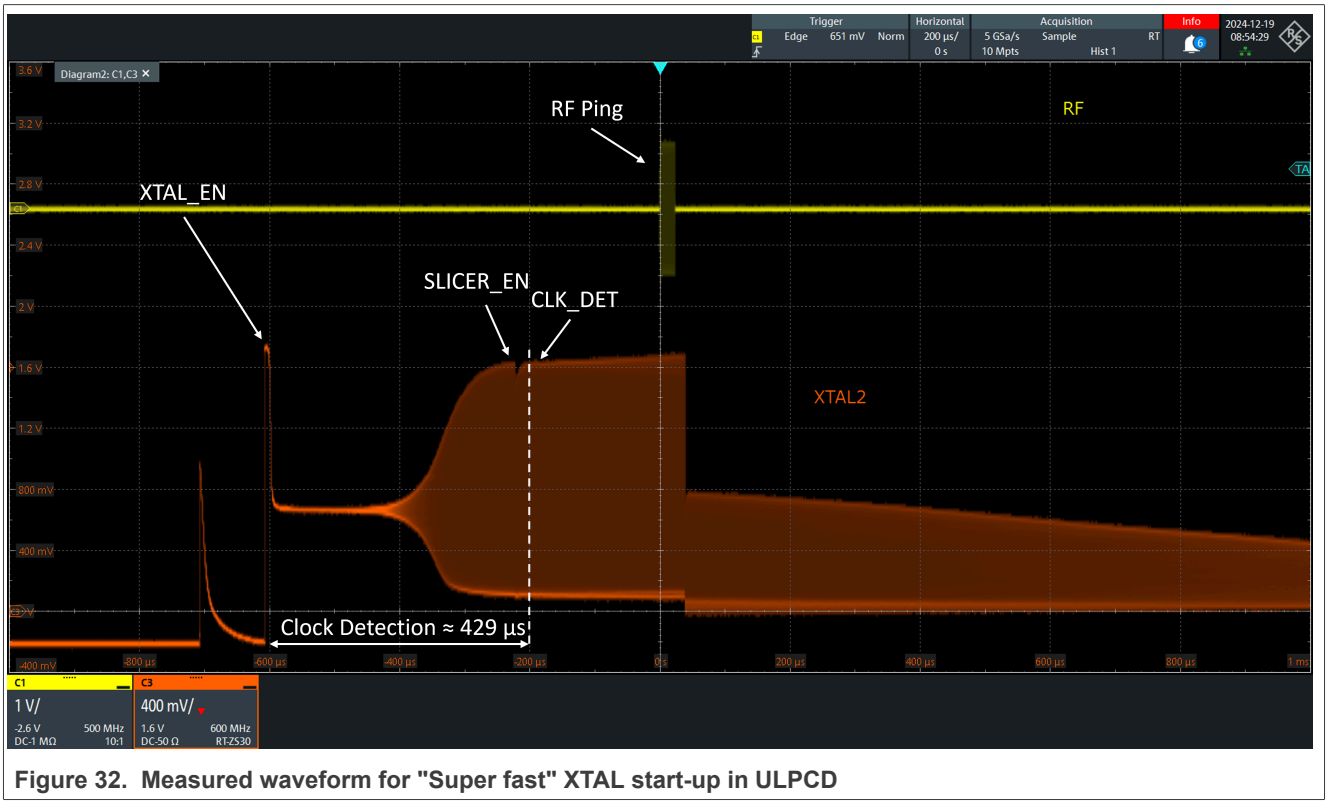

Figure 32. Measured waveform for "Super fast" XTAL start-up in ULPCD

Note: *As the XTAL reached its full amplitude very fast, the CLK_DET "spike" is not very visible in the waveform.*

5.3 Measurement using test signals for ULPCD (PN7642 only)

PN7642 allows to use a test signals in ULPCD mode to measure the XTAL start-up. The advantage is that the user does not need any special equipment (for example, a high-end scope with an active probe). The measurement can be performed with the help of a standard scope or a logic analyzer.

See an example of the measurement setup in Figure 33.

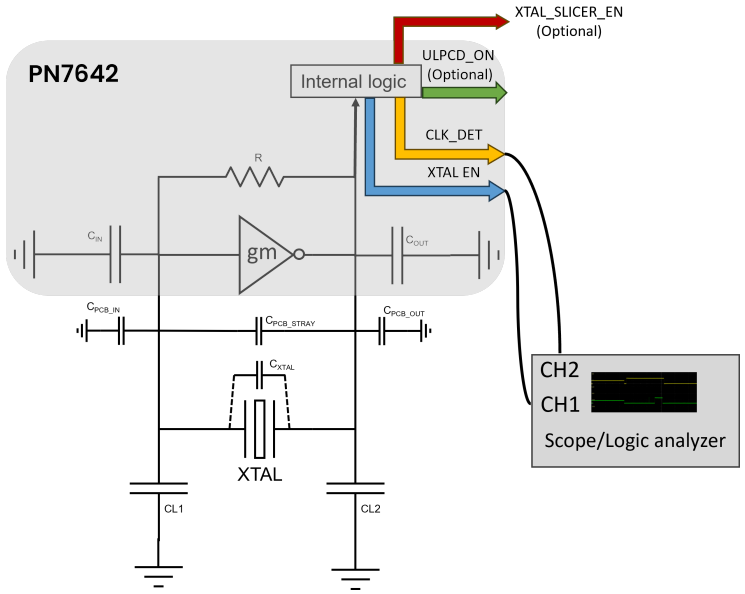

Figure 33. XTAL start-up measurement using a test signals

See an example of the measurement in Figure 34. This measurement also contains RF field and XTAL2 waveform for better understanding.

Users can only capture when the XTAL starts (XTAL_EN signal) and when the clock is detected (CLK_DET). The delta between these two signals is the "clock detection time".

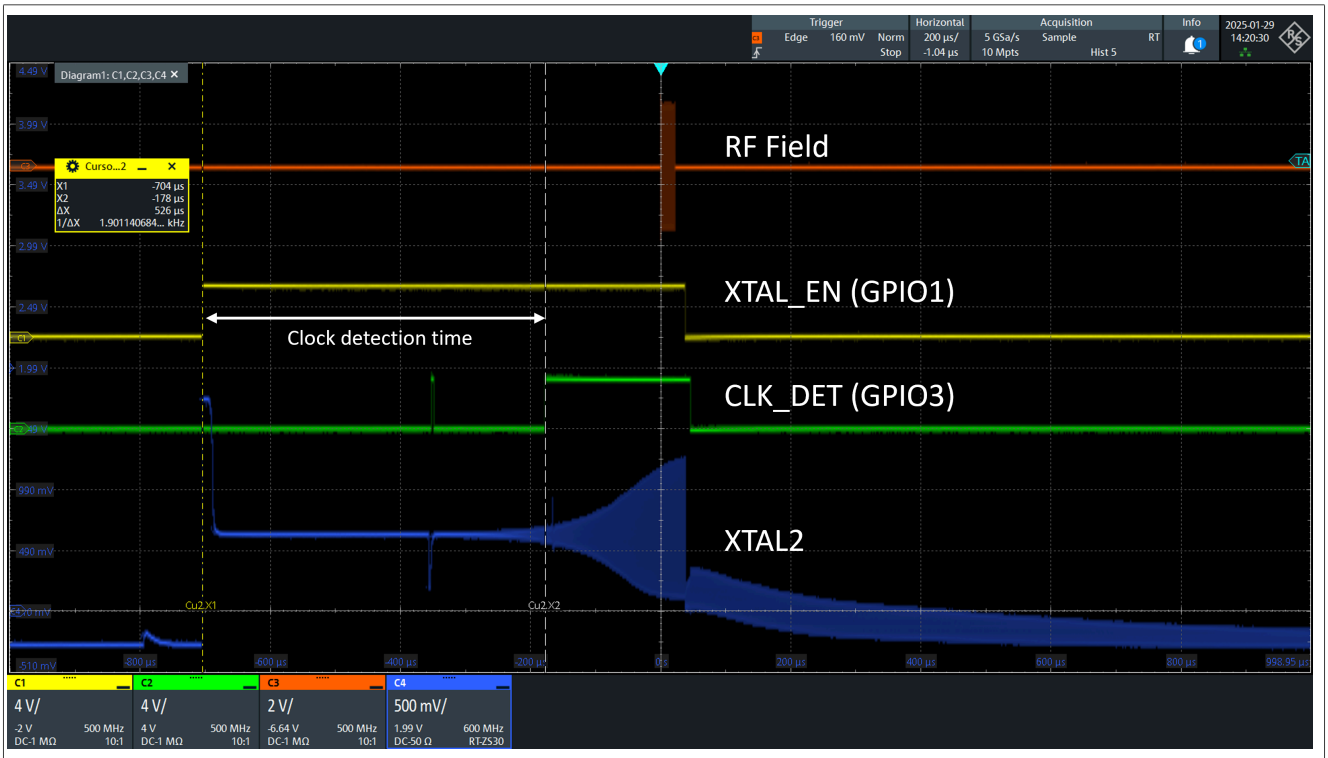

Figure 34. XTAL start-up measurement using a test signals - example

Users can also check the ULPCD duration time using an ULPCD_ON test signal (see Figure 35). This time defines how long the IC is in the "active" mode. The shorter the ULPCD_ON time, the lower the average power consumption. The ULPCD_ON time directly depends on the XTAL start-up (Clock detection time). The shorter the clock detection time, the shorter the ULPCD_ON time.

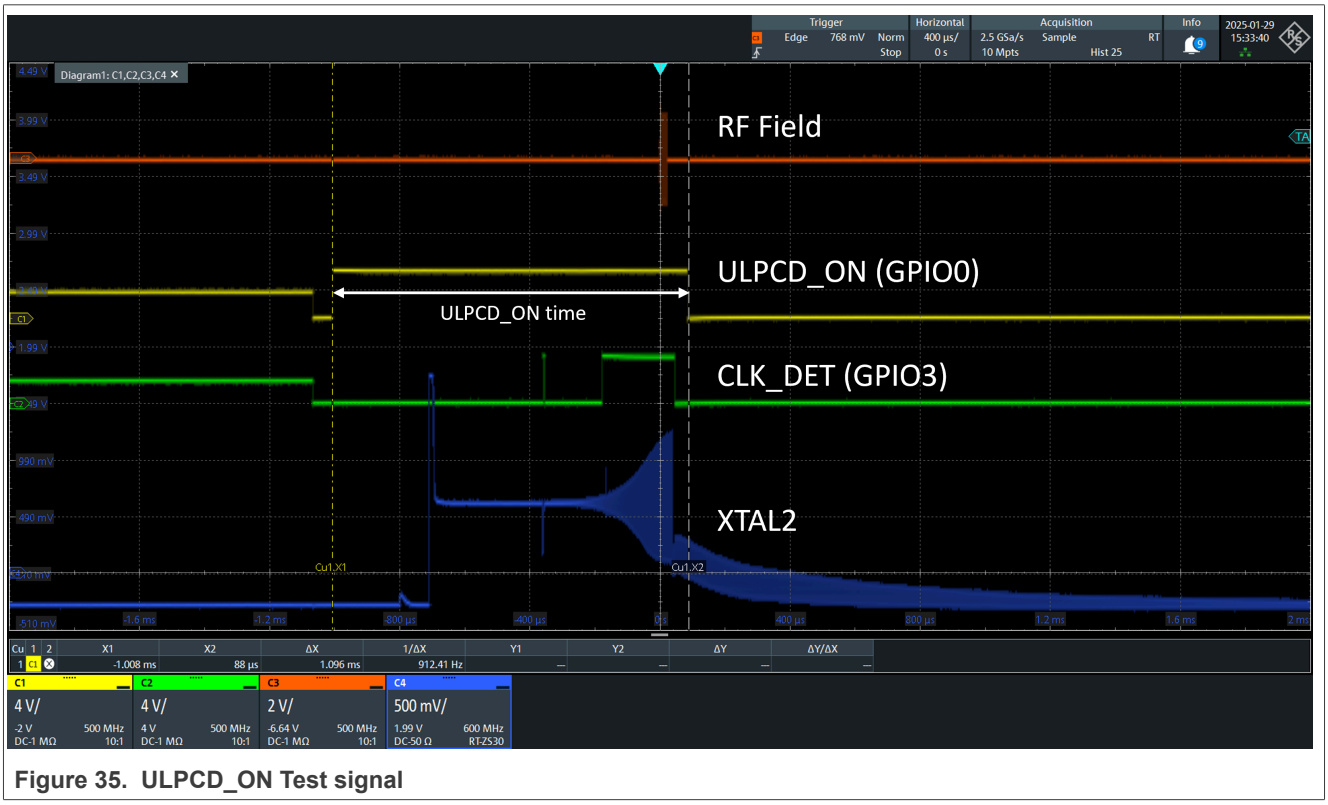

Figure 35. ULPCD_ON Test signal

5.3.1 How to use test signals for PN7642

The test signals are available through the *PCRM_ULPCD_CTRL4 (address: 0xEB)* register. The NFC Cockpit can be used to control the test signals during the measurement.

See the flow in Figure 36:

1. Select the *PCRM_ULPCD_CTRL4* register (in PCRM_HP).
2. Set bits 5, 6 and 7 to "***1***".
3. Write the register:
   a. Once the PN7642 wakes up from ULPCD (for example, when a load is detected), this register is reset. User have to write the register before every ULPCD entering.
4. Activate ULPCD by clicking "Enter ULPCD" and check the test signals on the GPIOs (see Table 6).

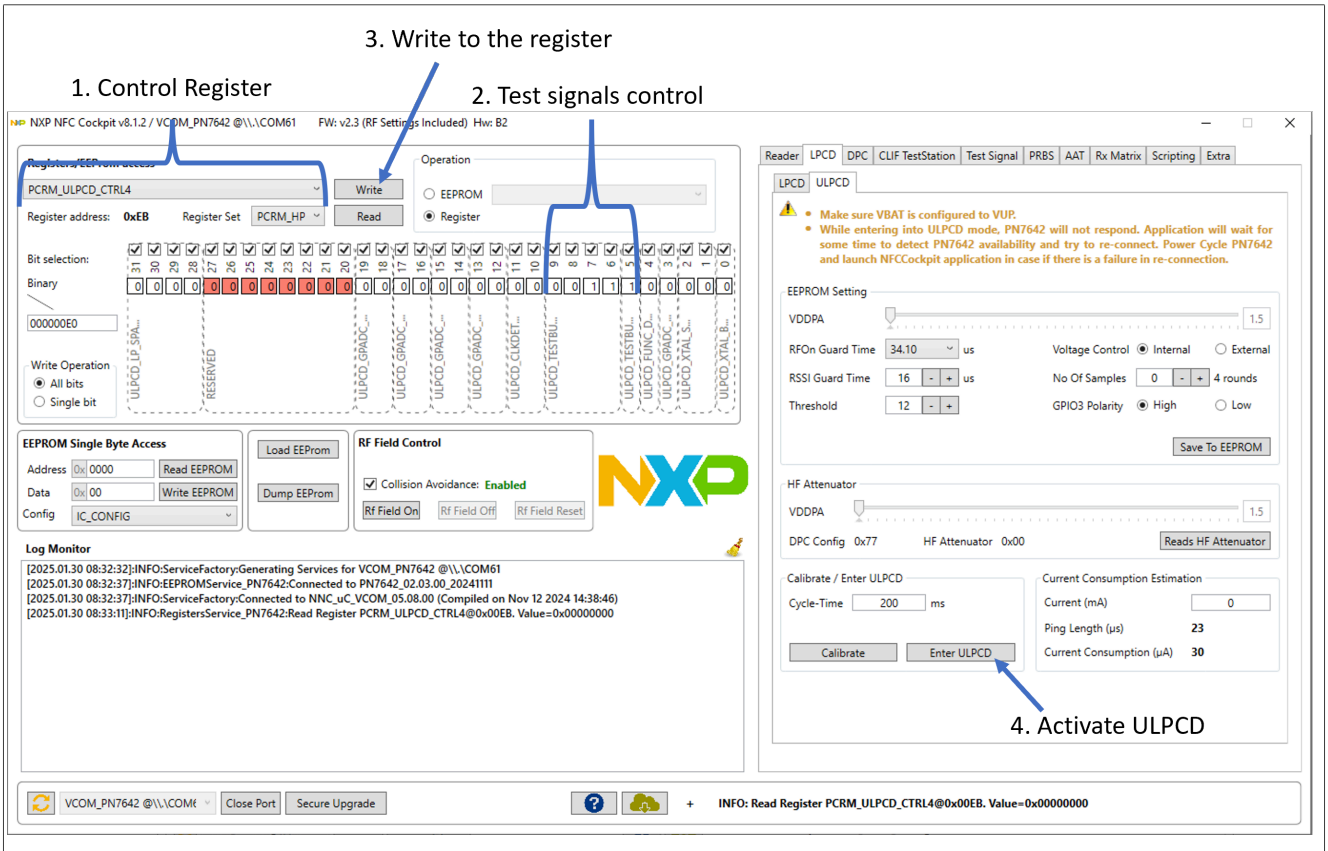

Figure 36. Test signals in NFC Cockpit

Table 6. Test signals mapping

Test signal name	GPIO mapping	Description
ULPCD_ON	GPIO0	the overall ULPCD cycle duration
XTAL_EN	GPIO1	when the XTAL is enabled
XTAL_SLICER_EN	GPIO2	when the slicer is enabled
CLK_DET	GPIO3	when the clock signal is detected

6 Layout recommendations

The PCB introduces some parasitics, which must be considered and minimized during the PCB design. The stray capacitance of the PCB (C_{PCB_STRAY}) might influence the XTAL start-up significantly. Find a simplified illustration showing most of the PCB parasitics in Figure 37. In general, the XTAL must be connected as close as possible to the CLK1 and CLK2 pins from the NFCC to achieve the best performance possible. Find more design recommendations below:

- As the XTAL is sensitive to parasitic capacitance and noise, it is advised to:
  - place the XTAL far from other signals (especially other CLK lines or signals with frequent switching);
  - place the XTAL far from heat sources;
  - limit the crosstalk between CLK lines and other signals.
- Load capacitor connections:
  - Choose a capacitor with a good temperature stability such as COG/NP0 and a maximum tolerance of 2%.
  - Place the capacitors close to each other and to the XTAL.
  - Avoid connecting them to dirty ground.
- PCB layout (see an example in Figure 40):
  - XTAL1 and XTAL2 traces should be as short as possible to reduce C_{PCB_IN} / C_{PCB_OUT} parasitic capacitance (ideally max. **5 mm**)
  - Increase the spacing ("*d*") between XTAL1 and XTAL2 to reduce the C_{PCB_STRAY} (at least **0.5 mm**).
  - Isolate XTAL1 and XTAL2 traces with the help of the GND layer.
  - If possible, route the XTAL1 and XTAL2 traces symmetrically (same length).
  - Reduce the XTAL1 and XTAL2 trace width (max. **0.15 mm**)
  - Do not use vias for XTAL1 and XTAL2 traces.
  - Use a “keep-out” area around the crystal unit. The GND connection should use vias to the next GND layer.

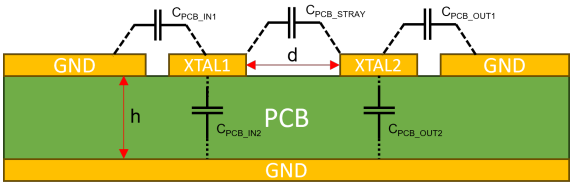

Figure 37. Illustration of the PCB parasitics

The stray and parasitic capacitances can be estimated using the formulas described in Figure 38.

$$C_{PCB\_STRAY} = \frac{\varepsilon_{free\_space} * \varepsilon_{r-air} * l * w}{d} \text{ (pF)}$$

Figure 38. PCB Stray capacitance calculation

$$C_{PCB\_IN2}/C_{PCB\_OUT2} = \frac{\varepsilon_{free\_space} * l * w * \varepsilon_{r-pcb}}{h} \text{ (pF)}$$

Figure 39. Parasitic capacitance calculation

- $\varepsilon_{r\text{-free air}}$ – vacuum permittivity
- $\varepsilon_{r\text{-PCB}}$ – relative permittivity of the PCB
- l – length of the trace
- w – width of the trace
- d – distance between traces
- h – height of the PCB

Find an example of PCB layout in Figure 40.

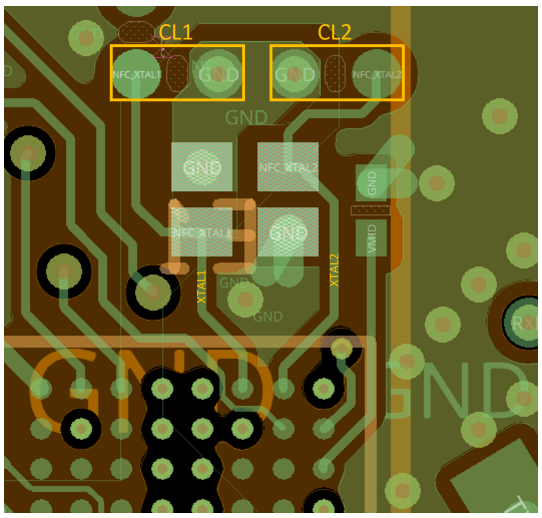

Figure 40. XTAL PCB layout example

7 XTAL references

Each NFCC from the NXP portfolio may require an XTAL with differing parameters due to different clock block implementations and/or requirements for start-up timing (ULPCD, LPCD, or Standard operation).

NFCC clock interfaces with XTAL oscillators have been verified with several references as shown in Section 7. Other crystal units might be suitable for the specified usage, but only those discussed within this document have been validated by NXP.

When using a different XTAL, frequency accuracy, drive level, nominal load capacitance, and ESR must be carefully selected according to the specification provided in each product data sheet.

7.1 XTAL references - PN5190/PN7642/PN7220

The recommended XTAL specifications are provided in the product data sheets (PN5190B1, PN5190B2, PN7642 and PN7220).

To allow a broader range of crystals, NXP validated additional crystals with a slight deviation for shunt and motional capacitance from the recommended crystal specifications in the data sheets.

See the list of validated XTALs in Table 7.

Table 7. Validated XTALs for PN5190/PN7642/PN7220

XTAL Manufacturer	XTAL Part Number	Support	CLK_DET time in ULPCD (µs)	Comment
KYOCERA	CX1210SB27120 B0HPRC1	Standard Operation/ LPCD/ULPCD	381	Fully complaint to the XTAL specification in data sheets.
ABRACON (**)	ABM11W-27.1200 MHZ-8-D1X-T3	Standard Operation/ LPCD/ULPCD	381	$C_{motional\ NOM}$= 1.89 fF
Würth Elektronik / IQD (**)	830108212709 / LFXTAL094650	Standard Operation/ LPCD/ULPCD	381	$C_{motional\ MAX}$= 2.5 fF, $C_{shunt\ MAX}$= 3pF
TXC	8J27170002	Standard Operation/ LPCD/ULPCD	438	$C_{motional\ MIN}$= 0.5 fF

Note: *ULPCD may allow a broader range of crystals, however, NXP has not validated all of them. In this case, customers are required to perform thorough validation of their design with these crystals.*

Note: *When using the combination **830108212709 (LFXTAL094650)** or **ABM11W-27.1200MHZ-8-D1X-T3** with **PN5190 B1** and **ULPCD**, an external damping resistor must be included in the design. See Section 10.*

Note: *The CLK_DET time shown in Table 7 is a typical value measured on PNEV5190BP EVK. The time may differ depending on the PCB design.*

The XTAL (FA-118T 27.1200MD50Z-K3) used on PNEV5190BP, OM27642EVK and PNEV7220BP1 is intended for use on evaluation boards only and is not recommended for integration into customer production designs due to ESR_{MAX}= 200 Ω.

7.2 XTAL references – PN7160/PN7161

The recommended XTAL specification is provided in the PN7160 product data sheet.

See the list of XTAL References in Table 8.

Table 8. XTAL references – PN7160

XTAL Manufacturer	XTAL Part Number	Note
NDK	NX2016SA 27.12 MHz EXS00A-CS06346	C_L= 10 pF version
NDK	NX2016HA 27.12 MHz EXS00A-CH00075	C_L= 10 pF version
Murata	XRCGB27M120F3M10R0	Specific footprint (Pins 2 and 4 are NC.)

Note: *For PN7160/1, it is important to use a crystal with* ***nominal load capacitance between 10 pF - 12 pF****. Lower value might lead to low negative resistance and then issues with the XTAL start-up. For sufficient oscillation margin, It is also important to choose the right external loading capacitors (C_{L1} and C_{L2}). Select these capacitors to ensure the frequency offset from 13.56 MHz remains between* ***-5 ppm and 0 ppm****. It is strongly advised to maintain a* ***negative*** *frequency offset (e.g., -3 ppm) rather than a positive one (e.g., +3 ppm). See Section 3.3.1.*

When using a different XTAL than shown in Table 8, users are recommended to use the XTALs according to the Table 9. In this case, customers are also required to perform the robustness testing at the application level with the XTAL chosen by them.

Table 9. PN7160/PN7161 crystal requirements

Parameter	Symbol	Electrical Specs			Unit
		Min.	Typ.	Max.	
Nominal Load Capacitance	CL	10	-	12	pF
Equivalent Series Resistance	ESR	-	50	100	Ω
Shunt Capacitance	C_S	-	0.5	1	pF
Motional Capacitance	Cm	1	-	1.5	fF

Starting from firmware version **12.50.11**, the PN7160/1 includes an XTAL start retry mechanism. If the XTAL fails to start on its first attempt, the subsequent starts (up to 6 attempts in total) are performed. Additionally, users can initiate the subsequent XTAL starts with a boosted *gm* value. Users are recommended to use this feature. It can be enabled using the following NCI command:

- **A0 03 01 08** - Defaut *gm* value during XTAL start retry (default)
- **A0 03 01 18** - Boosted *gm* value during XTAL start retry

The user can receive an NCI notification (*60 07 01 E9*) when the retry mechanism is applied following the XTAL start failure. This notification can be enabled or disabled by the following NCI command:

- **A0 6F 01 00** - Notification is disabled (Default)
- **A0 6F 01 01** - Notification is enabled

7.2.1 PN7160/PN7160 - XTAL startup issue - Symptoms

If the XTAL encounters startup issues, users may notice symptoms such as missing or deviated NFC polling in the RF waveform as shown in Figure 41.

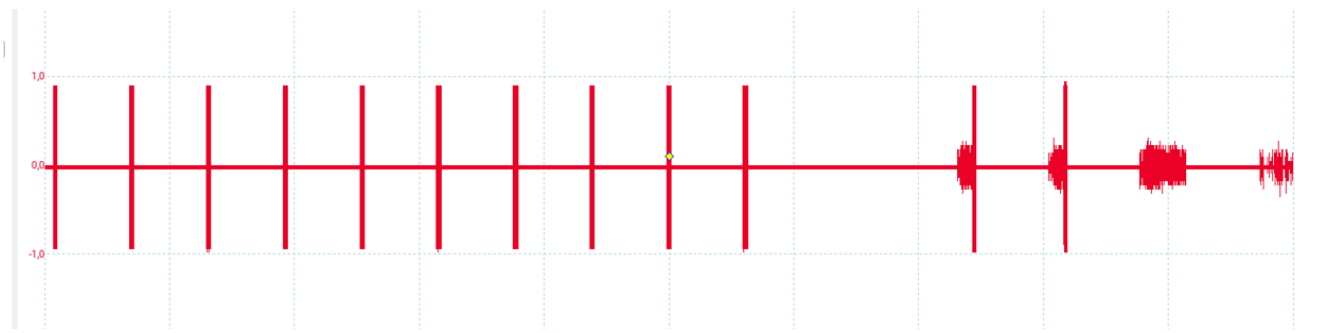

Figure 41. PN7160/1 NFC Polling when XTAL cannot start properly

7.3 XTAL references – CLRC663 plus Family

The recommended XTAL specification is provided in the CLRC663 plus Family product data sheet.

See the list of XTAL References in Table 10.

Table 10. XTAL references – CLRC663 plus Family

XTAL Manufacturer	XTAL Part Number	Note
MURATA	XRCGB27M120F3M10R0	-

7.4 XTAL references – PN5180

The recommended XTAL specification is provided in the PN5180 product data sheet.

See the list of XTAL References in Table 11.

Table 11. XTAL references – PN5180

XTAL Manufacturer	XTAL Part Number	Note
TXC	7M-27.120MEEQ-T	-

7.5 XTAL references – PN7462 Family

The recommended XTAL specification is provided in the PN7462 Family product data sheet.

See the list of XTAL References in Table 12.

Table 12. XTAL references – PN7462 Family

XTAL Manufacturer	XTAL Part Number	Note
EPSON	Q22FA12800034	-

8 Annex 1: XTAL start-up time simulations

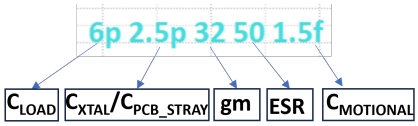

Figure 42. XTAL start-up – Legend

8.1 Different C_{LOAD}

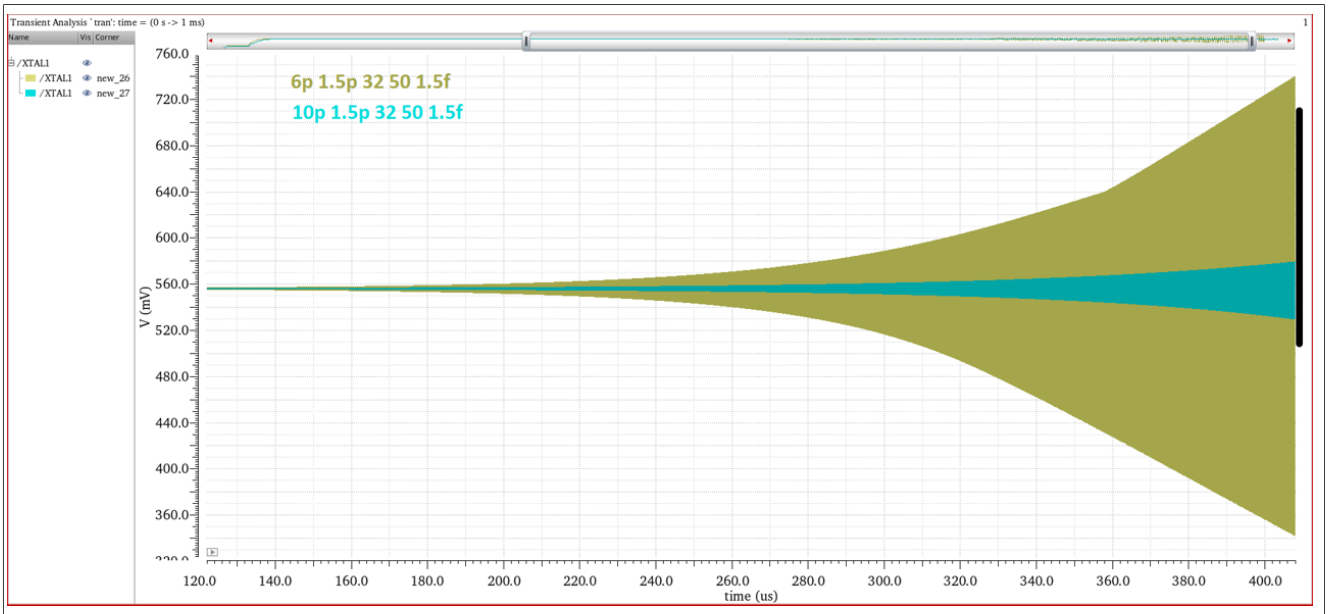

Figure 43. XTAL Start-Up, C_{LOAD} = 10 pF and 6 pF

8.2 Different $C_{MOTIONAL}$

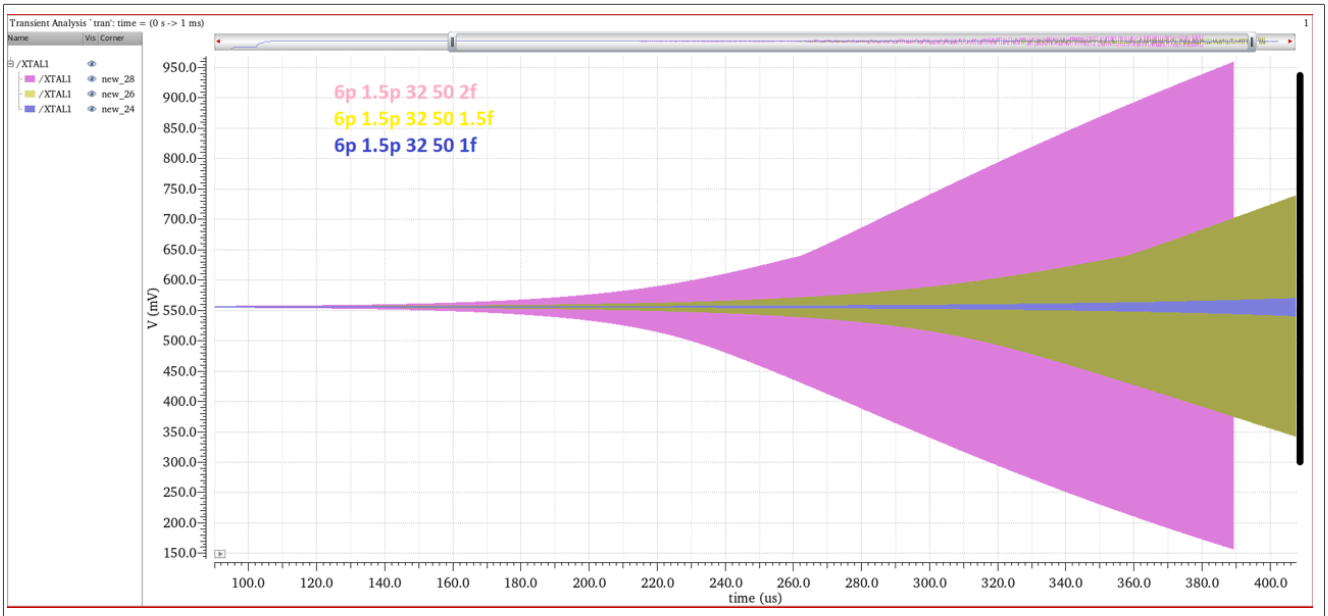

Figure 44. XTAL Start-Up, $C_{MOTIONAL}$ = 1 fF, 1.5 fF, 2 fF

8.3 Different C_{SHUNT}

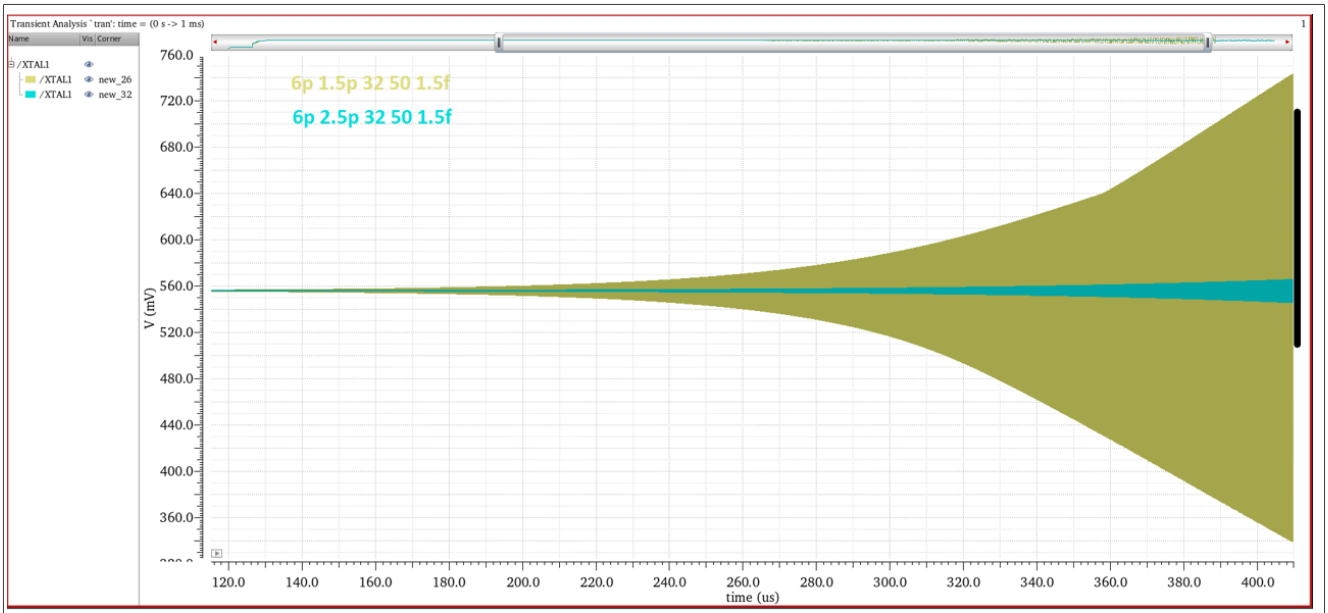

Figure 45. XTAL Start-Up, C_{XTAL} + C_{PCB_STRAY} = 1.5 pF and 2.5 pF

8.4 Different ESR

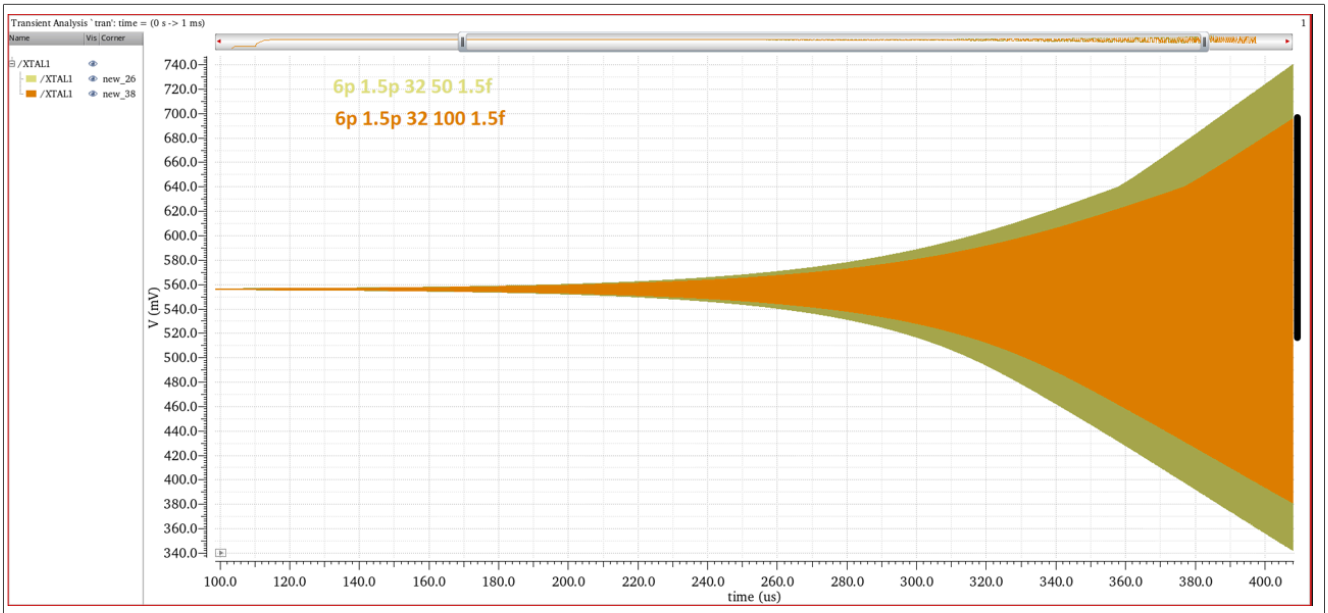

Figure 46. XTAL Start-Up, ESR = 50 Ω and 100 Ω

8.5 Different gm

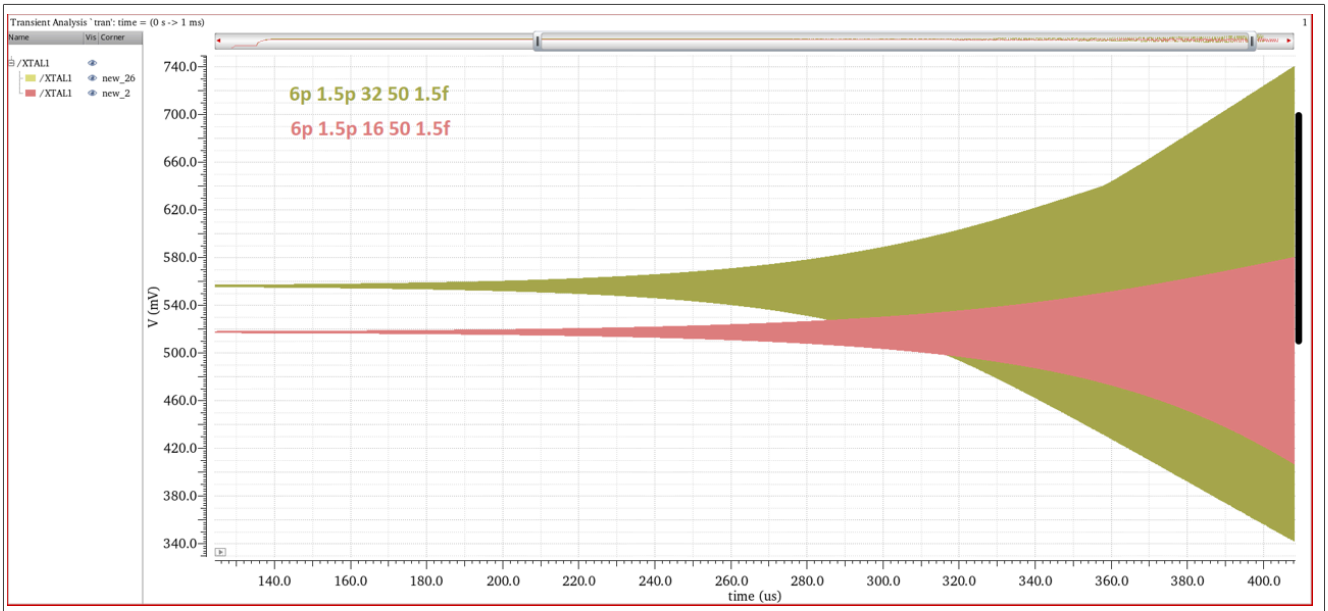

Figure 47. XTAL Start-Up, gm = 16 and 32

9 Annex 2: Buffer board

The measurement of the XTAL1 and XTAL2 signals requires a low capacitance active probe which might not always be available.

Users can build a simple “buffer board” which behaves very similar to the active probe. This board loads XTAL1 and XTAL2 with approximately1 pF.

See the schematic and setup it in Figure 48.

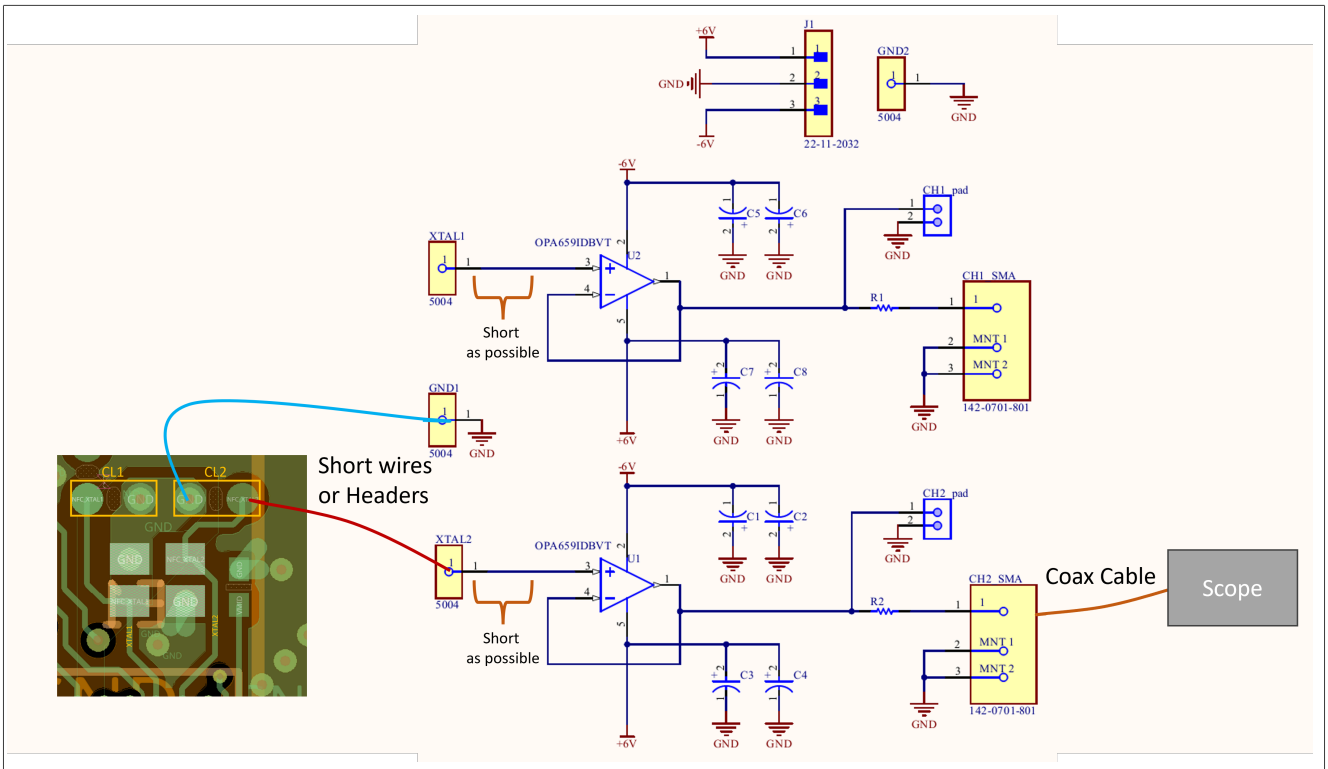

Figure 48. Buffer board schematic and setup

Note: *It is recommended to measure only one signal at a time (either XTAL1 or XTAL2). Measuring both simultaneously can affect the accuracy of the measurement.*

See the bill of materials used for the buffer board in the table below:

Table 13. Bill of materials

Identifier	Description	Value/Part number
U1, U2	JFET input amplifier	OPA659IDBVT
C5, C7, C1, C3	Tantalum caps	293D106X9035D2TE3
C6, C8, C2, C4	Tantalum caps	T494A104M035AH
R1, R2	Resistor	50 Ω
J1	Header	2.54mm Header
CH1_SMA, CH2_SMA	SMA Connector	–

Figure 49 shows an example of the buffer board designed for the PN5190 EVK.

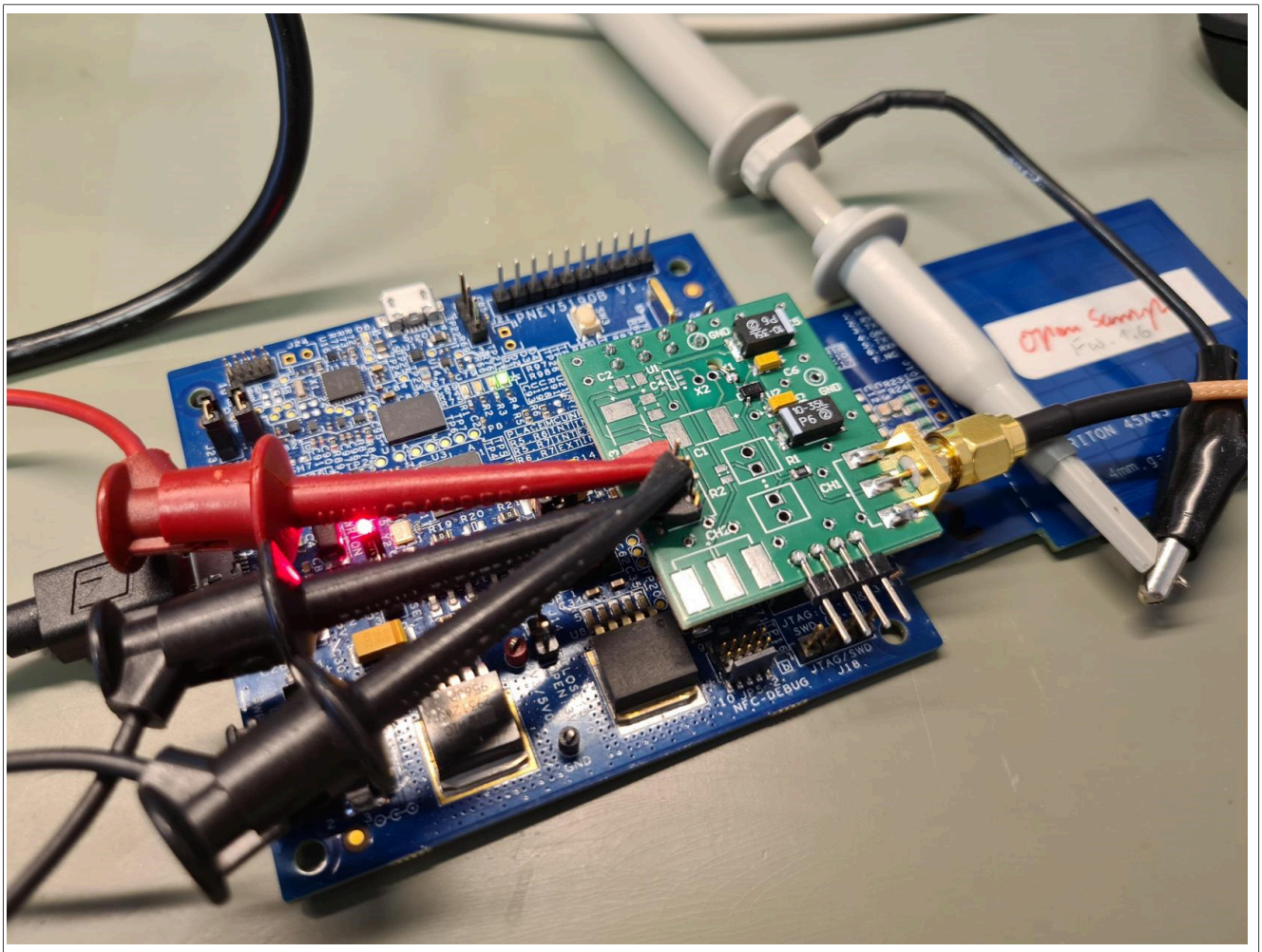

Figure 49. PN5190 EVK + buffer board

Figure 50 shows an XTAL2 waveform during ULPCD capture using the buffer board.

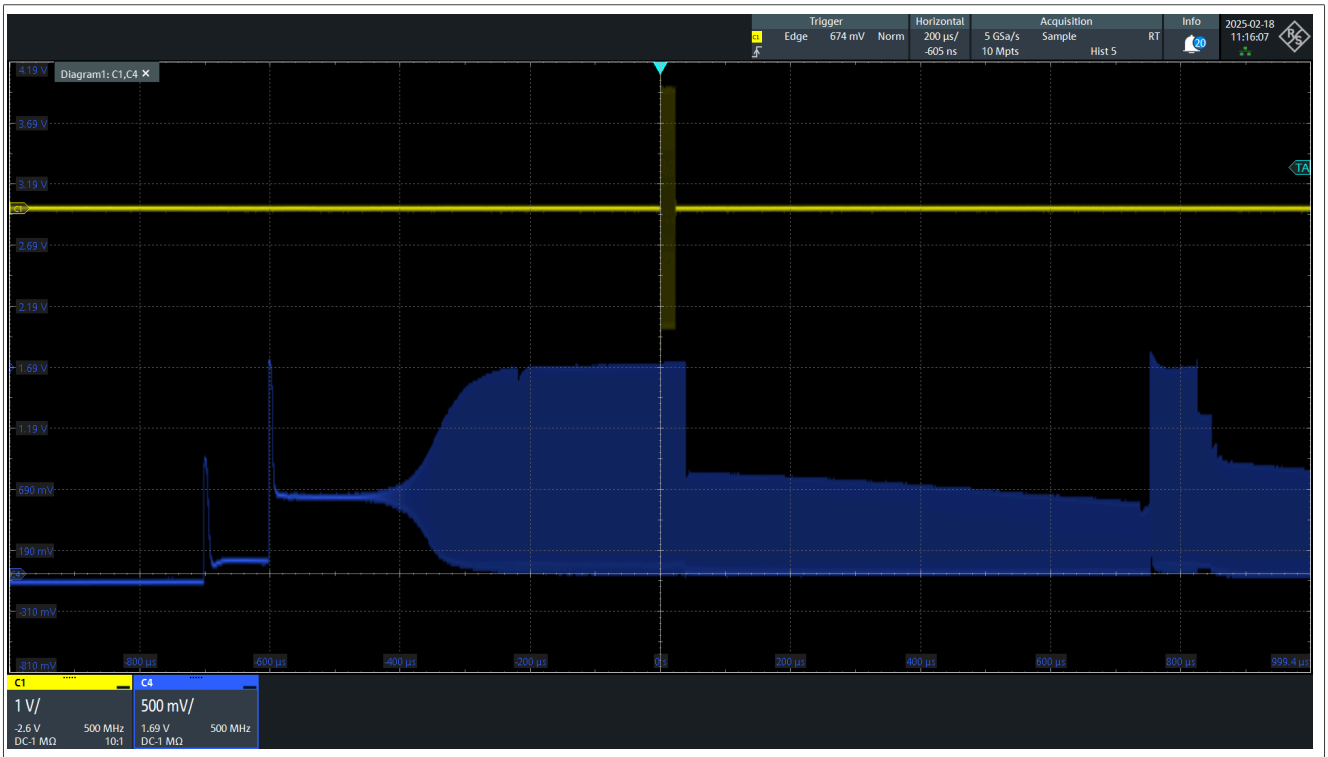

Figure 50. XTAL waveform measured by buffer board (Yellow – RF Field, Blue – XTAL2)

10 Annex 3: PN5190 B1 - ULPCD XTAL oscillator damping

Würth Elektronik / IQD PN: 830108212709 (LFXTAL094650) and **ABRACON PN: ABM11W-27.1200MHZ-8-D1X-T3** crystal units have very low ESR (High Q factor). This leads to the behavior that as soon as the crystal oscillator is disabled, the XTALs still maintain a high oscillation amplitude for a period of time before the amplitude sufficiently decreases.

This might be a problem for **PN5190 B1 in combination with ULPCD**. Therefore, users must use a damping resistor "***Rd***" as shown in Figure 51. This facilitates quicker damping of the crystal oscillator once it is turned off.

If the damping resistor is not used, the ULPCD application can fail in ULPCD Calibration/Card Detection with the following errors: *GPADC_ERROR, CLOCK_ERROR and XTAL_START_ERROR*.

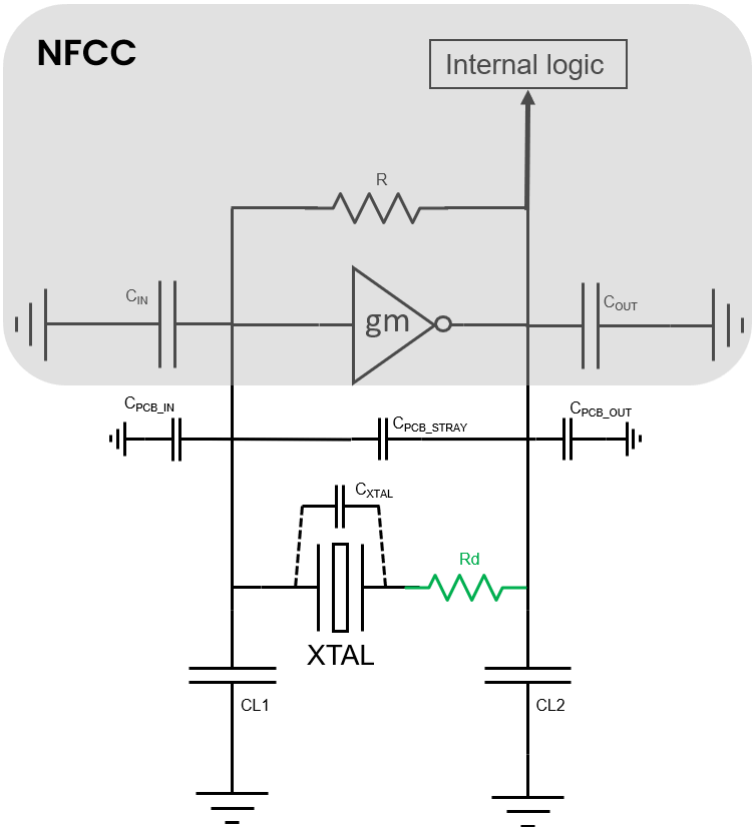

Figure 51. XTAL Oscillator setup for PN5190 B1 including damping resistor.

10.1 How to determine Rd resistor

Users must measure **XTAL1** Amplitude ("Calibration Amplitude") before “Normal IC boot” ($V_{CA(Vpp)}$) during ULPCD Calibration/Card Detection. This amplitude should be **600 mVpp +-10%**.

The measurement can be done with the help of the low capacitance active probe or Buffer board.

If the **($V_{CA(Vpp)}$) > 660 mVpp** , the user has to increase the "Rd" resistor.

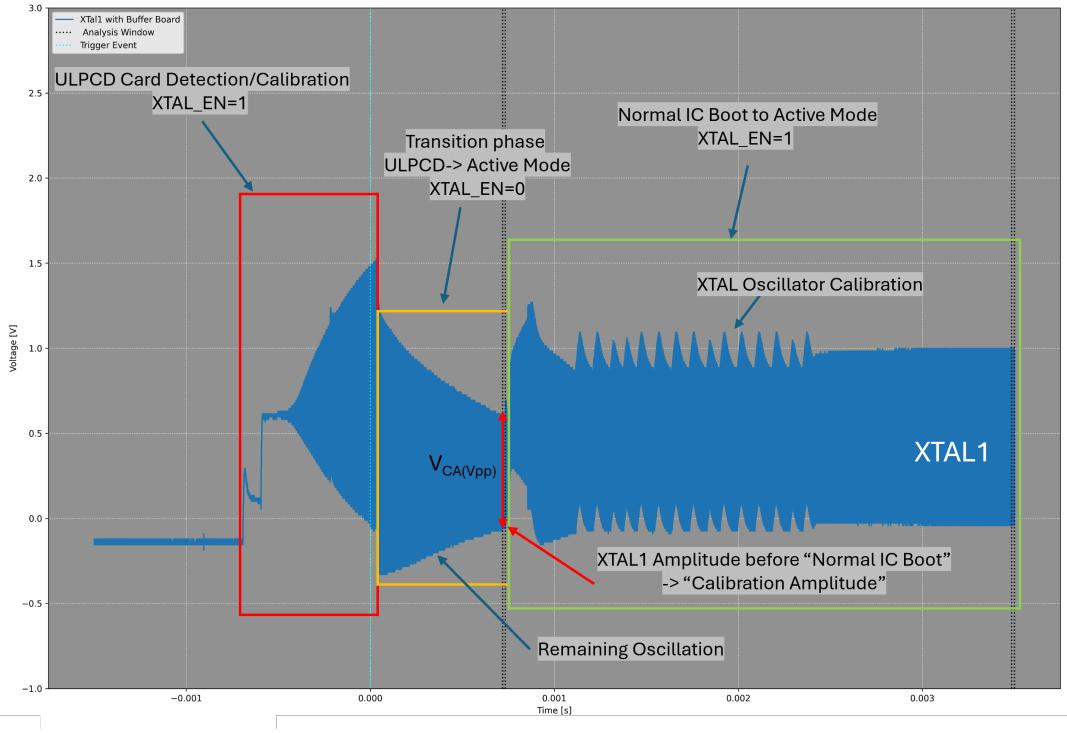

Figure 52. XTAL1 waveform during ULPCD Calibration/Card Detection

The amplitude measurement has to be done before a second XTAL start (before the first "glitch" in the waveform). See an example in Figure 53.

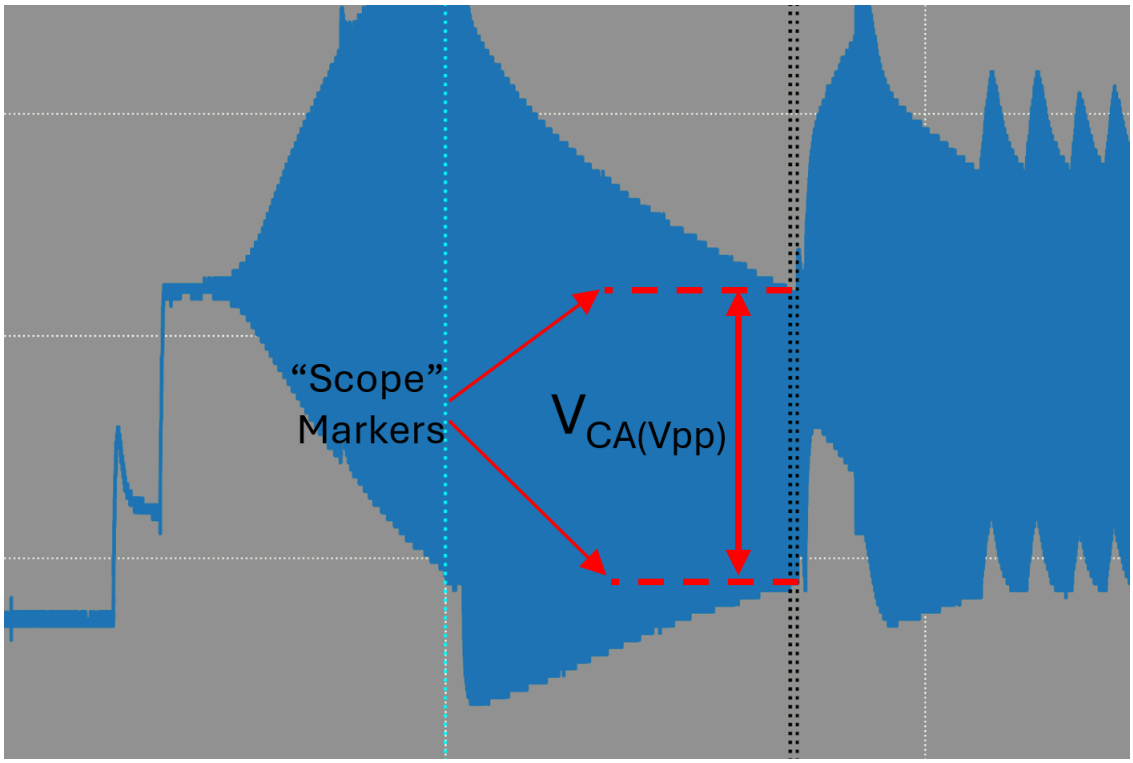

Figure 53. An Example of the "Calibration Amplitude" Measurement

Table Table 14 shows a reference "Rd" values for PN5190 B1 evaluation board. These values can serve as an initial reference for customer design.

Table 14. "Rd" values for PN5190 B1 evaluation board

XTAL name and part number	Rd value in Ω
Würth Elektronik / IQD PN: **830108212709 (LFXTAL094650)**	100
ABRACON PN: **ABM11W-27.1200MHZ-8-D1X-T3**	75

11 Abbreviations and acronyms

Table 15. Abbreviations and acronym

Acronym	Description
NFCC	NFC controller
ESR	Equivalent series resistance
XTAL	Crystal oscillator

12 References

[1] Data sheet – PN7160/PN7161: Near Field Communication (NFC) controller (link)
[2] Data sheet – CLRC663: High performance multi-protocol NFC frontend CLRC663 and CLRC663 plus (link)
[3] Data sheet – PN5180: High-performance multiprotocol full NFC frontend, supporting all NFC Forum modes (link)
[4] Data sheet – PN7462: NFC Cortex-M0 microcontroller (link)
[5] Data sheet – PN7642: Single-chip solution with high-performance NFC reader, customizable MCU, and security toolbox (link)
[6] Data sheet – PN5190B1: NFC frontend (link)
[7] Data sheet – PN5190B2: NFC frontend (link)
[8] Data sheet – PN7220: NFC controller with NCI interface supporting EMV and NFC Forum applications (link)
[9] Webpage – PN7160/PN7161: NFC Plug and Play Controller with Integrated Firmware and NCI Interface (link)
[10] Webpage – CLRC663 plus Family: High-Performance NFC Frontends (link)
[11] Webpage – PN5180: Full NFC Forum-Compliant Frontend IC (link)
[12] Webpage – PN7462: NFC Cortex®-M0 All-in-One Microcontroller with Optional Contact Interface for Access Control (link)
[13] Webpage – PN7642: Single-chip solution with high-performance NFC reader, customizable MCU, and security toolbox (link)
[14] Webpage – PN5190: NFC Frontend supporting challenging RF environment for payment, physical access control (link)
[15] Webpage – PN7220: High-Performance, One-Chip NFC Controller for EMVCo 3.1 and NFC Forum Operation (link)
[16] Software – NFC Cockpit Configuration Tool for NFC ICs (link)

13 Revision history

Table 16. Revision history

Document ID	Release date	Description
AN14518 v.4.0	9 September 2025	Editorial changes (typos, etc.). • Section 7.1 "XTAL references - PN5190/PN7642/PN7220": – Removed table "Other XTAL options for PN5190/PN7642/PN7220". – Added statement about "FA-118T 27. 1200MD50Z-K3".
AN14518 v.3.0	7 May 2025	Editorial changes. • Section 3.4.2 "Transconductance "gm" values ": updated. • Section 3.5 "Drive level ": – Removed Section "Drive level - check". – Section 3.5.1 "Drive level - Based on the crystal current": added. – Section 3.5.2 "Drive level - Based on the crystal voltage ": added. • Section 7.1 "XTAL references - PN5190/PN7642/PN7220": – Table 7: added ABM11W-27.1200MHZ-8-D1X-T3 and 830108212709 / LFXTAL094650. • Section 7.2 "XTAL references – PN7160/PN7161": – added Table 9. – added information regarding the XTAL start retry mechanism from firmware version 12.50.11 onward. – added Section 7.2.1 "PN7160/PN7160 - XTAL startup issue - Symptoms". • Section 9 "Annex 2: Buffer board": updated. • Section 10 "Annex 3: PN5190 B1 - ULPCD XTAL oscillator damping": added.
AN14518 v.2.0	5 March 2025	Editorial changes. Reworked document structure for better usability. • Section 4 "NXP crystal oscillator calculator ": added. • Section 5 "XTAL start-up": content and Figure 25 updated. • Section 5.2 "NFC Cockpit measurement for ULPCD with PN5190 and PN7642": added. • Section 5.3 "Measurement using test signals for ULPCD (PN7642 only)": added. • Section 6 "Layout recommendations": Figure 40 updated. • Section 7.1 "XTAL references - PN5190/PN7642/PN7220": – updated content. – Table 7: added CX1210SB27120B0HPRC1 and 8J27170002 • Section 9 "Annex 2: Buffer board": added. • Section 12 "References": updated.
AN14518 v.1.0	29 November 2024	• Initial version

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