AN14153

How to Link ADC Channel 0 with Internal Voltage Reference Source on LPC86x

Rev. 1.0 — 11 December 2023 Application note

Document information

Information	Content
Keywords	AN14153, LPC86x, ADC, LPCXpresso860-MAX, channel 0
Abstract	This application note describes how to connect LPC86x ADC input channel 0 with an internal 0.9 V voltage reference source.

1 Introduction

This application note describes how to connect LPC86x ADC input channel 0 (CH0) with the internal 0.9 V V-reference source (internal voltage reference). This is a new feature on LPC86x. The previous LPC8xx series does not have an internal band gap source that can be used for ADC V-reference. Without the internal V-reference source, LPC8xx cannot easily achieve certain use cases like detecting an external power source (for example, Li-ion battery) voltage value.

Note: *If this feature is enabled, the switch matrix must enable the pin PIO0_7 as ADC0 CH0. Pin PIO0_7 cannot be used for other digital functions. It is suggested to connect an external 0.1 µF capacitor with PIO0_7.*

1.1 How to link ADC CH0 to an internal voltage reference

LPC86x can enable internal voltage reference by the `SYSCON->PDRUNCFG` register:

- To disable the internal voltage reference, set `SYSCON->PDRUNCFG` bit 10 as 1
- To enable internal voltage reference, clear `SYSCON->PDRUNCFG` bit 10 to 0

Refer the code as follows:

```
SYSCON->PDRUNCFG   &= 0xFFFFFBFF;    // Bit 10, Set 1 Power down PMU Vref2ADC, Set 0
 Powered PMU Vref2ADC
```

On LPC86x, ADC input CH0 can be linked with an internal 0.9 V V-reference source by the `SYSCON->FCLKSEL[3]` register (address is `0x4004 809C`). For the system configuration register group, the offset is `0x09C`.

To enable the ADC CH0 link with internal voltage reference, the user must set `SYSCON->FCLKSEL[3]` bit 0 as 1 and bit 1 as 0. Clean bit 0 and bit 1 or set bit 0 and bit 1 disables this feature. Refer the code as follows:

```
SYSCON->FCLKSEL[3] &= 0xFFFFFFFC;    // Clean the ADC CH0 link with PMU Vref2ADC enable/
disable register bit in SYSCON->FCLKSEL[3] bit 0 and bit 1
SYSCON->FCLKSEL[3] |= 0x01;          // Enable ADC CH0 linked with PMU Vref2ADC by set
 SYSCON->FCLKSEL[3] bit 1 as 0, bit 0 as 1
```

1.2 Internal voltage reference and dynamic characteristics

The internal voltage reference specification of LPC86x ADC CH0 is the same as the internal voltage reference of the comparator. For more information, refer to the chapter *Comparator and internal voltage reference* (document LPC86x data sheet).

T_{amb} = -40 °C to +105 °C; V_{DD} = 3.3 V;

Table 1. Internal voltage reference static and dynamic characteristics

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
V_o	Output voltage	T_{amb} = -40 °C to 105 °C	860	-	940	mV
		T_{amb} = 25 °C		904		mV

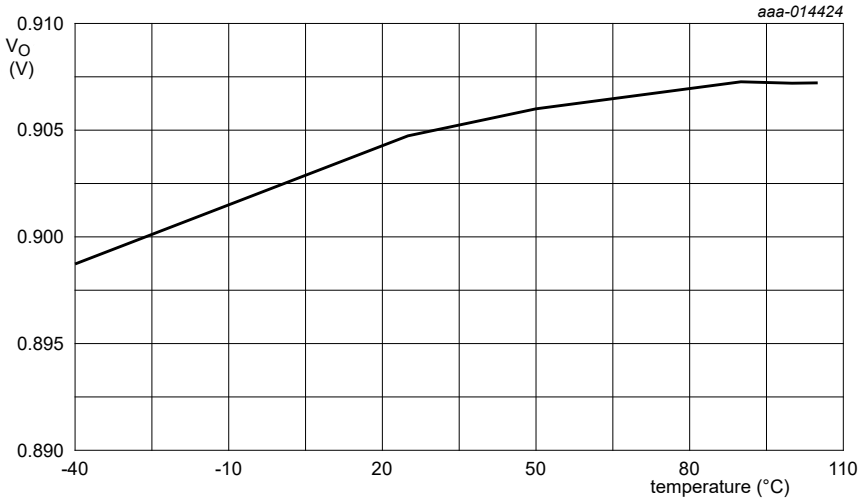

Figure 1. Typical internal voltage reference output voltage

1.3 How to get an internal voltage reference default value

The internal voltage reference value is different for different chips. LPC86x measurement ADC CH0 internal voltage reference value in factory calibration under room temperature is saved with part ID of LPC86x.

Table 2. Device ID register values

Part number	Part ID
LPC865M201JBD64/00	0xnnnn8651
LPC865M201JHI48/00	0xnnnn8652
LPC865M201JHI33/00	0xnnnn8654

The first 4 characters (0xnnnn) in part ID is the internal voltage reference default value under room temperature with mV as the unit. To get the default value, the 0xnnnn must convert from hexadecimal to decimal. For example, if the 0xnnnn = 0x037F = 895 mV, the default internal voltage value is 0.895 Volts.

2 Implementation

To get the internal voltage reference value by ADC CH0, the example code is based on the SDK example:

`\SDK_2_13_0_LPCXpresso860MAX\boards\lpcxpresso860max\driver_examples\adc\lpc_adc_basic`

Ensure that the user is familiar with the above example and related hardware (LPCXpresso860-MAX).

To get the internal voltage reference value, perform the following steps:

1. Include `fsl_iap.c` and `fsl_iap.h` into the `lpc_adc_basic` project, and add `#include "fsl_iap.h"` in `fsl_adc_basic.c`:

```
/* Read part identification number to get the PMU voltage reference default value */
status = IAP_ReadPartID(&partID);
if (status == kStatus_IAP_Success) {
PRINTF("\r\nPartID value:\t%X\r\n", partID);
PRINTF("\r\nPartID:\t%X\r\n", partID&0x00FFFF);
PRINTF("\r\nInternal Voltage Reference:\t%d\r\n", (partID>>16)&0x00FFFF);
}
```

2. Configure PIO0_7 as ADC CH0 by switch matrix:

```
/* ADC_CHN0 connect to P0_7 */
SWM_SetFixedPinSelect(SWM0, kSWM_ADC_CHN0, true);
```

3. Attach right clock source to ADC and enable ADC from Power-down mode:

```
CLOCK_Select(kADC_Clk_From_Fro); // Attach FRO clock to ADC0
CLOCK_SetClkDivider(kCLOCK_DivAdcClk, 1U);
POWER_DisablePD(kPDRUNCFG_PD_ADC0); // Power on ADC0
```

4. To enable ADC CH0, configure the ADC block by calling `ADC_Configuration()`.
5. Power up the internal voltage reference by setting `SYSCON->PDRUNCFG`:

```
SYSCON->PDRUNCFG &= 0xFFFFFBFF; // Bit 10, Set 1 Power down PMU Vref2ADC, Set 0
 Powered PMU Vref2ADC
```

6. To link ADC CH0 with the internal voltage reference, configure `SYSCON > FCLKSEL[3]` as `0x01`:

```
SYSCON->FCLKSEL[3] &= 0xFFFFFFFC; // Clean the ADC CH0 link with PMU Vref2ADC enable/
disable register bit in SYSCON->FCLKSEL[3] bit 0 and bit 1
SYSCON->FCLKSEL[3] |= 0x01; // Enable ADC CH0 linked with PMU Vref2ADC by set SYSCON-
>FCLKSEL[3] bit 1 as 0, bit 0 as 1
```

7. Read the ADC CH0 value by calling `API ADC_GetChannelConversionResult()`, after the software trigger ADC conversion.

2.1 Running the demo

To compile the example code in this application note or replace the `int main(void)` source code with appendix content, perform the following steps:

1. Add `include <fsl_iap.h>` in the source code.
2. Compile and download the code.
3. Open UART terminal with 9600-N-8-N-1.
4. To run the code, press the RESET button. The welcome log displays, as shown in Figure 2.

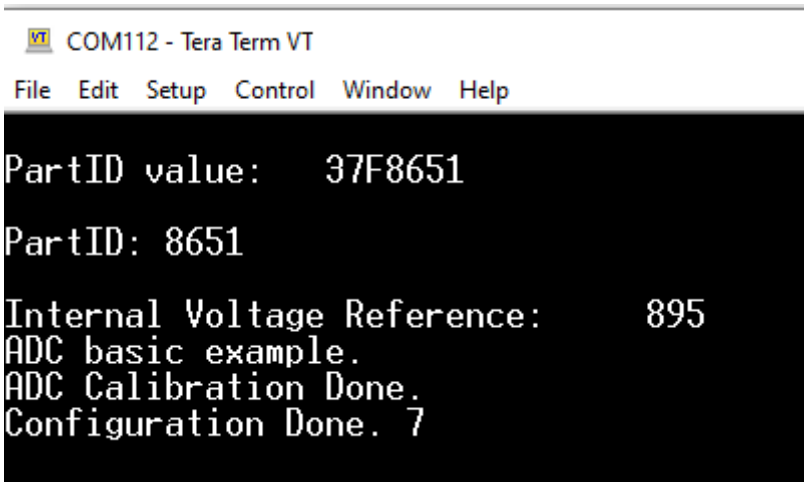

Figure 2. ADC reads internal voltage reference value

5. To start the ADC conversion test, press any key. The program automatically calculates conversion time and speed. The result displayed on the UART terminal is shown in Figure 3.

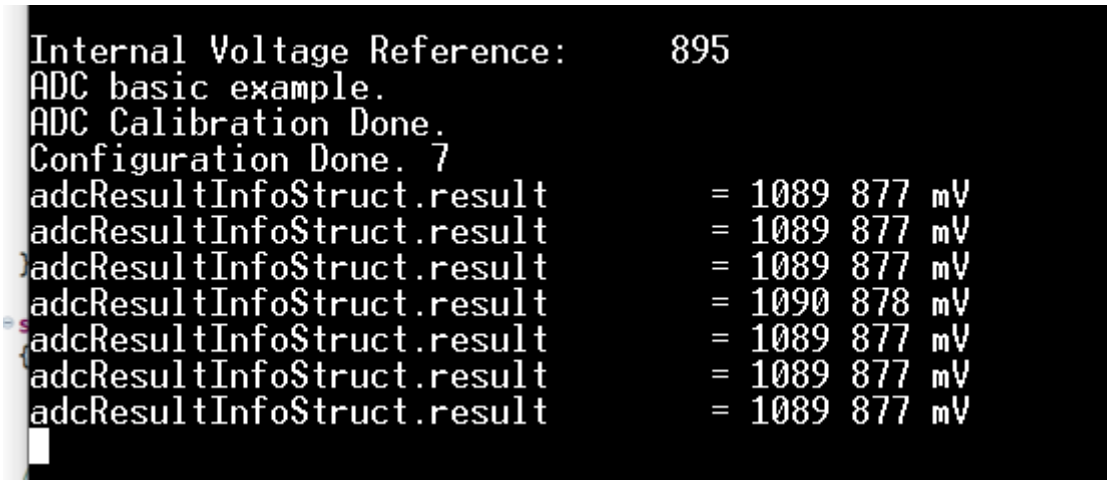

Figure 3. ADC sample rate result in UART terminal

3 Main source code

The main() source code is given below. The user can replace the `int main(void)` in `fsl_adc_basic.c`, then test the ADC CH0 link with the internal voltage reference.

```
int main(void)
{
    status_t status;
    uint32_t partID;
    /* Attach clock to USART0 (debug console) */
    CLOCK_Select(BOARD_DEBUG_USART_CLK_ATTACH);
    BOARD_InitBootPins();
    BOARD_BootClockFRO30M();
    BOARD_InitDebugConsole();
    /* Read part identification number to get the PMU voltage reference default value */
    status = IAP_ReadPartID(&partID);
    if (status == kStatus_IAP_Success)
    {
      PRINTF("\r\nPartID value:\t%X\r\n", partID);
      PRINTF("\r\nPartID:\t%X\r\n", partID&0x00FFFF);
      PRINTF("\r\nInternal Voltage Reference:\t%d\r\n", (partID>>16)&0x00FFFF);
    }
    CLOCK_Select(kADC_Clk_From_Fro); // Attach FRO clock to ADC0
    CLOCK_SetClkDivider(kCLOCK_DivAdcClk, 1U);
    POWER_DisablePD(kPDRUNCFG_PD_ADC0); // Power on ADC0
    uint32_t frequency = 0U;
    /* Calibration after power up. */
    frequency = CLOCK_GetFreq(DEMO_ADC_CLOCK_SOURCE) /
 CLOCK_GetClkDivider(kCLOCK_DivAdcClk);
    if (true == ADC_DoSelfCalibration(DEMO_ADC_BASE, frequency))
    {
    PRINTF("ADC Calibration Done.\r\n");
    }
    /* Configure the converter and work mode. */
    ADC_Configuration();
    PRINTF("Configuration Done. %x\r\n", SYSCON->FCLKSEL[3]);
    SYSCON->PDRUNCFG &= 0xFFFFFBFF; // Bit 10, Set 1 Power down PMU Vref2ADC, Set 0
 Powered PMU Vref2ADC
    SYSCON->FCLKSEL[3] &= 0xFFFFFFFC; // Clean the ADC CH0 link with PMU Vref2ADC enable/
disable register bit in SYSCON->FCLKSEL[3] bit 0 and bit 1
    SYSCON->FCLKSEL[3] |= 0x01; // Enable ADC CH0 linked with PMU Vref2ADC by set SYSCON-
>FCLKSEL[3] bit 1 as 0, bit 0 as 1
    while (1)
```

```
    {
    /* Get the input from terminal and trigger the converter by software. */
    GETCHAR();
    ADC_DoSoftwareTriggerConvSeqA(DEMO_ADC_BASE);
    /* Wait for the converter to be done. */
    while (!ADC_GetChannelConversionResult(DEMO_ADC_BASE, DEMO_ADC_SAMPLE_CHANNEL_NUMBER,
 &adcResultInfoStruct))
    {
    }
    PRINTF("adcResultInfoStruct.result = %d %d mV\r\n", adcResultInfoStruct.result,
 (adcResultInfoStruct.result*3300/4096));
    }
}
```

4 Conclusion

This application note provides the example code to evaluate ADC CH0 linked with an internal 0.9 V voltage reference. The result shows that after powering up the internal 0.9 V internal voltage reference and linking ADC CH0 with this source, the ADC can read the internal voltage reference value from CH0.

5 Reference

Table 3 lists and explains the additional documents that can be referred for more information. Some of the documents listed below are available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer (FAE) or sales representative.

Table 3. References

Document	Link/how to access
LPC86x User Manual (UM11607)	UM11607.pdf
LPC86x Data Sheet	LPC86x.pdf

6 Note about the source code in the document

Example code shown in this document has the following copyright and BSD-3-Clause license:

Copyright 2023 NXP Redistribution and use in source and binary forms, with or without modification, are permitted provided that the following conditions are met:

1. Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer.
2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer in the documentation and/or other materials provided with the distribution.
3. Neither the name of the copyright holder nor the names of its contributors may be used to endorse or promote products derived from this software without specific prior written permission.

THIS SOFTWARE IS PROVIDED BY THE COPYRIGHT HOLDERS AND CONTRIBUTORS "AS IS" AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL THE COPYRIGHT HOLDER OR CONTRIBUTORS BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN

ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

7 Revision history

Table 3 summarizes the revisions to this document.

Table 4. Revision history

Revision number	Release date	Description
1	11 December 2023	Initial public release

Legal information

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Contents

For more information, please visit: https://www.nxp.com

Date of release: 11 December 2023
Document identifier: AN14153