AN14102

Industrial application measurements using NXP AFE

Rev. 1.1 — 30 November 2023 Application note

Document information

Information	Content
Keywords	NAFExx388, industrial, multichannel, universal, analog front-end (AFE), high-precision, temperature measurement, load cell, thermocouple, 4 mA-20 mA, RTD
Abstract	The NAFExx388 is a highly configurable industrial-grade multichannel universal input analog front-end (AFE) that meets high-precision voltage/current measurement requirements for industrial applications.

1 Introduction

The NAFE (NXP AFE) is a highly configurable industrial-grade multichannel universal input analog front-end (AFE) that meets high-precision measurement requirements. The device integrates low-leakage, high-voltage (HV) fast multiplexers, low-offset and low-drift programmable gain amplifier (PGA) and buffers, high data-rate 24-bit sigma-delta analog-to-digital converter (ADC), precise voltage and current excitation source, and low-drift voltage reference. All HV analog pins are diode-protected internally for electromagnetic compatibility (EMC), which simplifies the system design bill of material (BOM) requirement. The NAFE is equipped with various diagnostic and supplies supervisory circuitry for condition monitoring and anomaly detection. The NAFE also integrates two precise calibration voltage sources for ease of end-to-end system self-calibration. These features help to predict maintenance and avoid abrupt and costly downtime. The universality of the NAFE family of products allows its application to a variety of industrial applications, such as programmable logic controllers (PLCs), I/O modules, data loggers, instrumentation, high-precision sensor, data acquisition systems, and so on.

This article discusses systems-level implementation of voltage and current sensing, temperature and weight scale measurements, and system diagnostics using the NAFE13388EVB (evaluation board) and GUI.

1.1 NAFE product family

NAFE	1	3	3	8	8
	1: Low power 7: High speed	1: No VIEX 3: VIEX	1: No Cal 3: Factory calibrated	4: 16 bit 8: 24 bit	4: 4-ch 8: 8-ch

Contact the NXP factory or an NXP sales representative to get further information and available part numbers.

1.2 NAFE features

- Eight configurable HV inputs
  - Single-ended or differential, with ranges up to ±25 V
  - Independent configurations for voltage, current, resistance, resistance temperature detector (RTD), thermocouple
  - Overvoltage protected up to ±36 V for less than one hour
- Programmable gain: x0.2 to x16
- Fast data rates
  - 7.5 SPS to 288 kSPS
  - Simultaneous 50 Hz/60 Hz line rejection
  - ENOB: 17 bit at 72 kSPS
- High accuracy
  - 0.005 % FS accuracy at room after user calibration
  - 0.1 % FS accuracy over -25 °C to 105 °C
- System calibration
  - End-to-end calibration with integrated precise voltage sources
  - Accurate factory-calibrated products are available
- ±3 °C internal temperature sensor
- Precise excitation voltage and current sources
- 0.2 % internal oscillator accuracy at room temperature
- Diagnostic system for fault detection and prediction
- CRC error detection
- Ten GPIOs
- 32 MHz SPI interface
- Robust 7.5 kV HBM ESD and IEC61000-4-5 2 kV surge protection
- Power supply: HV: ±7 V to ±24 V, LV: 3.3 V
- 150 mW low-power consumption
- Operating temperature range TA: -40 °C to +125 °C
- Package: 64 pin, 9 mm x 9 mm x 0.85 mm HVQFN

2 Applications

The following sections discuss various system-level applications and show their implementation using the NAFE13388EVB (evaluation board) and GUI.

2.1 Self diagnostic

The NAFE family of products has an in-built, low-voltage multiplexer (LVMUX) that routes the internal node voltages (scaled HVDD and HVSS, AVDD, VREF_Coarse, GPIO0-GPIO1) to the ADC input to run self diagnostic without an external measuring unit. This ability to sense an internal node in conjunction with the flexible and configurable global alarm gives the user the ability to create a power-up, self-diagnostic sequence by assigning diagnostic signals of interest to different logic channels and running a multichannel conversion command.

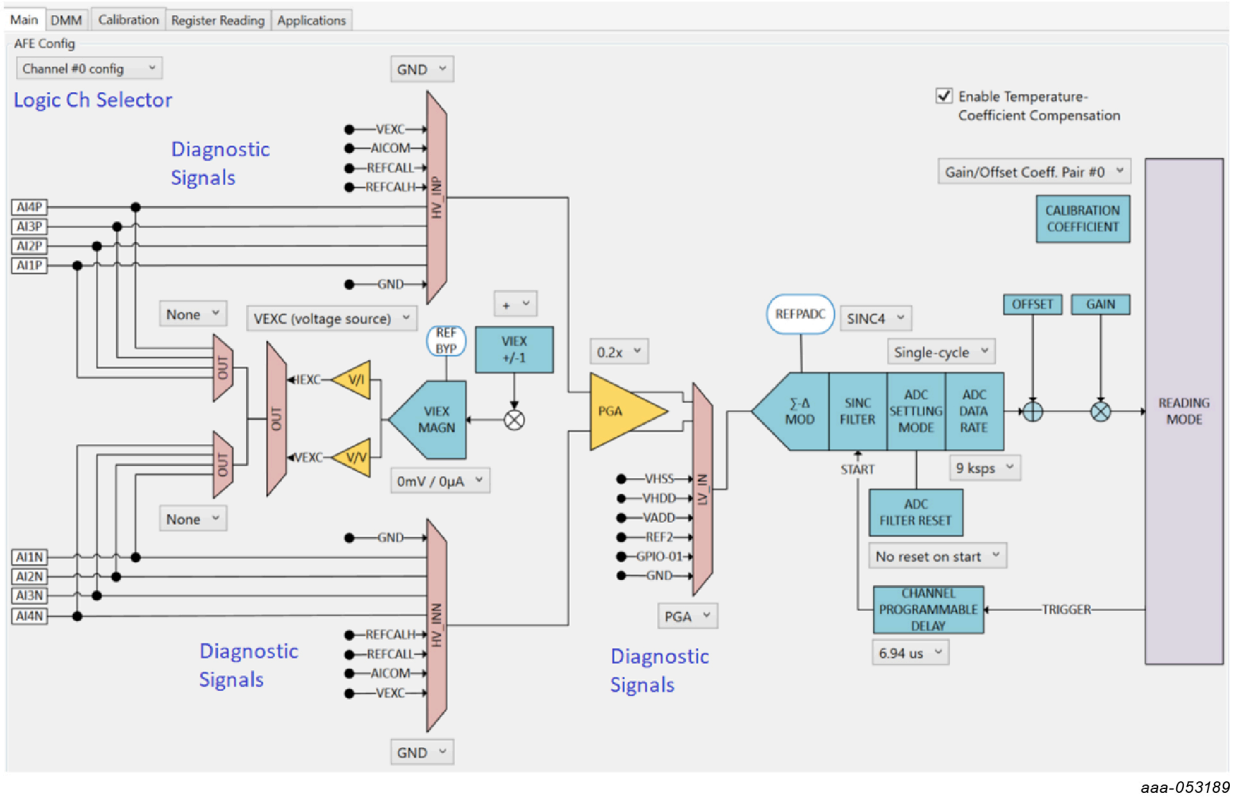


Figure 1. NAFE13388 block diagram

2.2 Voltage sensing

NAFE product family offers maximum eight inputs. Each of these inputs can be used independently (Single-ended mode) or in pairs (Differential mode). Single-ended mode can be used to monitor up to eight application-key voltage levels, such as voltage reference, power rail, or transductor output. Differential mode can be used to monitor up to four differential signals, such as voltages across a sensor.

Below is an example block diagram of an industrial application where NAFE is used to measure signals from different field instruments.

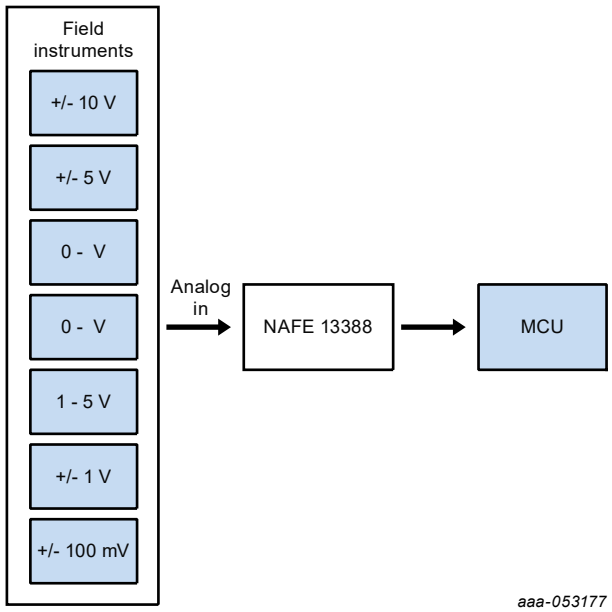


Figure 2. Example for voltage sensing using NAFE

The NAFE product family provides 16 logic channels (different from eight physical input channels) to allow 16 different channel configurations and once these unique configurations are defined, the user can seamlessly switch between different configurations, avoiding the additional SPI transaction overhead.

Gain is configured based on the system input range requirement (See Table 26):

Table 1 shows the logic channel assignment and configuration for the example hardware application mentioned above:

Table 1. Logic channels assignment and gain selection for Vsense

Industrial signals are ±10, ±5, Uni 0-10, 0-5, 1-5, ±1 V, ±100 mV

Logic channel	Mapping	Input signal (V)	Gain (V/V)	NAFE AIN range (V)	NAFE FS (V)
0	AI1P-AICOM	±10	0.2X	±10	±12.5
1	AI1N-AICOM	±5	0.4X	±5	±6.25
2	AI2P-AICOM	0-10	0.2X	±10	±12.5
3	AI1N-AICOM	0-5	0.4X	±5	±6.25
4	AI3P-AICOM	1-5	0.4X	±5	±6.25
5	AI3N-AICOM	±1	2X	±1	±1.25
6	AI4P-AI4N	0.100	16X	±0.125	±0.156

The NAFE13388 features a digital filter that provides a 50 Hz and 60 Hz Normal mode rejection (NMR).

Figure 3 shows the SINC4 filter NMR at the date rate of 10 sps, 50 sps, and 60 sps.

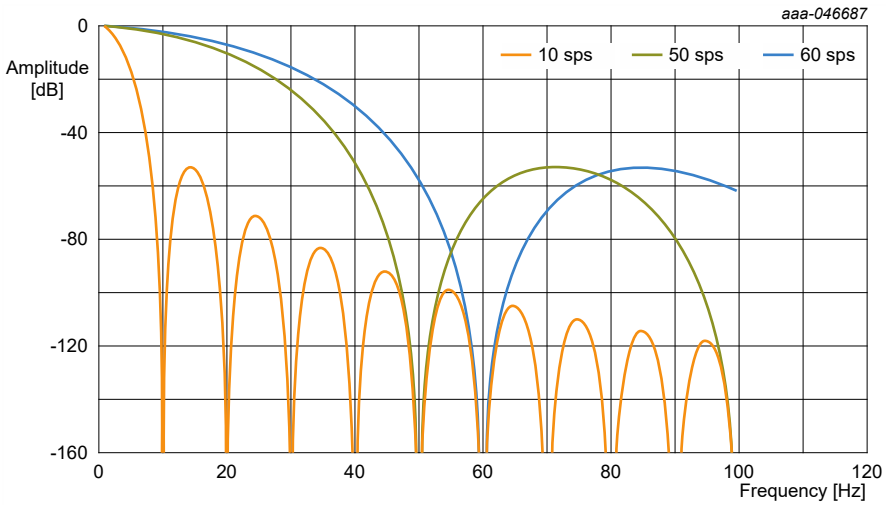


Figure 3. SINC Normal mode rejection vs frequency vs data rata

Data rate/ADC sinc selection is based on signal level and noise tolerance (see Table 26):

Table 2. Logic channels data rate selection for Vsense

Logic channel	Gain (V)	Sinc	Data rate (sps)	Noise (uVrms)	ENOB
0	0.2X	SINC4	12000	53.6	19.8
1	0.4X	SINC4	12000	26.8	19.8
2	0.2X	SINC4	24000	76.3	19.3
3	0.4X	SINC4	24000	38.2	19.3
4	0.4X	SINC4	6000	19	20.3
5	2X	SINC4	6000	4	20.3
6	16X	SINC4 + SINC1	50	0.13	21.9

Channel delay configuration: Channel delay must honor the Tswitch time of 16.4 µs and 8.2 µs, for low-power and high-speed NAFE parts, respectively. If a system is designed, for example, with the NAFE13388, Table 3 shows the corresponding reading time for each channel configuration.

T_reading = T_fixed + T_prog_delay + T_conv

Where, T_fixed = (2 × T_sys_clk) ± 1 × T_sys_clk for first reading,

T_fixed = 0 for subsequent readings.

With this configuration of delay, the reading times (*T_reading* = *T_prog_delay* + *T_conv*) are:

Table 3. Logic channels read time for Vsense

Logic Channel	Data rate (sps)	Conversion period (s)	Channel delay (s)	Read time
0	12000	83.3E-6	16.5E-6	99.8E-6
1	12000	83.3E-6	16.5E-6	99.8E-6
2	24000	41.7E-6	16.5E-6	58.2E-6
3	24000	41.7E-6	16.5E-6	58.2E-6
4	6000	166.7E-6	33.4E-6	200.1E-6
5	6000	166.7E-6	33.4E-6	200.1E-6
6	50	20.0E-3	16.5E-6	20.016E-3

The requested time to complete one cycle of multichannel conversion is 20.70 ms, which is primarily driven by the small signal measurement requirements at Logic channel 6. See Table 27 for popular reading times.

The above selections are configured in the following NAFE registers:

- CH_CONFIG0 (Signal mapping and Gain)
- CH_CONFIG1 (Data rate and Sinc)
- CH_CONFIG2 (Channel delay)

Table 4. Register configuration for Vsense

Register name	Field	Field value [Hex]							Register value [Hex]						
		CH0	*CH1*	*CH2*	*CH3*	*CH4*	*CH5*	*CH6*	*CH0*	*CH1*	*CH2*	*CH3*	*CH4*	*CH5*	*CH6*
CH_CONFIG0	HV_AIP[15:12]	1	7	2	2	3	7	4	1711	7131	2711	2731	3731	7391	44F1
	HV_AIN[11:8]	7	1	7	7	7	3	4							
	CH_GAIN[7:5]	0	1	0	1	1	4.	7							
	HV_SEL[4]	1	1	1	1	1	1	1							
	LVSIG_IN[3:1]	0	0	0	0	0	0	0							
	TCC_OFF[0]	1	1	1	1	1	1	1							
CH_CONFIG1	CH_CAL_ GAIN_ OFFSET[15:12]	0	1	0	1	1	4	7	28	1028	18	1018	1038	4038	7071
	CH_ THRS[11:8]	0	0	0	0	0	0	0							
	ADC_DATA_ RATE[7:3]	5	5	3	3	7	7	14							
	ADC_SINC[2:0]	0	0	0	0	0	0	1							
CH_CONFIG2	CH_ DELAY[15:10]	11	11	11	11	14	14	11	4400	4400	4400	4400	5000	5000	4400
	ADC_ NORMAL_ SETTLING[9]	0	0	0	0	0	0	0							
	ADC_FILTER_ RESET[8]	0	0	0	0	0	0	0							
	CH_CHOP[7]	0	0	0	0	0	0	0							

See Section 3.4 paragraph for system-level configuration options for the NAFE. The code to implement the above example setup is discussed and shared in "*NAFE Applications with MCU Expresso*".

2.3 Current sensing

Current sensing is used for several purposes in an electrical system, such as sensor, resistance reading, current consumption, power calculation, and so on. A current signal isn't affected by voltage drop in the loop wire and is less susceptible to noise pickup/cross talk than the voltage circuit. Current sensing is preferred over voltage signal, when the field instrument is far away from the data acquisition system (DAS) and programmable logic control unit (PLC). The NAFE requires an external precision resistor to utilize its input channels for measuring current via an external precision resistor. It is possible to sense up to four currents with differential input.

Consider an industrial system that uses the NAFE to sense signals from the pressure transmitter in the range of 4 mA to 20 mA of current corresponding to 0 bars to 10 bars of pressure, which means 2.5 bars (25%) of pressure is represented by 4 mA of current. A standard current signal of 4 mA to 20 mA has widespread acceptance in industrial applications because of the following reasons:

- Safety, as the technicians would feel no shock to touch 4 mA to 20mA when used with a nominal 24 VDC loop-power supply.
- Ease of measurement with wide choice of shunt resistor range (1 ohm to 500 ohm with 250 ohm being the most common).
- As 4 mA to 20 mA uses 4 mA as zero engineering unit (for example: 0 bar), it has inherent "live zero" for trouble shooting, which means 0 mA detection by DAS indicates a fault, such as a broken wire, high-wire resistance, noise, faulty transmitter, and so on.
- 4 mA meets the minimum 3 mA loop current analog transmitter requirement to operate and the 20 % bias rule (4 mA = 20 % of 20 mA). 20 mA is chosen to be below the dangerous threshold of 30 mA for the human heart and has the same ratio of 1:5 to meet pneumatic device ratios (3 psi to 15 psi).

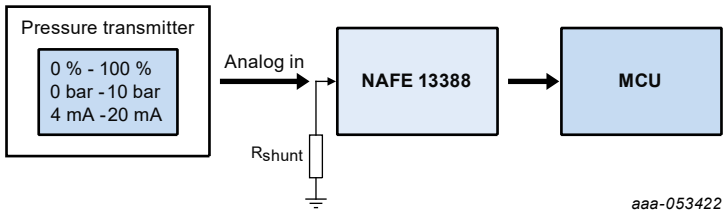


Figure 4. Current sensing

Consider the following when choosing a precision resistor:

- Current resolution
- Power dissipation of the resistor
- System and device limitations (for example, the device could not accept large shunt resistance)
- Voltage across the resistor should be within NAFE measurement range

Current resolution depends on the ADC voltage resolution and is inversely proportional to Rshunt value:

$$I_{Resolution} = \frac{V_{Resolution}}{R_{Shunt}}$$

Similarly, the following equation is used to select Rshunt of the appropriate voltage and power ratings: $P_{Shunt} = R_{Shunt} * I_{Max}^{2}$

$$V_{max} = R_{Shunt} * I_{Max}$$

Using the standard 250, 125, 100 ohm of Rshunt leads to the below system characterstics:

Table 5. System current requirement and options

Current requirement (mA)	Rshunt options (Ω)	Voltage range (V)	NAFE gain (V)	NAFE AIN range (V)	Voltage resolution (nV)	Current resolution (nA)
4-20	250	1-5	0.4X	±5	1500	6.00
4-20	125	0.5-2.5	0.8X	±2.5	745	5.96
4-20	100	0.4-2.0	1X	±2	596	5.96

Configuration of other NAFE parameter mapping and the reading times (*T_reading* = *T_prog_delay* + *T_conv*) are:

Table 6. Logic channel assignment for current sensing using 250 ohm

Logic channel	Signal	Mapping	Sinc	Data rate	Delay	Read time
0	Input current	AI4P-AI4N	SINC4	12000	16.5 us	99.8 us

Below is the register configuration to implement the above:

- CH_CONFIG0 (Signal mapping and Gain)
- CH_CONFIG1 (Data rate and Sinc)
- CH_CONFIG2 (Channel delay)

Table 7. Register configuration for current sensing using 250 ohm

Register name	Field	Field value [Hex]	Register value [Hex]
		CH0	*CH0*
CH_CONFIG0	HV_AIP[15:12]	4	4430
	HV_AIN[11:8]	4	
	CH_GAIN[7:5]	1	
	HV_SEL[4]	1	
	LVSIG_IN[3:1]	0	
	TCC_OFF[0]	0	
CH_CONFIG1	CH_CAL_GAIN_OFFSET[15:12]	1	1028
	CH_THRS[11:8]	0	
	ADC_DATA_RATE[7:3]	5	
	ADC_SINC[2:0]	0	
CH_CONFIG2	CH_DELAY[15:10]	11	4400
	ADC_NORMAL_SETTLING[9]	0	
	ADC_FILTER_RESET[8]	0	
	CH_CHOP[7]	0	

See Section 3.4 for system-level configuration options for the NAFE. The code to implement the above application setup is discussed and shared in "*NAFE Applications with MCU Expresso*".

2.4 Temperature sensing

Temperature is the most common physical quantity measured in industrial and factory environments. An electrical system can use several types of temperature sensors ranging, from integrated IC sensor (such as in NAFE13388) to external resistor temperature detector (RTD), thermocouple, and thermistors.

Though RTD and thermistors are both active measurement elements that vary resistance with temperature, the former is constructed of metal winding (platinum, copper, and so on) while the later consists of metal oxide semiconductor pressed into a container. On the other hand, thermocouples use unique pairing of dissimilar metals to create a junction to sense the temperature, which causes a voltage difference (Seebeck effect) in

accordance with the change in temperature. Below is the relative comparison of the three external temperature sensors:

Table 8. Relative comparison of thermistor, RTD and thermocouple

Features	Thermistors	RTD	Thermocouple
Sensitivity	Highest	Medium	Lowest
Temp range	Lowest (-40 °C to 250 °C)	Medium (-240 °C to 650 °C)	Highest (-210 °C to 1760 °C)
Accuracy	Medium	Highest	Medium
Linearity	Lowest	Highest	Medium
Stability	Lowest	Highest	Medium
Self-heating	Highest	Lowest	Not applicable
Cost	Medium	Highest	Lowest
Durability	Lowest	Medium	Highest

RTD: RTD is offered in 2, 3, or 4 wires configuration. An external circuit called a "signal conditioning circuit" is needed to sense the resistance, some of these types will be discussed below using the NAFE.

2.4.1 2-wire RTD

This is the simplest and cheapest topology, where known current injected through the RTD and voltage across the RTD is measured.

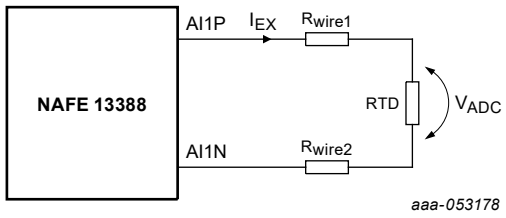


Figure 5. 2-wires RTD connection to NAFE

Pros:

- No additional passive components are needed.
- Cheaper RTD, having only two wires.
- Only two channels of the NAFE are needed.

Cons:

- As the same terminals are used to inject current and read voltage, addition of lead wire resistance to the element resistance leads to measurement inaccuracy (higher temperature reporting). So, it is advisable to keep the lead length shortest for a 2-wire application.

2.4.2 NAFE configuration for 2-wire RTD

The NAFE13388 has integrated VIEX (voltage current excitation sources) that can be programmed to pre-defined levels of voltages or current. VIEX can be used to excite the external sensor and the source magnitude, polarity, and output pins can be configured using CH_CONFIG3 register as below:

- Select the excitation source, current or voltage (VIEX_VI)
- Excitation polarity (VIEX_POL)
- Excitation V/I source magnitude (VIEX_MAG)
- Output pin AIxP (VIEX_AIP_EN)
- Output pin AIxN (VIEX_AIN_EN)

The excitation source must be current source to excite the NTC. The excitation magnitude must be high enough to avoid the noise issue and low enough to avoid self-heating of the NTC, which makes 750 uA a good trade-off.

VIEX configuration:

Table 9. Logic channel VIEX selection

Logic channel	VIEX parameter	Value
0	Source	Current
	Polarity	Positive
	Magnitude	750 uA
	AIxP	AI1P
	AIxN	None

NAFE analog input channel configuration:

Table 10. Logic channel analog input selection

Logic channel	Mapping	Sinc	Data rate	Delay	Read time
0	AI1P to AI1N	SINC4 + 1	50	0	20 ms

Below is the register configuration to implement the above:

- CH_CONFIG0 (Signal mapping and Gain)
- CH_CONFIG1 (Data rate and Sinc)
- CH_CONFIG2 (Channel delay)
- CH_CONFIG3 (VIEX)

Table 11. Register configuration for 2-wire RTD

Register name	Field	Field value [Hex]	Register value [Hex]
		CH0	*CH0*
CH_CONFIG0	HV_AIP[15:12]	1	11B1
	HV_AIN[11:8]	1	
	CH_GAIN[7:5]	5	
	HV_SEL[4]	1	
	LVSIG_IN[3:1]	0	
	TCC_OFF[0]	1	
CH_CONFIG1	CH_CAL_GAIN_OFFSET[15:12]	5	50B1
	CH_THRS[11:8]	0	
	ADC_DATA_RATE[7:3]	16	
	ADC_SINC[2:0]	1	

Table 11. Register configuration for 2-wire RTD*...continued*

Register name	Field	Field value [Hex]	Register value [Hex]
		CH0	*CH0*
CH_CONFIG2	CH_DELAY[15:10]	B	2E80
	ADC_NORMAL_SETTLING[9]	1	
	ADC_FILTER_RESET[8]	0	
	CH_CHOP[7]	1	
CH_CONFIG3	VIEX_VI[15]	1	B008
	VIEX_POL[14]	0	
	VIEX_MAG[13:10]	C	
	VEXC_EN[9]	0	
	OPEN_DET_CURRENT[8]	0	
	VIEX_CHOP[6]	0	
	VIEX_AIP_EN[5:3]	1	
	VIEX_AIN_EN[2:0]	0	

The value of current through the RTD is known, so the resistance can be calculated (R = V/I) after measuring the voltage across it by the NAFE. Below is the transfer function to convert a resistance value (measured by the NAFE) to a temperature value.

$$R(t) = R_0\left[1 + At + Bt^2 + C(t - 100)t^3\right]$$

All the constant (R0, A, B, C) in the above function depends on the sensor part number. Below are the values of the sensor from Honeywell (*HEL-705-T-0-12-00*):

- R_0 = 100 [Ω]
- A = 3.908 * 10^{-3} [°C^{-1}]
- B = -5.775 * 10^{-7} [°C^{-2}]
- C = -4.183 * 10^{-12} [°C^{-4}]*if t<0*
- C = 0*if t≥0*

Performing some simplifications and linearization, an equation can be obtained for the temperature that is good from 0 °C to 100 °C.

$$T(r) = \frac{r - R_0}{AR_0}$$

Where:

- R_0 = 100 [Ω]
- A = 3.908 * 10^{-3} [°C^{-1}]
- r is the resistance read on the sensor

The NAFE internal VIEX source can be used to force a known current through the RTD and the voltage drop across it can be measured using NAFE ADC channels. This measured voltage can be used to calculate the sensor resistance and rewrite the temperature conversion equation, as below:

$$T(r) = \frac{\frac{V_{ADC}}{I_{ex}} - R_0}{AR_0}$$

Where:

- R_0 = 100 [Ω]
- A = 3.908 * 10^{-3} [°C^{-1}]
- V_{ADC} is the voltage read by the NAFE ADC.
- I_{ex} is the excitation current sourced by the NAFE VIEX

The code and algorithm to implement the above application setup is discussed and shared in "*NAFE Applications with MCU Expresso*".

2.4.3 3-wire RTD

The addition of a third wire to 2-wire configuration can effectively cancel the average lead wire resistance when all the lead wires are the same length, composition, and thus the same resistance.

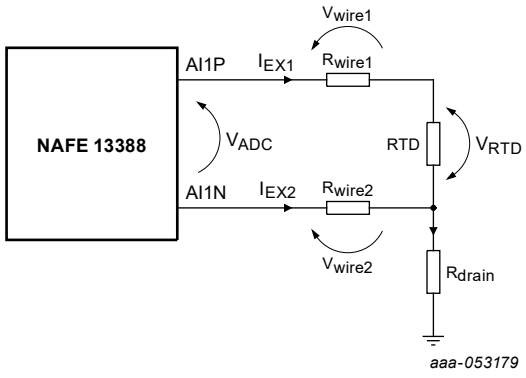


Figure 6. 3-wire RTD connection to NAFE13388

R_{wire1} and R_{wire2} are the sum of two contributions:

- PCB (printed circuit board) routing
- Sensor cable

R_{drain} is a wire resistance (third cable) useful to drain the sum of I_{ex1} and I_{ex2} through ground. If it is replaced with a precision resistor, it may be useful to accurately read the current using NAFE ADCP-ADCN channels.

$$V_{ADC} = V_{wire1} + V_{RTD} - V_{wire2}$$

if the following assumption is made:

$$R_{wire1} = R_{wire2} \quad AND \quad I_{ex1} = I_{ex2}$$

The equation for VADC become:

$$V_{ADC} = V_{RTD}$$

Pros:

- Accurate RTD measurements because of lead wire resistance cancellation
- More cost effective than a 4-wire, especially when the measurement unit and sensor are distance apart

Cons:

- Attention to solution design in terms of layout and component selection to match the resistance on each node.
- Additional matching current source – I_{ex1} and I_{ex2}.

2.4.4 NAFE configuration for 3-wire RTD

VIEX can be routed to two channels, AI1P and AI2N, for 3-wire configuration as below:

Table 12. Logic channel VIEX selection for 3-wire RTD

Logic channel	VIEX parameter	Value
0	Source	Current
	Polarity	Positive
	Magnitude	750 uA
	AIxP	AI1P
	AIxN	AI1N

Below is the NAFE register configuration for 3-wire RTD application:

- CH_CONFIG0 (Signal mapping and Gain)
- CH_CONFIG1 (Data rate and Sinc)
- CH_CONFIG2 (Channel delay)
- CH_CONFIG3 (VIEX)

Table 13. Register configuration for 3-wire RTD

Register name	Field	Field value [Hex]	Register value [Hex]
		CH0	*CH0*
CH_CONFIG0	HV_AIP[15:12]	1	11B1
	HV_AIN[11:8]	1	
	CH_GAIN[7:5]	5	
	HV_SEL[4]	1	
	LVSIG_IN[3:1]	0	
	TCC_OFF[0]	1	
CH_CONFIG1	CH_CAL_GAIN_OFFSET[15:12]	5	50B1
	CH_THRS[11:8]	0	
	ADC_DATA_RATE[7:3]	16	
	ADC_SINC[2:0]	1	
CH_CONFIG2	CH_DELAY[15:10]	B	2E80
	ADC_NORMAL_SETTLING[9]	1	
	ADC_FILTER_RESET[8]	0	
	CH_CHOP[7]	1	
CH_CONFIG3	VIEX_VI[15]	1	B009
	VIEX_POL[14]	0	
	VIEX_MAG[13:10]	C	
	VEXC_EN[9]	0	
	OPEN_DET_CURRENT[8]	0	
	VIEX_CHOP[6]	0	
	VIEX_AIP_EN[5:3]	1	
	VIEX_AIN_EN[2:0]	1	

See Section 3.4 for system-level configuration options for NAFE. The code and algorithm to implement the above application setup is discussed and shared in "*NAFE Applications with MCU Expresso*".

2.4.5 4-wire RTD

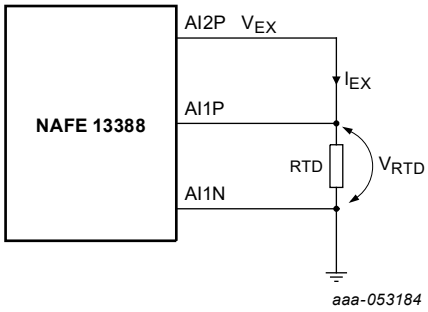


Figure 7. 4-wire RTD connection to NAFE13388

The 4-wire connection makes it possible to eliminate the cabling influence on the measurement result, as any asymmetries in the connection cable's resistance and excitation current mismatches are compensated.

This configuration requires at least three NAFE input pins as shown in Figure 7. While one pin is used to inject current into the RTD, two different pins are used to sense the voltage across the RTD. As there is no flow of current in the measurement path, the measurements are more accurate than the 2-wire and 3-wire measurements.

Pros:

- Most accurate measurement out of three RTD wire configurations
- Simpler solution

Cons:

- Requires one source channel and two measurement channels
- RTD with four cables is expensive compared to 2-wire and 3-wire solutions

2.4.6 NAFE configuration for 4-wire RTD

VIEX configuration for 4-wire RTD:

Table 14. Logic channel VIEX selection for 4-wire RTD

Logic channel	VIEX parameter	Value
0	Source	Current
	Polarity	Positive
	Magnitude	750 uA
	AIxP	AI2P
	AIxN	None

Below is the NAFE register configuration for 4-wire RTD application:

- CH_CONFIG0 (Signal mapping and Gain)
- CH_CONFIG1 (Data rate and Sinc)
- CH_CONFIG2 (Channel delay)
- CH_CONFIG3 (VIEX)

Table 15. Register configuration for 4-wire RTD

Register name	Field	Field value [Hex]	Register value [Hex]
		CH0	*CH0*
CH_CONFIG0	HV_AIP[15:12]	1	11B1
	HV_AIN[11:8]	1	
	CH_GAIN[7:5]	5	
	HV_SEL[4]	1	
	LVSIG_IN[3:1]	0	
	TCC_OFF[0]	1	
CH_CONFIG1	CH_CAL_GAIN_OFFSET[15:12]	5	50B1
	CH_THRS[11:8]	0	
	ADC_DATA_RATE[7:3]	16	
	ADC_SINC[2:0]	1	
CH_CONFIG2	CH_DELAY[15:10]	B	2E80
	ADC_NORMAL_SETTLING[9]	1	
	ADC_FILTER_RESET[8]	0	
	CH_CHOP[7]	1	
CH_CONFIG3	VIEX_VI[15]	1	B010
	VIEX_POL[14]	0	
	VIEX_MAG[13:10]	C	
	VEXC_EN[9]	0	
	OPEN_DET_CURRENT[8]	0	
	VIEX_CHOP[6]	0	
	VIEX_AIP_EN[5:3]	2	
	VIEX_AIP_EN[2:0]	0	

The code and algorithm to implement the above application setup is discussed and shared in "*NAFE Applications with MCU Expresso*".

2.4.7 4-wire RTD measurement using NAFE13388 GUI

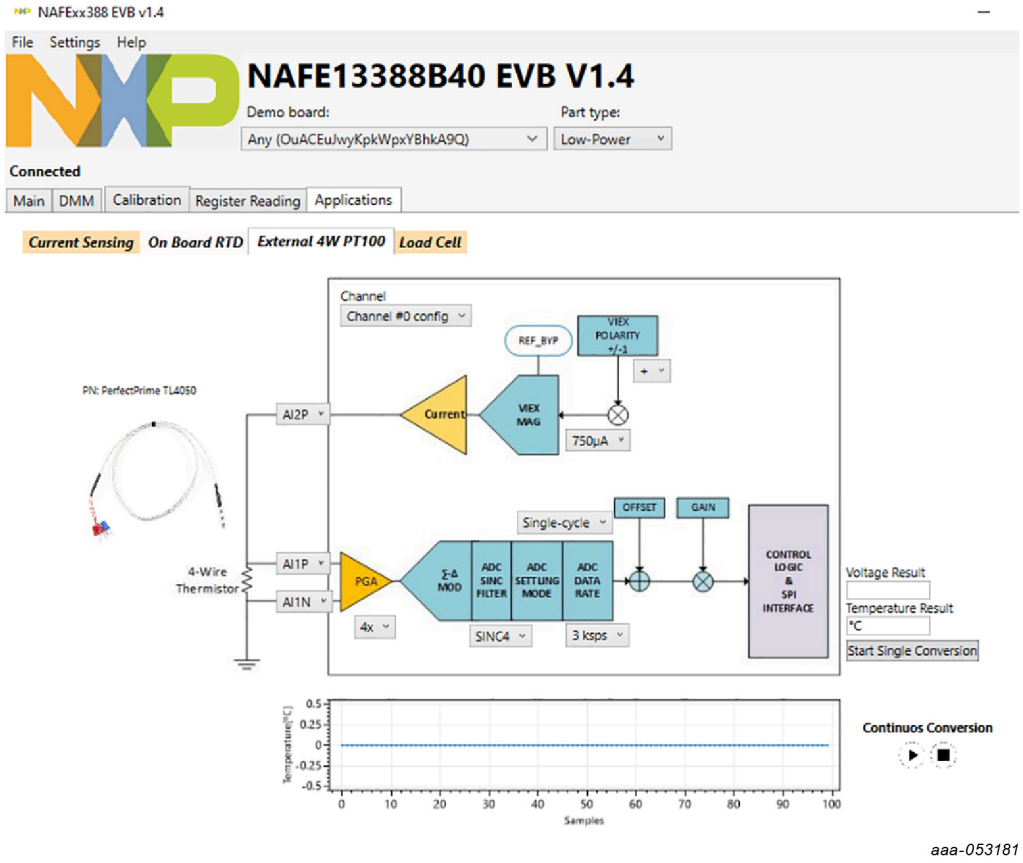


Figure 8. 4-wire RTD measurement using NAFExx388 GUI

The NAFExx388-EVB GUI (available at NAFExx388-EVB 8 Channels Universal Input AFE Evaluation Board | NXP Semiconductors) has an Applications tab that provides an easy and fast prototype for current, temperature, and load-cell sensing applications. Figure 8 from the NAFExx388 GUI shows 4-wire RTD application. The user must match the channel's selection to the physical 4-wire RTD connection on the EVB (evaluation board). The channels' configuration and sensor transfer function is built into the software to report back the temperature reading in °C. The user can do a single conversion or check the continuous conversion plot (every 100 samples) for dynamic changes in temperature, such as an RTD probe, initially at room temperature, being dipped into a cup of ice.

2.4.8 Thermocouple

A thermocouple is a thermal sensor used to transform a temperature into an electrical quantity (voltage) using the Seebeck effect. A thermocouple is formed by joining two different metals. The joining point is the temperature sensing junction (T_{TC}) while the open end (cold junction) is used to measure the differential voltage (V_{TC}) and in effect the temperature at the sensing junction.

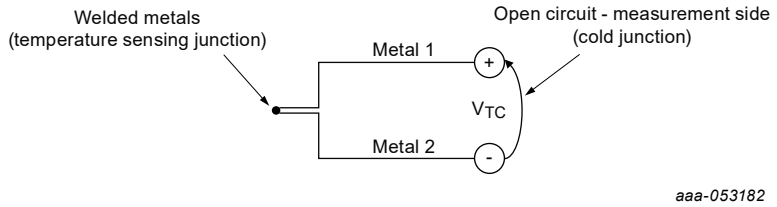


Figure 9. Thermocouple

The voltage read in the cold junction is a function of the temperature difference between the two sides. For this reason, the measurement taken with a thermocouple is not absolute value of temperature, but it is related to the temperature of the cold junction.

There are various kinds of thermocouple. They differ in the materials used as each pair of material has different behavior in terms of temperature range, linearity, and voltage/temperature coefficient.

The transfer function that allows the conversion of a voltage value to a temperature value is a complicated polynomial function. The National Institute of Standards and Technology (NIST) provides an easy-to-use lookup table to linearize the conversion function. Table 16 applies to a K-type thermocouple composed of a pair of chrome and aluminum metals.

Table 16. NIST conversion table

ITS-90 table for type K thermocouple											
°C	0	-1	-2	-3	-4	-5	-6	-7	-8	-9	-10
Thermoelectric voltage in mV											
-270	-6.458										
-260	-6.441	-6.444	-6.446	-6.448	-6.450	-6.452	-6.453	-6.455	-6.456	-6.457	-6.458
-250	-6.404	-6.408	-6.413	-6.417	-6.421	-6.425	-6.429	-6.432	-6.435	-6.438	-6.441
-240	-6.344	-6.351	-6.358	-6.364	-6.370	-6.377	-6.382	-6.388	-6.393	-6.399	-6.404
-230	-6.262	-6.271	-6.280	-6.289	-6.297	-6.306	-6.314	-6.322	-6.329	-6.337	-6.344
-220	-6.158	-6.170	-6.181	-6.192	-6.202	-6.213	-6.223	-6.233	-6.243	-6.252	-6.262
-210	-6.035	-6.048	-6.061	**-6.074**	-6.087	-6.099	-6.111	-6.123	-6.135	-6.147	-6.158
-200	-5.891	-5.907	-5.922	-5.936	-5.951	-5.965	-5.980	-5.994	-6.007	-6.021	-6.035

Table 16 shows the relationship between the voltage measured at the cold junction and the temperature at the sensing junction. The temperature at the sending junction is the linear sum of the column header with the row header of the cell matching the measured voltage given that the cold junction is at 0 °C. For example, the measured value of -6.074 mV (bold in the table) corresponds to the temperature -210 + (-3) = -213 °C.

Instead, if the cold junction is not at a controlled/known temperature, another sensor (RTD, thermistor, or diode) must be used to monitor its temperature at the cold junction. The following steps are required for accurate temperature measurement:

1. Read the cold junction temperature (T_{CJ}), through another sensor.
2. Convert T_{CJ} in V_{CJ} using the NIST table, V_{CJ} is the voltage corresponding to the temperature read.
3. Read the cold junction potential difference (V_{TC}).
4. Sum V_{TC} and V_{CJ}
5. Using the sum obtained in the previous point, obtain the corresponding temperature from the NIST table. This resultant temperature now is absolute temperature with respect to 0 °C.

2.4.8.1 Schematic example with NAFE – reference RTD on board + thermocouple sensing

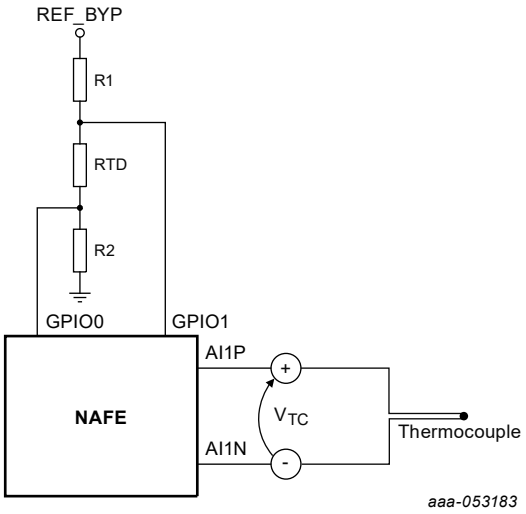


Figure 10. Thermocouple measurement using NAFE11388

In this use case below features of NAFE are utilized:

- Auxiliary differential input (GPIO0-GPIO1), to read the RTD reference temperature.
- Buffered voltage reference (REF_BYP), to excite the RTD voltage divider.
- Analog input (AI1P-AI1N), to read a V_{TC} potential difference at the ends of the cold junction.

2.4.8.2 NAFE configuration - Reference RTD on board + thermocouple sensing

This configuration must consider the following requirements:

- Two channels must be configured, one for the RTD and another one for the thermocouple.
- Multichannel conversion is needed.
- GPIO0-GPIO1 is an additional feature of the NAFE. This is a low-voltage channel without PGA.
- VTC conversion needs to be low noise, as the measurement levels are sub mV or lower.

The following tables show the logic channel assignment and configuration for the GPIO0-GPIO1 and for the thermocouple mentioned above:

Table 17. Logic channel assignment for thermocouple

Logic channel	Signal	Mapping
0	RTD	GPIO0-GPIO1
1	Thermocouple	AI1P to AI1N

Gain configuration based on the input range:

Table 18. Logic channel gain and data rate selection for thermocouple

Logic channel	Input signal (mV)	Gain (V/V)	NAFE AIN range (V)	Sinc	Data rate (Sps)	Noise (uVrms)
0	9 to 150	8X	±0.250	SINC4 + SINC4	60	0.2
1	-6.4 to 54.9	16X	±0.125	SINC4 + SINC4	60	0.14

Data rate/ADC sinc configuration based on signal bandwidth and noise (Refer to Table 28 in Section 5):

With this configuration of delay, the reading times (*T_reading* = *T_prog_delay* + *T_conv*) are:

Table 19. Logic channels reading times for thermocouple

Logic channel	Data rate	Conversion period	Delay	Read time
0	60	16.6 ms	111 us	16.711 ms
1	60	16.6 ms	111 us	16.711 ms

The requested time to complete one cycle of multichannel conversion is 34 ms.

Below is the register configuration to implement the thermocouple measurement:

- CH_CONFIG0 (Signal mapping and Gain)
- CH_CONFIG1 (Data Rate and Sinc)
- CH_CONFIG2 (Channel Delay)

Table 20. Register configuration for thermocouple measurement

Register name	Field	Field value [Hex]		Register value [Hex]	
		CH0	*CH1*	*CH0*	*CH1*
CH_CONFIG0	HV_AIP[15:12]	A	1	AAC3	11F1
	HV_AIN[11:8]	A	1		
	CH_GAIN[7:5]	6	7		
	HV_SEL[4]	0	1		
	LVSIG_IN[3:1]	1	0		
	TCC_OFF[0]	1	1		
CH_CONFIG1	CH_CAL_GAIN_OFFSET[15:12]	6	7	6094	7094
	CH_THRS[11:8]	0	0		
	ADC_DATA_RATE[7:3]	12	12		
	ADC_SINC[2:0]	4	4		
CH_CONFIG2	CH_DELAY[15:10]	1A	1A	6800	6800
	ADC_NORMAL_SETTLING[9]	0	0		
	ADC_FILTER_RESET[8]	0	0		
	CH_CHOP[7]	0	0		

2.5 Weight scale (load cell)

A load cell is a transductor used to translate mechanical force, such as weight, into measurable quantity. Load cells are usually composed of a strain gauge positioned on an elastic element. The elastic element is usually made of steel, so it is strong, but also has some elasticity. The minute variations on the spring element can be detected with strain gauges. The strain of the strain gauge is then converted by the electronics (ADC + excitation circuit) to determine the weight.

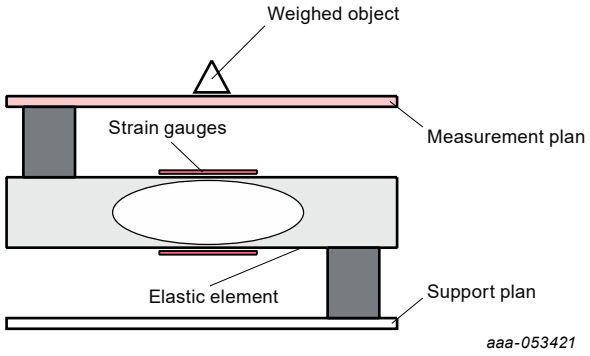


Figure 11. Load cell

2.5.1 Schematic example with NAFE – excitation + sensing

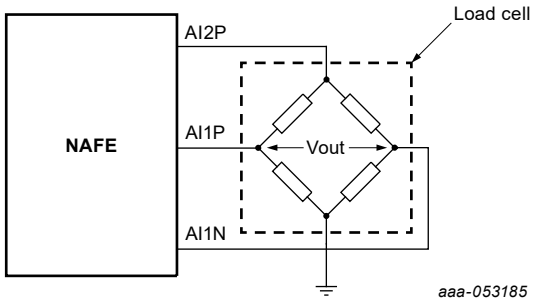


Figure 12. Load cell measurement using NAFE13388

In a load cell, a Wheatstone bridge structure is used to transform a resistance value to a voltage value. The Wheatstone architecture utilizes a strain gauge in place of resistors. AI2P of the NAFE is used as output voltage, while AI1P and AI1N are used to sense the voltage across the bridge.

2.5.2 NAFE configuration

This application needs a voltage excitation source and two input channels to sense the voltage. Use a slow data rate and a higher gain configuration to improve the quality of reading as the sense voltage range will be in the order of mV.

Configuration of other NAFE parameter mapping:

Table 21. Logic channel assignment for load cell

Logic channel	Signal	Mapping
0	Bridge Vout	AI1P to AI1N

Table 22. Logic channel data rate selection for load cell

Logic channel	Sinc	Data rate	Delay	Reading time
0	SINC4 + SINC1	100	16.5 us	10.016 ms

The reading times (*T_reading* = *T_prog_delay* + *T_conv*) are:

To summarize the VIEX configuration:

Table 23. Logic channel VIEX selection for load cell

Logic channel	VIEX parameter	Value
0	Source	Voltage
	Polarity	Positive
	Magnitude	6 V
	AIxP	AI2P
	AIxN	None

Below is the register configuration to implement the above:

- CH_CONFIG0 (Signal mapping and Gain)
- CH_CONFIG1 (Data rate and Sinc)
- CH_CONFIG2 (Channel delay)
- CH_CONFIG3 (VIEX)

Table 24. Register configuration for load cell

Register name	Field	Field value [Hex]	Register value [Hex]
		CH0	*CH0*
CH_CONFIG0	HV_AIP[15:12]	1	11F1
	HV_AIN[11:8]	1	
	CH_GAIN[7:5]	7	
	HV_SEL[4]	1	
	LVSIG_IN[3:1]	0	
	TCC_OFF[0]	1	
CH_CONFIG1	CH_CAL_GAIN_OFFSET[15:12]	7	70A4
	CH_THRS[11:8]	0	
	ADC_DATA_RATE[7:3]	14	
	ADC_SINC[2:0]	1	
CH_CONFIG2	CH_DELAY[15:10]	B	2E80
	ADC_NORMAL_SETTLING[9]	1	
	ADC_FILTER_RESET[8]	0	
	CH_CHOP[7]	1	
CH_CONFIG3	VIEX_VI[15]	0	3410
	VIEX_POL[14]	0	
	VIEX_MAG[13:10]	D	
	VEXC_EN[9]	0	
	OPEN_DET_CURRENT[8]	0	
	VIEX_CHOP[6]	0	
	VIEX_AIP_EN[5:3]	2	
	VIEX_AIN_EN[2:0]	0	

The code and algorithm to implement the above application setup is discussed and shared in "*NAFE Applications with MCU Expresso*".

Perform the following two steps to make accurate measurements:

- Offset compensation
- Conversion coefficient calculation

Offset compensation consists of taking a voltage measurement without any object on the weight scale. The measurement obtained from this conversion is the offset(O).

After the offset measurement, put an object on the weight scale with known weight(P), take a conversion and save the result(K).

Calibration coefficient is:

$$Coeff = \frac{P}{K\text{-}O}$$

Now any weight can be measured, given the voltage conversion read by the ADC (V_{ADC}):

$$Weight = Coeff * \left(V_{ADC} - O\right)$$

2.5.3 NAFE GUI example - weight scale using NAFExx388 GUI

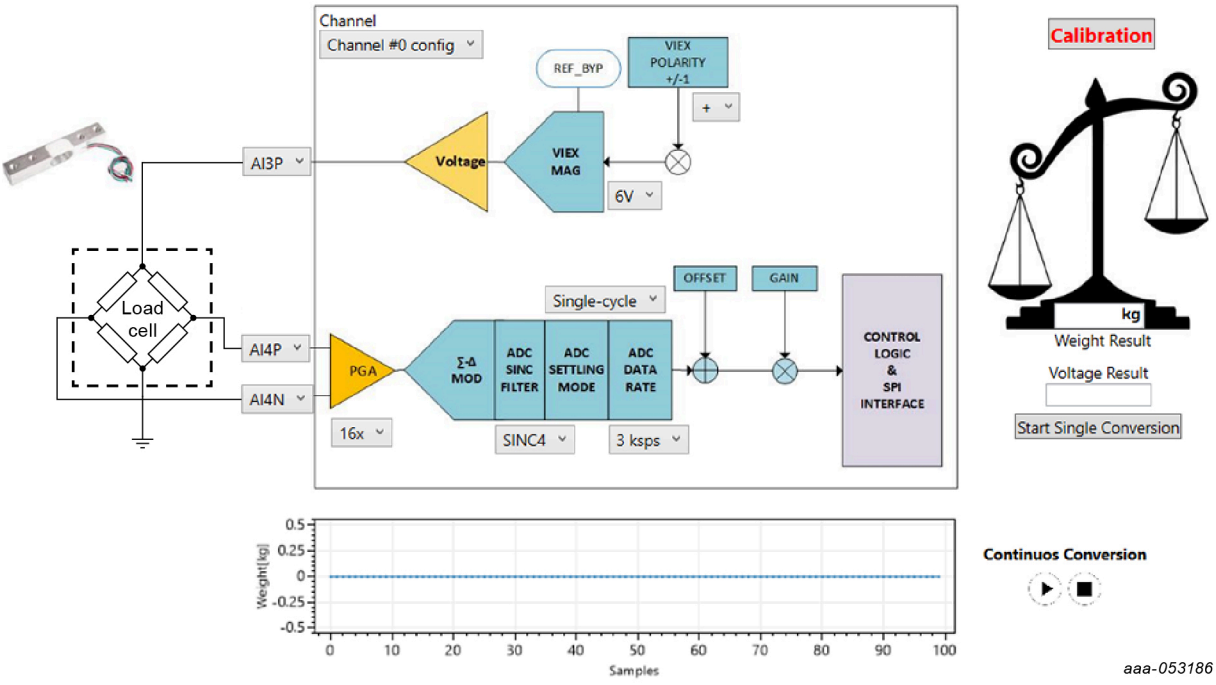


Figure 13. Weight measurement using NAFExx388 GUI

A snippet from the NXP GUI is shown in Figure 13. Select the correct channels in the GUI to match the physical load cell connection and the GUI enables the user to have a voltage and temperature conversion with automated calculation and calibration.

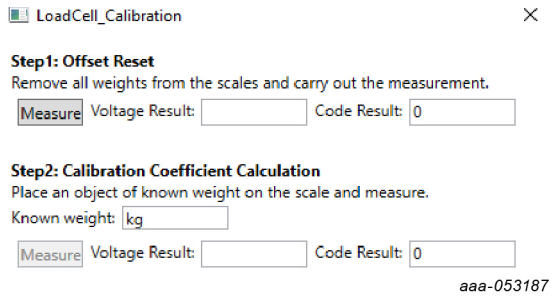


Figure 14. Load cell calibration

Click the **Calibration** button (highlighted red) to perform the two steps mentioned above to calibrate the system for measurement accuracy. Once the calibration is done, the **Calibration** button turns black to indicate that the system is calibrated. Now the user can perform a single measurement or continuous measurement.

2.6 Management of external components using NAFE GPIOs

The NAFE comes with ten GPIOs that satisfy most of the needs for monitoring and control in typical applications.

GPIOs can work as input or output, could be useful to monitor external component pins, or manage external components such as Relay, input pin, or another silicon device.

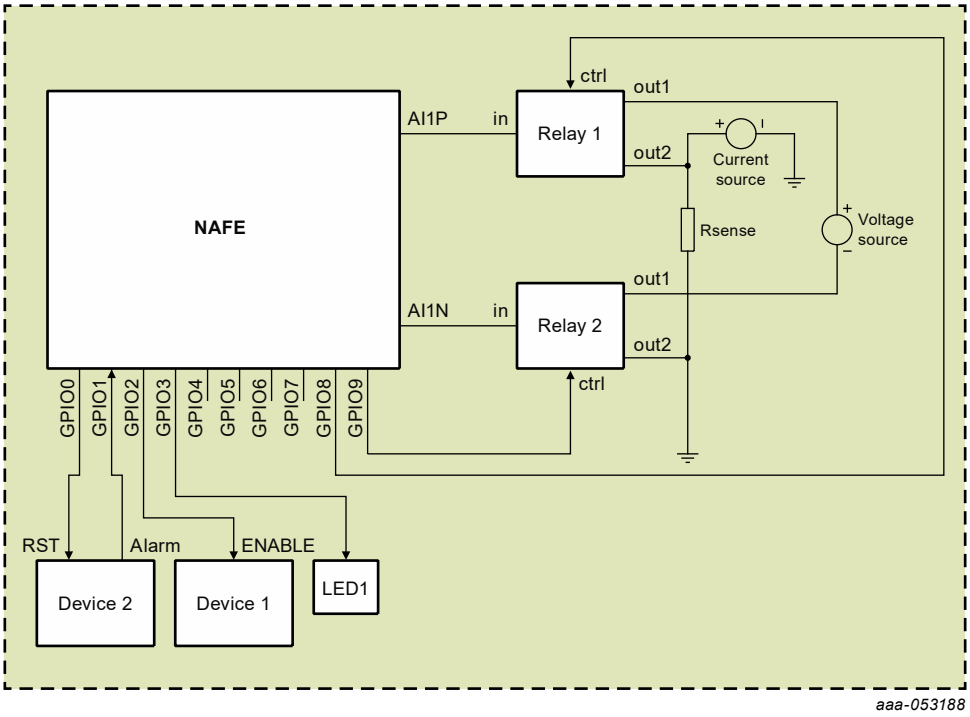


Figure 15. NAFE GPIO usage example

3 Feature clarifications

3.1 Overload vs Overrange

The NAFE can detect two different alarms, similar but different, overload and overrange:

- Overload is related to the saturation of ADC code, therefore this alarm triggers when the ADC reaches the maximum code.
- Overrange is also related to ADC code, but the trigger value is user defined through register CH_CONFIG5 and CH_CONFIG6.

OVRLOAD works only in Differential mode, because this is related to the ADC word overflow (Single-ended mode uses half the range of the ADC).

The alarms useful to the user to monitor the in-range value of the ADC are the UNDRNG and OVRRNG flags defined in the registers CH_CONFIG5 and CH_CONFIG6. If the user wants to use the entire range of the ADC, CH_CONFIG5, and CH_CONFIG6 registers should be configured as below:

- **Single-ended mode**
  - OVRNG = 0x3FFFFF
  - UNRNG = 0xBFFFFF
- **Differential mode**
  - OVRNG = 0xFFFFFF
  - UNRNG = 0x0

Nevertheless, the user has the freedom to choose other values. For example, if the user wants to stop 5 % before the total excursion, that can be done by appropriately changing the values in the registers CH_CONFIG5 and CH_CONFIG6.

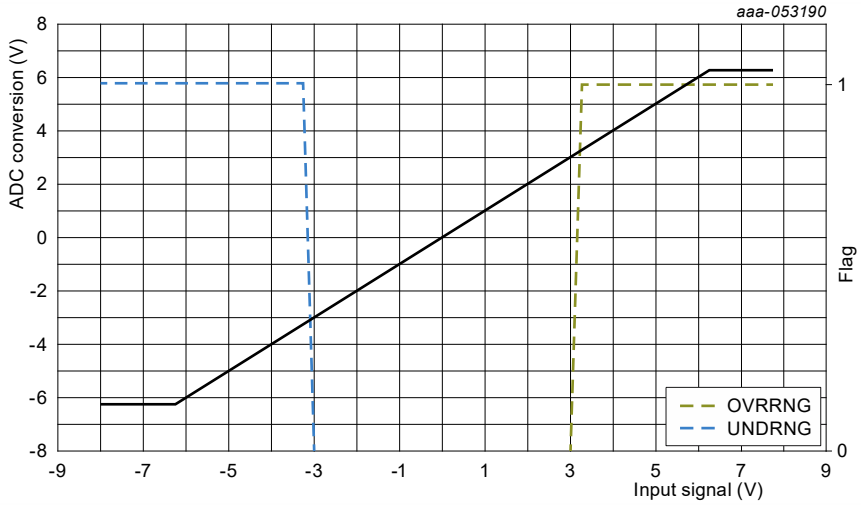


Figure 16. Under-range and over-range flag

3.2 Calibration pointers with respect to gain settings

The NAFE has the on-chip calculation based on gain/offset coefficient. This means it is possible to save the calibration coefficient inside a specific register. The NAFE uses these conversion values to adjust the output code.

These coefficients are saved in 32 different registers, 16 registers each for gain and offset. During device power up or reset, the factory calibrated coefficients stored in NVM (non-volatile memory) are loaded into the preset

registers, if available. The user may overwrite with different calibration coefficients, as needed. The gain and offset coefficients are channel-gain setting dependent.

The below pointers are pre-assigned by NXP for each PGA gain setting and the calibration is performed according to the respective gain ranges. This does not deprive customers of the possibility to use each of the 16 pairs for user calibration (system-specific custom calibration).

- Pair 0 ⇒ PGA gain = 0.2 V/V
- Pair 1⇒ PGA gain = 0.4 V/V
- Pair 2⇒ PGA gain = 0.8 V/V
- Pair 3 ⇒ PGA gain = 1 V/V
- Pair 4 ⇒ PGA gain = 2 V/V
- Pair 5 ⇒ PGA gain = 4 V/V
- Pair 6 ⇒ PGA gain = 8 V/V
- Pair 7 ⇒ PGA gain = 16 V/V

To set the channel to point at a specific pair, use the *CH_CAL_GAIN_OFFSET* field in register *CH_CONFIG1.*

3.3 Part selection tradeoffs

Assume that the system requires three signals (range < 10 V) to be measured continuously within 62.5 µs with a power target of < 200 mW. The measured signal range up to 10 V dictates the PGA gain to be 0.2 V/V. The user must honor the channel switch time (Tswitch in the NAFE13388 and NAFE73388 data sheets) for the ADC code to settle within 0.01 % of the final value. This makes the total time to measure one cycle of three channel measurements to be 3 * (Tcnv + Tch_delay) where Tcnv= 1/DataRate and Tch_delay ≥ Tswitch.

If the highest data rate of 288 Ksps (= 3.472 µs) on NAFE13388 and Tch_delay of 16.5 µs (Code = 17) are used to satisfy NAFE13388 Tswitch of 16.4 µs, the total time of 59.6 µs can meet the system requirement of 62.5 µs at a typical power consumption of 150 mW. After referring to Noise Vs Data rate table of NAFE13388, the system noise is estimated to be 27.946 mVrms.

Doing the same analysis on the NAFE73388 data rate offering shows that the six highest data rates ≥ 96 Ksps (code = 5) can meet the system requirement of 62.5 µs total conversion time. To keep the noise lowest, the system designer should pick the slowest acceptable data rate (96 Ksps with 149 uVrms noise at 0.2 V/V) as the noise increases with an increase in data rate.

Based on the above analysis, using the NAFE73388 with a data rate of 96 Ksps provides the best noise performance while meeting the system conversion time requirement at typical power consumption of 180 mW.

NAFE13388 data sheet Table 8 - Noise uVrms (24-bit)

Code	Data rate	2,304,000	Estimate noise (uVrms) vs. gain setting							
		OSR	0.2	0.4	0.8	1	2	4	8	16
0	288000	8	27946.8	13973.4	6986.7	5589.4	2794.7	1397.4	698.7	349.45
1	192000	12	7546.0	3773.0	1886.5	1509.2	754.6	377.4	188.8	94.62
2	144000	16	2984.2	1492.1	746.1	596.9	298.5	149.3	74.9	37.85
3	96000	24	818.1	409.1	204.6	163.7	82.0	41.2	21.1	11.50
4	72000	32	343.5	171.8	86.0	68.8	34.6	17.8	9.7	6.26
5	48000	48	137.2	68.7	34.5	27.7	14.2	7.8	5.1	4.09
6	36000	64	98.8	49.5	24.9	20.0	10.4	5.9	4.1	3.45

NAFE73388 data sheet Table 8 - Noise µVrms (24-bit)

Code	Data rate	4,608,000	Estimate noise (uVrms) vs PGA gain setting							
		OSR	0.2	0.4	0.8	1	2	4	8	16
0	576000	8	27947.2	13973.6	6986.8	5589.5	2794.7	1397.4	698.8	349.58
1	384000	12	7546.8	3773.4	1886.7	1509.4	754.8	377.5	189.0	94.92
2	288000	16	2985.9	1493.0	746.5	597.2	298.7	149.6	75.2	38.42
3	192000	24	822.2	411.1	205.7	164.6	82.6	41.8	21.9	12.69
4	144000	32	350.8	175.5	87.9	70.4	35.7	18.7	10.9	7.79
5	96000	48	149.0	74.6	37.6	30.2	15.8	9.1	6.4	5.58
6	72000	64	110.9	55.6	28.1	22.6	12.0	7.2	5.3	4.76

3.4 System settings

In addition to the channel settings discussed in previous sections, there are several other settings that affect the entire system.

Register (16-bit)	Bit order	Bit name	RW	Reset	Short description
SYS_CONFIG0 0x30\h	15	DRDY_PWDT	RW	0x0	DRDY pulse width duration (# of SYSCLK cycle): 0\h = 2, 1\h = 8
	14	ADC_DATA_OUT_16BIT	RW	0x0	ADC data register readout: 0\h = 24 bit, 1\h = 16 bit
	13	STATUS_STICKY			Prepended status bits behavior when bursting output data with STATUS_EN = 1. 0\h = Sticky, 1\h = Live (sampling at rising edge of DRDY).
	12	MCLK_OUT_ENABLE	RW	0x0	Enable the master clock(2*SYSCLK) output to GPIO9 pin. This bit supersedes and ignores the other GPIO9 setting.
	11:10	REF_SEL[1:0]	RW	0x0	**Select** to use Internal(REF_INT) or External(REF_EXT) 2.5 V voltage references for REF_BYP(of PGA) and REF_ADC(of ADC): **0\h** = Both REF_BYP and REF_ADC use REF_INT. **1\h** = REF_BYP uses REF_INT and REF_ADC uses REF_EXT. **2\h** = REF_BYP uses REF_EXT and REF_ADC uses REF_INT. **3\h** = REF_BYP uses REF_EXT and REF_ADC uses REF_EXT. ***Note:*** *Internal reference is always powered on.*
	9:8	CK_SRC_SEL[1:0]	RW	0x0	Select clock sources: 0\h = internal clock, 1\h = internal clock, and disable crystal oscillator circuit. 2\h = applied external 18.432 MHz clock at XI pin, and disable crystal oscillator circuit. 3\h = 18.432MHz Crystal is installed at XI, XO pins.
	7	CRC_EN	RW	0x0	Enable CRC: 0\h = disable, 1\h = enable.
	6	STATUS_EN	RW	0x0	To prepend 8-bit Live status bits to ADC data of enabled channels, MCH_EN[i] = 1. In Multichannel Read mode, the first 8 bits status bits is OR'd of the channels when in data output burst. SPI data: <status_8b><CH_DATAi>,<status_ 8b><CH_DATAj>... ***Note:*** *Live status bits(MSB to LSB): overload, underload, over-range, under-range, overtemperature, global_alarm, overvoltage, CRC error.*
	5	ADC_SYNC	RW	0x0	ADC Synchronization mode enabled for host-driven with SYNC pulse at pin. This works with all conversion modes. 0\h = disabled SYNC pin, 1\h = ADC is synchronized to SYNC pulse at rising edge and used as conversion start trigger
	4	DRDY_PIN_EDGE			To set the behavior of DRDY pin; especially in Multichannel modes, 0\h = produce rising edge on every channel conversion done, 1\h = produce rising edge only when the sequencer is done with the last enabled channel conversion.
	3	GLOBAL_ALRM_STICKY	RW	0x0	Global alarm interrupt default behavior is: 0\h = cleared when global alarm register is read, 1\h = Write 1 to clear a specific bit in the Global Alarm Interrupt register.
	2	SPI_DOUT_DRIVE	RW	0x0	Increase DOUT output drive if high capacitance loading.
	1	INTB_DRIVER_TYPE	RW	0x0	INTB pin driver type: 0 = 100 Kohm pullup with open drain, 1 = CMOS push-pull.
	0	CRC_ERROR_ON_GPIO2	RW	0x0	To enable routing of CRC_ERROR interrupt to GPIO2 pin. 0\h = normal GPIO function 1\h = Output CRC_ERROR to GPIO2 pin, active high.

3.4.1 Data ready pulse duration (DRDY_PWDT)

DRDY (rising edge) is an output pin that indicates the conversion status. DRDY is driven to high when the new conversion result is stored in the SPI buffer and is ready for reading.

It is possible to change the duration of the data ready pulse to adapt to the customer system. The default pulse duration is two cycle times of the system clock. In cases this isn't enough to capture the data, the user can change the pulse duration to eight cycle times of the system clock.

3.4.2 Data output bits depth (ADC_DATA_OUT_16BIT)

The default format of the ADC output is 24 bits. It is possible to reduce the format to 16 bits. This could be useful when 16 bits of precision is sufficient and higher speed is required.

3.4.3 Sticky global alarm or status bits (STATUS_STICKY/ GLOBAL_ALRM_STICKY)

Alarm or simple info is reported through the global alarm interrupt (GAI) register or status bits (bits appended after word data).

This flag can have two different behaviors:

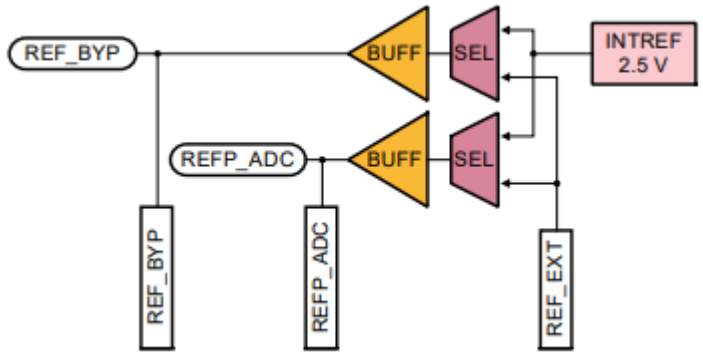
- Live flags
- Clearable flags

If sticky behavior is enabled, clearing the status of the flag requires a clear command. If the sticky behavior is disabled, the status of the flag works in Live mode.

GAI register (address 0x33\h) can be configured as non-sticky or sticky behavior by programing SYS_CONFIG0.GLOBAL_ALRM_STICKY = 0 or SYS_CONFIG0.GLOBAL_ALRM_STICKY = 1, respectively. Status bits can be made stick by programming SYS_CONFIG0.STATUS_STICKY = 1.

3.4.4 Voltage reference selector (REF_SEL)

The reference source for REF_BYP and REF_ADC could be independently selected as external or internal, by programming SYS_CONFIG0.REF_SEL[1:0].



3.4.5 Clock source selector (CK_SRC_SEL)

Clock source can be provided internally, externally directly, or generated externally through a crystal. The NAFE default is internal clock and can be configured for an appropriate external source by programming SYS_CONFIG0.CK_SRC_SEL[1:0].

3.4.6 Status byte enable (STATUS_EN)

A live status byte can be prepended to ADC data by asserting STATU_EN bit in SYS_CONFG0. This status byte indicates the out-of-bound load, range, temperature, voltage, alarm, and CRC error condition.

3.4.7 ADC signal start conversion (ADC_SYNC)

The conversion start can be triggered either by the SPI (serial peripheral interface) command at the last clock falling edge or by SYNC rising edge. SYS_CONFIG0.ADC_SYNC bit needs to be programmed to enable this ADC conversion start synchronization with the SYNC pulse applied at the SYNC pin (pin 40). The minimum width of the SYNC pulse should be 2 x T_sys_clk.

3.4.8 Data-ready behavior (DRDY_PIN_EDGE)

Data-ready pin behavior can be changed in multichannel modes to meet system design needs. In Default mode, a rising edge is produced at the end of every channel conversion, but it is possible to produce rising edge only when the sequencer is done with the last enabled channel conversion by programming SYS_CONFIG0.DRDY_PIN_EDGE = 1.

4 Revision history

Table 25. Revision history

Revision	Date	Description
v 1.1	11/30/2023	• Table 4 – Under "Field value [Hex]", changed "*CH 5* 6" to "*CH6*" – Under "Register value [Hex]", changed "CH_CONFIG2" values to "4400", "4400", "4400", "4400", "5000", "5000", and "4400" from "2C00", "2C00", "2C00", "2C00", "3800", "3800", and "2C00", respectively • Updated Figure 4, Figure 6
v.1	11/27/2023	Initial version

5 Appendix

Table 26. HV input ranges and resolutions

Nominal range values (V)								
Type	PGA gain setting							
	0.2	0.4	0.8	1	2	4	8	16
Bipolar DIFF	±20.00000	±10.00000	±5.00000	±4.00000	±2.00000	±1.00000	±0.50000	±0.25000
BipolarSE	±10.00000	±5.00000	±2.50000	±2.00000	±1.00000	±0.50000	±0.25000	±0.12500
Unipolar DIFF	±10.00000	±5.00000	±2.50000	±2.00000	±1.00000	±0.50000	±0.25000	±0.12500
Unipolar SE	±10.00000	±5.00000	±2.50000	±2.00000	±1.00000	±0.50000	±0.25000	±0.12500
Min and max values (V)								
Type	PGA gain setting							
	0.2	0.4	0.8	1	2	4	8	16
Bipolar DIFF	±25.00000	±12.50000	±6.25000	±5.00000	±2.50000	±1.25000	±0.62500	±0.31250
BipolarSE	±12.50000	±6.25000	±3.12500	±2.50000	±1.25000	±0.62500	±0.31250	±0.15625
Unipolar DIFF	±12.50000	±6.25000	±3.12500	±2.50000	±1.25000	±0.62500	±0.31250	±0.15625
Unipolar SE	±12.50000	±6.25000	±3.12500	±2.50000	±1.25000	±0.62500	±0.31250	±0.15625
Full range scale (V)								
Type	PGA gain setting							
	0.2	0.4	0.8	1	2	4	8	16
Bipolar DIFF	50	25	12.5	10	5	2.5	1.25	0.625
BipolarSE	25	12.5	6.25	5	2.5	1.25	0.625	0.3125
Unipolar DIFF	25	12.5	6.25	5	2.5	1.25	0.625	0.3125
Unipolar SE	12.5	6.25	3.125	2.5	1.25	0.625	0.3125	0.15625
Resolution (V)								
Type	PGA gain setting							
	0.2	0.4	0.8	1	2	4	8	16
Bipolar DIFF	3.0E-6	1.5E-6	745.1E-9	596.0E-9	298.0E-9	149.0E-9	74.5E-9	37.3E-9
BipolarSE	3.0E-6	1.5E-6	745.1E-9	596.0E-9	298.0E-9	149.0E-9	74.5E-9	37.3E-9
Unipolar DIFF	3.0E-6	1.5E-6	745.1E-9	596.0E-9	298.0E-9	149.0E-9	74.5E-9	37.3E-9
Unipolar SE	3.0E-6	1.5E-6	745.1E-9	596.0E-9	298.0E-9	149.0E-9	74.5E-9	37.3E-9

Table 27. Popular reading periods

System clock = 4,608,000						
ADC data rate (sps)	ADC conversion period(s)	Fixed delay (# sysclk)	Prog delay (# sysclk)	Prog delay(s)	Actual reading period(s)	Target reading period(s)
288000.00	3.472E-6	0	0	000.000E+0	3.5E-6	4.0E-6
288000.00	3.472E-6	0	2	434.028E-9	3.9E-6	4.0E-6
192000.00	5.208E-6	0	4	868.056E-9	6.1E-6	6.0E-6
192000.00	5.208E-6	0	6	1.302E-6	6.5E-6	6.7E-6
144000.00	6.944E-6	0	4	868.056E-9	7.8E-6	8.0E-6
144000.00	6.944E-6	0	14	3.038E-6	10.0E-6	10.0E-6
96000.00	10.417E-6	0	8	1.736E-6	12.2E-6	12.0E-6
96000.00	10.417E-6	0	12	2.604E-6	13.0E-6	13.3E-6
96000.00	10.417E-6	0	16	3.472E-6	13.9E-6	14.0E-6
72000.00	13.889E-6	0	10	2.170E-6	16.1E-6	16.0E-6
72000.00	13.889E-6	0	18	3.906E-6	17.8E-6	18.0E-6
72000.00	13.889E-6	0	28	6.076E-6	20.0E-6	20.0E-6

Table 27. Popular reading periods*...continued*

System clock = 4,608,000						
48000.00	20.833E-6	0	20	4.340E-6	25.2E-6	25.0E-6
48000.00	20.833E-6	0	42	9.115E-6	29.9E-6	30.0E-6
36000.00	27.778E-6	0	56	12.153E-6	39.9E-6	40.0E-6
24000.00	41.667E-6	0	38	8.247E-6	49.9E-6	50.0E-6
18000.00	55.556E-6	0	20	4.340E-6	59.9E-6	60.0E-6
18000.00	55.556E-6	0	90	19.531E-6	75.1E-6	75.0E-6
18000.00	55.556E-6	1	204	44.271E-6	99.8E-6	100.0E-6
12000.00	83.333E-6	0	76	16.493E-6	99.8E-6	100.0E-6
9000.00	111.111E-6	0	40	8.681E-6	119.8E-6	120.0E-6
9000.00	111.111E-6	0	64	13.889E-6	125.0E-6	125.0E-6
9000.00	111.111E-6	0	178	38.628E-6	149.7E-6	150.0E-6
9000.00	111.111E-6	0	224	48.611E-6	159.7E-6	160.0E-6
6000.00	166.667E-6	0	154	33.420E-6	200.1E-6	200.0E-6
4500.00	222.222E-6	0	128	27.778E-6	250.0E-6	250.0E-6
4500.00	222.222E-6	0	358	77.691E-6	299.9E-6	300.0E-6
2250.00	444.444E-6	0	256	55.556E-6	500.0E-6	500.0E-6
2250.00	444.444E-6	0	716	155.382E-6	599.8E-6	600.0E-6
1125.00	888.889E-6	0	512	111.111E-6	1.0E-3	1.0E-3
1125.00	888.889E-6	0	1,664	361.111E-6	1.3E-3	1.3E-3
1125.00	888.889E-6	0	3,276	710.938E-6	1.6E-3	1.6E-3
562.50	1.778E-3	0	1,024	222.222E-6	2.0E-3	2.0E-3
400.00	2.500E-3	0	0	000.000E+0	2.5E-3	2.5E-3
200.00	5.000E-3	0	0	000.000E+0	5.0E-3	5.0E-3
100.00	10.000E-3	0	0	000.000E+0	10.0E-3	10.0E-3
60.00	16.667E-3	0	0	000.000E+0	16.7E-3	16.7E-3
50.00	20.000E-3	0	0	000.000E+0	20.0E-3	20.0E-3
30.00	33.333E-3	0	0	000.000E+0	33.3E-3	33.3E-3
30.00	33.333E-3	0	19,200	4.167E-3	37.5E-3	37.5E-3
25.00	40.000E-3	0	0	000.000E+0	40.0E-3	40.0E-3
25.00	40.000E-3	0	23,040	5.000E-3	45.0E-3	45.0E-3
20.00	50.000E-3	0	0	000.000E+0	50.0E-3	50.0E-3
15.00	66.667E-3	0	0	000.000E+0	66.7E-3	66.6E-3
10.00	100.000E-3	0	0	000.000E+0	100.0E-3	100.0E-3
7.50	133.333E-3	0	0	000.000E+0	133.3E-3	133.3E-3
7.50	133.333E-3	0	7,680	1.667E-3	135.0E-3	135.0E-3
7.50	133.333E-3	0	8,191	1.778E-3	135.1E-3	360.0E-3

Table 28. Noise µVrms (24-bit)

Code	Data rate	2,304,000	Estimate noise (uVrms) vs. gain setting							
		OSR	0.2	0.4	0.8	1	2	4	8	16
0	288000	8	27946.8	13973.4	6986.7	5589.4	2794.7	1397.4	698.7	349.45
1	192000	12	7546.0	3773.0	1886.5	1509.2	754.6	377.4	188.8	94.62
2	144000	16	2984.2	1492.1	746.1	596.9	298.5	149.3	74.9	37.85
3	96000	24	818.1	409.1	204.6	163.7	82.0	41.2	21.1	11.50
4	72000	32	343.5	171.8	86.0	68.8	34.6	17.8	9.7	6.26
5	48000	48	137.2	68.7	34.5	27.7	14.2	7.8	5.1	4.09
6	36000	64	98.8	49.5	24.9	20.0	10.4	5.9	4.1	3.45
7	24000	96	76.3	38.2	19.2	15.5	8.1	4.6	3.2	2.80
8	18000	128	65.7	32.9	16.6	13.3	7.0	4.0	2.8	2.42
9	12000	192	53.6	26.8	13.5	10.9	5.7	3.3	2.3	1.98
10	9000	256	46.4	23.2	11.7	9.4	4.9	2.8	2.0	1.71
11	6000	384	37.9	19.0	9.6	7.7	4.0	2.3	1.6	1.40
12	4500	512	32.8	16.4	8.3	6.7	3.5	2.0	1.4	1.21
13	3000	768	26.8	13.4	6.8	5.4	2.8	1.6	1.1	0.99
14	2250	1024	23.2	11.6	5.9	4.7	2.5	1.4	1.0	0.86
15	1125	2048	16.4	8.2	4.1	3.3	1.7	1.0	0.7	0.61
16	562.5	4096	11.6	5.8	2.9	2.4	1.2	0.7	0.5	0.43
17	400	5760	9.8	4.9	2.5	2.0	1.0	0.6	0.4	0.36
18	300	7680	8.5	4.3	2.2	1.7	0.9	0.5	0.4	0.31
19	200	11520	7.0	3.5	1.8	1.4	0.7	0.4	0.3	0.26
20	100	23040	5.0	2.5	1.3	1.0	0.5	0.3	0.2	0.18
21	60	38400	3.9	2.0	1.0	0.8	0.4	0.2	0.2	0.14
22	50	46080	3.6	1.8	0.9	0.7	0.4	0.2	0.2	0.13
23	30	76800	2.9	1.4	0.7	0.6	0.3	0.2	0.1	0.10
24	25	92160	2.7	1.3	0.7	0.5	0.3	0.2	0.1	0.09
25	20	115200	2.4	1.2	0.6	0.5	0.3	0.1	0.1	0.08
26	15	153600	2.2	1.1	0.5	0.4	0.2	0.1	0.1	0.07
27	10	230400	1.9	0.9	0.5	0.4	0.2	0.1	0.1	0.06
28	7.5	307200	1.7	0.9	0.4	0.3	0.2	0.1	0.1	0.05

6 Reference

[1] NAFE13388, *"NAFE11388 Universal ±25 V 8-Input Low Power AFE"*, data sheet

[2] NAFE73388, *"Universal ±25 V 8-Input High-Speed AFE with Excitation Sources"*, data sheet

[3] The Engineering Toolbox

[4] Instrumentation Tool

[5] NIST Table k type

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Date of release: 30 November 2023
Document identifier: AN14102