AN13732

PCA9482UK 6 A 2:1, 1:2, and 1:1 mode switched capacitor direct charger

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Document information

Information	Content
Keywords	6 A 2:1/1:2/1:1 mode switched capacitor; PCA9482UK
Abstract	Many mobile phones have adopted features requiring high system performance, such as 5G, multiple cameras, and high resolution LCDs with multi-processors, increasing the demand for higher battery capacity. These power-hungry features have created the need for users to charge their mobile phone batteries frequently and quickly. Legacy inductor-based chargers are still widely used in mobile applications, but the high heat from induction charging limits higher charging power for the battery. These chargers are unable to satisfy users who require fast charging. Switched-capacitor (SC) direct charging has been recognized as a good replacement for inductor-based charging, because of its higher efficiency and lower heat dissipation.

Revision history

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Rev	Date	Description
1.2	20230803	Section 3.4: Added comment on min/max AVDD voltage
1.1	20230227	Section 3.2: Added "nINT pin can be floating or open if not used."
1	20220927	Initial release.

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1 Introduction

Many mobile phones have adopted features requiring high system performance, such as 5G, multiple cameras, and high resolution LCDs with multi-processors, increasing the demand for higher battery capacity. These power-hungry features have created the need for users to charge their mobile phone batteries frequently and quickly.

Legacy inductor-based chargers are still widely used in mobile applications, but the high heat from induction charging limits higher charging power for the battery. These chargers are unable to satisfy users who require fast charging.

Switched-capacitor (SC) direct charging has been recognized as a good replacement for inductor-based charging, because of its higher efficiency and lower heat dissipation. Fast direct chargers have become mandatory in many mobile phones, including low-tier models.

PCA9482UK achieves best-in-class SC direct charging in terms of efficiency, with lower BOMs.

This application note provides details for possible customer applications, including external components.

2 PCA9482UK Charging application

2.1 30 W charging application

The input current at VBUS can reach 3 A, which is half of the maximum output current. A single PCA9482UK can support 30 W charging without an additional SC converter.

An example of the charging block is shown in Figure 1.

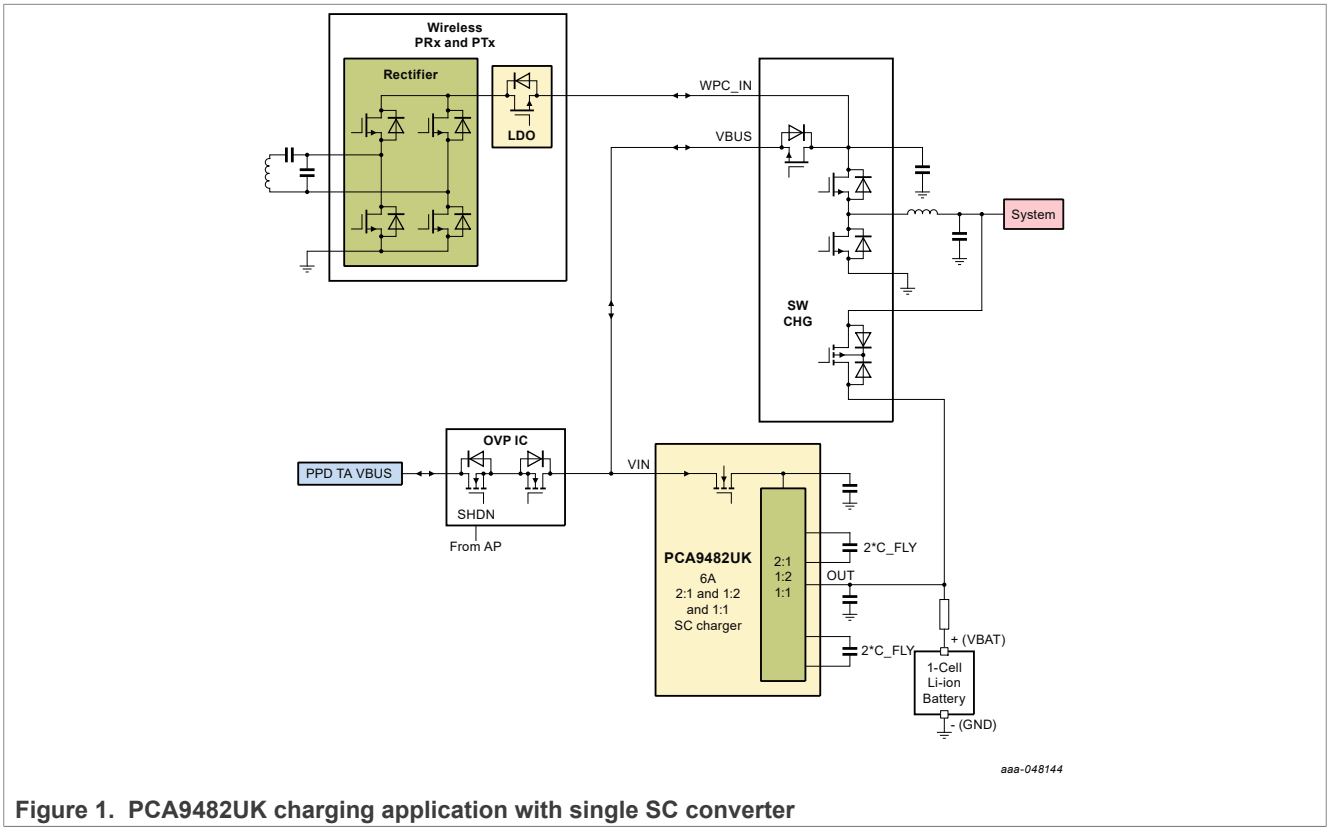

Figure 1. PCA9482UK charging application with single SC converter

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2.2 Guidance for monitoring status and interrupt for IVIN and IBAT regulation

PCA9482UK has input and charging current (IVIN and IBAT) regulation features. Both regulation features are used to limit input and battery charging current, in order to not exceed allowable input and charging current that are programmed at each register.

Input current is monitored at current sense circuit at OVPFET, and charging current is sensed at an external series sense resistor located at one of battery terminals. Sensed current is converted to voltage for gate control of OVPFET, and input current and charging current are regulated to the programmed limits when they exceed programmed current.

Corresponding status and interrupt bits indicate when current regulation happens. There is a fixed offset between real regulation and the threshold of the status and interrupt settings, so that real regulation happens after an interrupt is triggered and its status bit changes. The status bit, though, is repeatedly toggled around the threshold of status for input and charging current regulation, due to current ripple through OVPFET and the external sense resistor.

In an application, the system recognizes any set of interrupt and corresponding status for current regulation, and adjusts input current and voltage to exit the regulation condition. If the moment when the current regulation status bit is toggling should be ignored, though, then a repetition of reading the status register value three to five times is required. This would detect when the status bit stops toggling and settles on a particular status.

2.3 Guidance for IVIN ADC in reverse 1:1 and 1:2 mode

PCA9482UK supports an input current monitoring feature in forward 2:1 and 1:1 switching operations, using an ADC function.

When an IVIN ADC function in reverse 1:1 and 1:2 mode is needed for certain applications, PCA9482UK can also support that, using the folllowing register settings and calculations.

1. Register settings
   a. Set ADC_EN bit in address 0x2Ah to 1b to enable ADC function.
   b. Set ADC_READ_VIN_CURRENT_EN bit in address 0x2Bh to 1b to enable IVIN ADC feature.
   c. Read address 0x3Bh and 0x3Ch sequentially. ADC read should be low-byte (bit 7:0) first and then high byte (bit 11:8).
2. Calculation to convert from ADC readout to IVIN current (A):

IVIN Current (A) in reverse 1:2 and 1:1 mode = DEC[11 :0] x 0.00212

Note: *[7:0] bits in address 0x3B are [7:0] of the 12 bit ADC read value and [3:0] bits in address 0x3C are [11:8] of the 12 bit ADC read value.*

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3 PCA9482UK reference schematic

3.1 Reference schematic with OVP IC

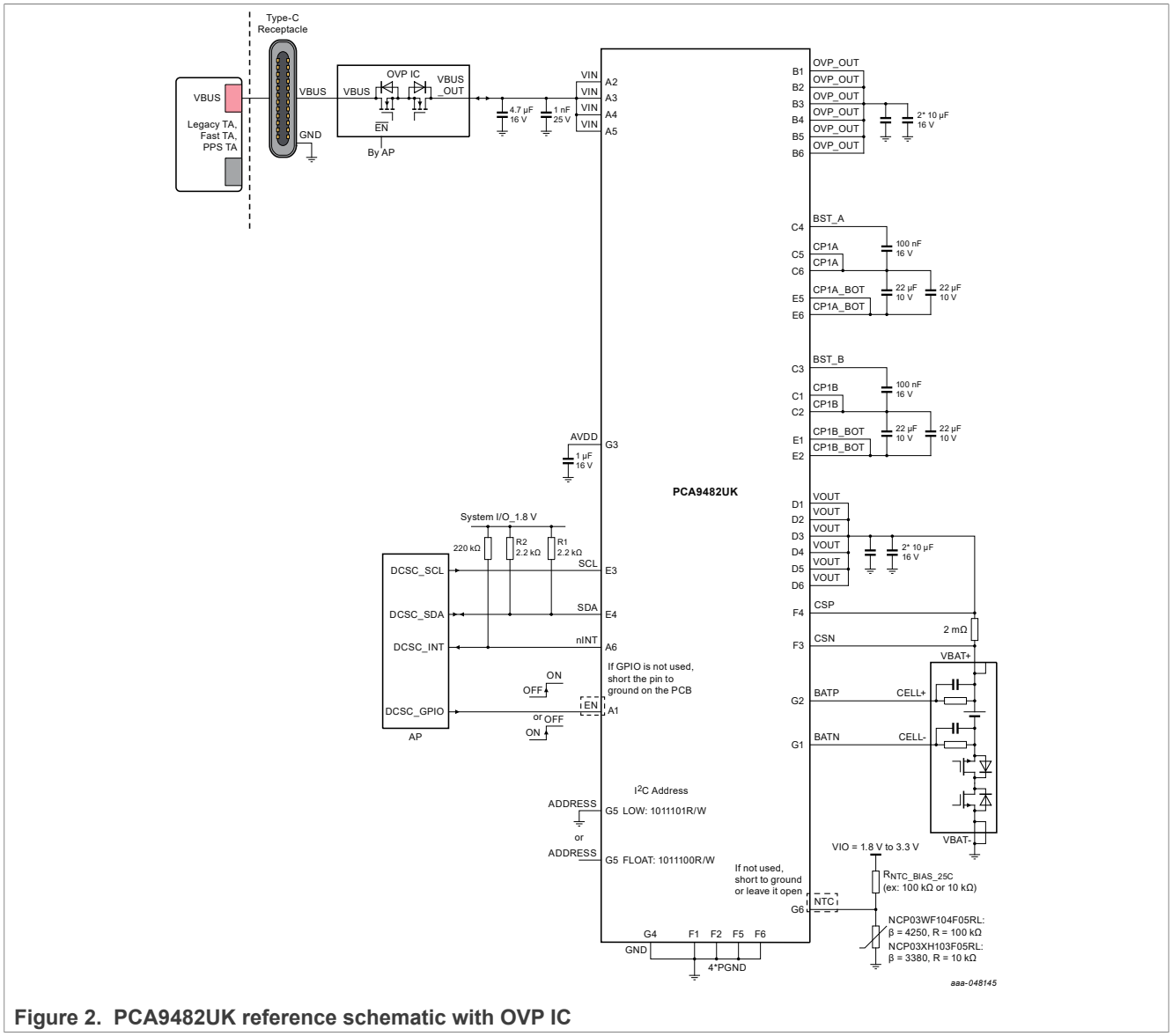

Figure 2. PCA9482UK reference schematic with OVP IC

3.2 I²C and other digital pins

PCA9482UK provides two options for the I²C address, determined by the ADDRESS pin setting, as shown in Table 1.

Table 1. I²C addresses

ADDRESS	Address (write) in hex	Address (read) In hex
LOW	BA	BB
FLOAT	B8	B9

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The I^2C interface supports clock speeds up to 1 MHz. SDA and SCL should have a 2.2 kΩ pullup resistor.

The EN pin is the digital pin used to enable the device. The polarity of the EN pin can be selected using EN_CFG in register 0x18.

nINT is the open drain output, requiring a 220 kΩ pullup resistor. It goes low when any unmasked interrupt bit is asserted.

nINT pin can be floating or open if not used.

3.3 NTC

The NTC input with AVDD pull-up voltage is connected to an external negative temperature coefficient (NTC) thermistor to monitor system temperature, or to NTC on the battery package to monitor battery temperature. To utilize the NTC function, set NTC_EN bit to 1b. There are two registers that can be used to set a different temperature threshold, such as hot/warm and cold/cool. If one of two programmed thresholds is monitored, the device issues a corresponding interrupt signal.

3.4 AVDD

AVDD is the internal LDO output, requiring a 1 µF/6.3 V bypass capacitor. Typical AVDD is 1.536 V. Minimum and maximum AVDD are 1.53 V and 1.54 V, respectively.

3.5 Input capacitor selection

In switched capacitor converter application, large AC currents flow through the input/output capacitors. The input capacitor helps to keep the input voltage stable during a switching operation.

Low equivalent series resistance (ESR) ceramic capacitors are highly recommended for this application. Larger size X7R MLCC capacitors are normally recommended. Capacitance derating needs to be considered at a DC bias voltage.

3.6 Flying capacitor selection

Large AC currents flow through the flying capacitors. Low ESR ceramic capacitors are highly recommended for this application. The flying capacitor must be selected to accommodate the maximum load current. Larger size X7R MLCC capacitors are normally recommended. Capacitance derating needs to be considered at a DC bias voltage.

In general, a recommended voltage ripple at CFLY is about 2% of output voltage. If the maximum output voltage is 5V, the ripple at CFLY is 100 mV. The value of CFLY can be obtained from the formula below in dual phase.

$$C_{FLY}\ (\mu F) = \frac{I_{OUT}\ (max)}{2 \times frequency \times \Delta V_{CFLY}\ (Voltage\ ripple)}$$

Where:

I_{OUT} (max): A maximum output current

ΔV_{CFLY}: voltage ripple on fly cap

Frequency: SC’s operating frequency

2 x 22 µF is fully verified in application, and can support 30 W charging in a smartphone form factor without additional thermal dissipation measures..

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3.7 Output capacitor selection

Large AC current flows through the flying capacitors and input/output capacitors. The average output current is given by the formula below.

I_{OUT} = 2 x Frequency x C_{FLY} x ΔV_{CFLY}

The total output voltage ripple is:

$$\Delta V_{OUT} = \frac{I_{OUT}}{2 \times frequency \times \left(C_{FLY} + C_{SC\_OUT}\right)}$$

A voltage ripple at C_{VOUT} should be determined using system requirements.

3.8 Bill of material (BOM)

Table 2 shows all the components for the device.

Table 2. Bill of material

Name	Value	Size	Part Name / Maker	Note
C_{VIN}	4.7 µF/16 V	1608	Murata, GRM188C71C475ME21	C_{EFF}=1.4 µF at 10 V
	1 nF/25 V	0603	Murata, GRM033R61E102KA01	Optional for high frequency filter
C_{OVP_OUT}	10 µF/16 V	1608	Murata, GRM188R61C106KAAL	Two capacitors. C_{EFF}=1.7 µF for one capacitor at 10 V
C_{FLY}	22 µF/16 V	1608	SEMCO, CL10A226MO7JZNC	Two capacitors. C_{EFF}=6.9 µF at 5 V
C_{BST}	100 nF/16 V	0603	Murata, GRM033R61C104KE14	
C_{VOUT}	22 µF/10 V	1608	SEMCO, CL10A226MP8NUNE	Two capacitors. C_{EFF}=5 µF at 4.5 V
C_{AVDD}	1 uF/6.3 V	0603	Murata, GRM033D70J105ME01	C_{EFF}=0.88 µF at 1.5 V
R_{SENSE}	1/2/5 mΩ			for battery current
R_{I2C}	2.2 kΩ	0603		SCL and SDA
R_{nINT}	220 kΩ	0603		
NTC	β=4250 or β=3380	0603	NCP03WF104F05RL or NCP03XH103F05RL	Place it if needed

4 Layout Guides

4.1 PCB layout guidelines

The device has a dual phase converter with two flying capacitors on each phase. Here is a PCB layout priority list for proper layout.

It is essential that PCB layout is performed in this order.

1. Utilize 8-layer board for optimal layout, and assign one layer as solid ground plane near the device to minimize high-current path.

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2. Place flying capacitors as close to CP1A, CP1B, CP1A_BOT and CP1B_BOT bumps as possible. The trace shall be wide enough to carry the charging and discharging current and short to minimize trace resistance which affects efficiency directly.
3. Place output capacitor as close as possible to VOUT bumps. Use as wide as possible on the 2nd layer to short VOUT from each phase.
4. Place input capacitors as close as possible to VIN and input power trace should be routed to center of VIN pins.
5. Place two OVP_OUT capacitors close to edge of bumps symmetrically.
6. Decoupling capacitors shall be placed next to the device and make trace connection as short as possible.
7. Ensure that there are sufficient thermal vias directly under bumps of the power FETs, power ground, connecting to copper on other layers.

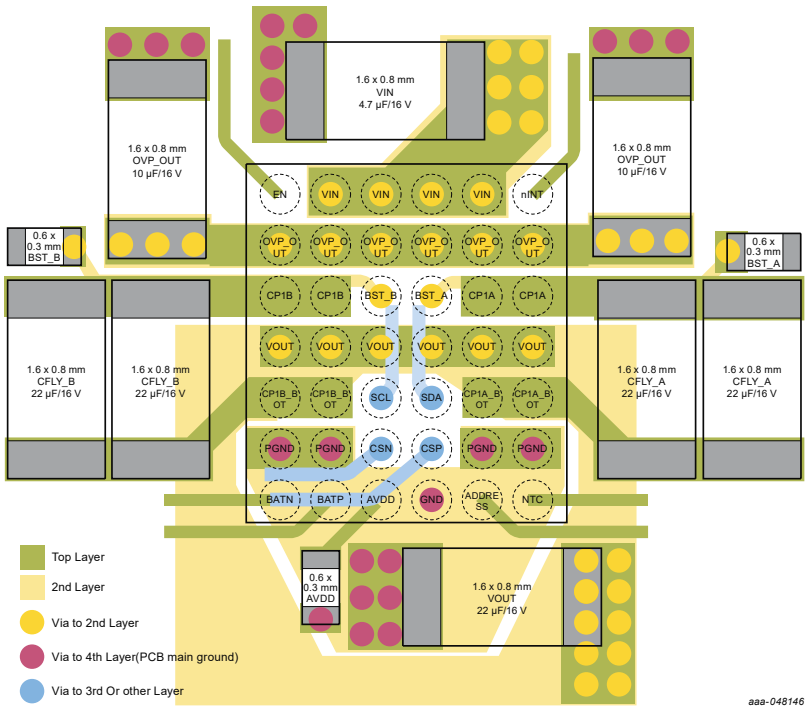

Figure 3. PCA9482UK recommended PCB layout

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