AN13609

NX30P6093A application note

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Document information

Information	Content
Keywords	NX30P6093A, high voltage I^2C controlled overvoltage protection load switch with OTG
Abstract	The NX30P6093A is a 5.6A I^2C controlled overvoltage protection load switch for USB Type-C and PD application. It includes undervoltage lockout, overvoltage lockout and overtemperature protection circuits

Revision history

Rev	Date	Description
v.1.0	20220406	Initial version

1 Scope and setup of the application note

1.1 Scope

This application note discusses the NX30P6093A functions for applications in general and the notes when using this device.

1.2 General setup of the application notes

The setup of this document is made in such a way, that a chapter or paragraph on a selected subject can be read as a stand-alone explanation with a minimum on cross-references to other document parts or the datasheet. This leads to some repetition of information within the application note and to descriptions or figures that are like the ones published in the NX30P6093A datasheet. In most cases typical values are given to enhance the readability.

Chapter 2: Introduction and features

Chapter 3: IC pin overview with a summary of the functions and typical levels

Chapter 4: Application diagram

Chapter 5: System description

Chapter 6: Debugging (or starting parts of) an application circuit Chapter 7: optional circuits and application tricks

Chapter 8: PCB design and layout guidelines

1.3 Related documents and tools

More documents and design tools can be found at the product page of NX30P6093A or are available through the local sales office.

2 Introduction

2.1 Introduction

The NX30P6093A is a 5.6A I^2C controlled overvoltage protection Load switch for USB Type-C and PD applications. It includes undervoltage lockout, overvoltage lockout and overtemperature protection circuits, designed to automatically isolate the power switch terminals when a fault condition occurs. It features input pin impedance detection function, providing USB power supply pin status to system to avoid short circuit damage for the Type-C port power supply pin.

2.2 Features

NX30P6093A has a default overvoltage protection threshold, and the OVLO threshold can be adjusted by both external resistor divider on ADJ pin and internal I^2C register. A 13ms debounce time is deployed every time before the device is switched ON, followed by a soft start to limit the inrush current.

USB OTG is supported when the plugged accessory is recognized as an OTG device by system and a 5V source is applied on VOUT pin of NX30P6093A. The current capability in USB OTG mode is limited to max 1.5A.

Designed for operation from 2.8V to 20.0V, it can be used in USB Type-C and PD power control applications to offer essential protection and enhance system reliability.

NX30P6093A is offered in a small 20-bump 1.7 x 2.16 mm, 0.4mm pitch WLCSP package.

2.2.1 Key features

- Wide supply voltage range for VIN from 2.8V to 20.0V
- System Power supply VDD from 3.0V to 4.5V
- I_{SW} maximum 5.6A continuous current for OVP mode
- Support 1.5A USB OTG
- 29V tolerance on VIN pin
- 16mΩ (typical) ultra-low ON resistance
- Adjustable VIN overvoltage protection by both external resistor and I^2C
- Built-in slew rate control for inrush current limit
- Integrated current source for VIN pin impedance detection
- Protection circuitry
  - Overtemperature protection
  - Overvoltage protection
  - Undervoltage lockout
- Surge protection:
  - IEC61000-4-5 exceeds ±100V on VIN
- ESD protection
  - IEC61000-4-2 contact discharge exceeds 8kV on VIN
  - IEC61000-4-2 air discharge exceeds 15kV on VIN
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 3kV on all pins
  - MM Class B exceeds 100 V on all the pins
- Specified from -40 °C to +85 °C

3 Pin description

Table 1. Pin description

Symbol	Pin	Type	Description
VIN	B3, B4, B5 C3, C4, C5	Power I/O	Power Input pins, these pins should be connected together on PCB
VOUT	A3, A4, A5 D3, D4, D5	Power I/O	Power Input pins, these pins should be connected together on PCB
GND	B2, C2	Ground	Ground pin, these pins should be connected to system ground with good connection for surge protection discharge current
$\overline{EN}$	A1	Input	Enable pin, active low. When it is tied to high, the device enters low power standby mode and VOUT is disconnected from VIN. Internal pull down resistor integrated
INT	B1	Output	I^2C-bus interface interrupt to be connected to the I^2C-bus master of the host processor
VDD	C1	Power	System Power supply for chip
SDA	D2	I/O	I^2C-bus interface serial data to be connected to the I^2C-bus master of the host processor
SCL	D1	Input	I^2C-bus interface serial clock to be connected to the I^2C-bus master of the host processor
ADJ	A2	Input	External OVLO adjust pin. Connect to OVLO resistor divider when select OVLO level by this pin. Connect to ground when it is not used, in this case OVLO determined internally

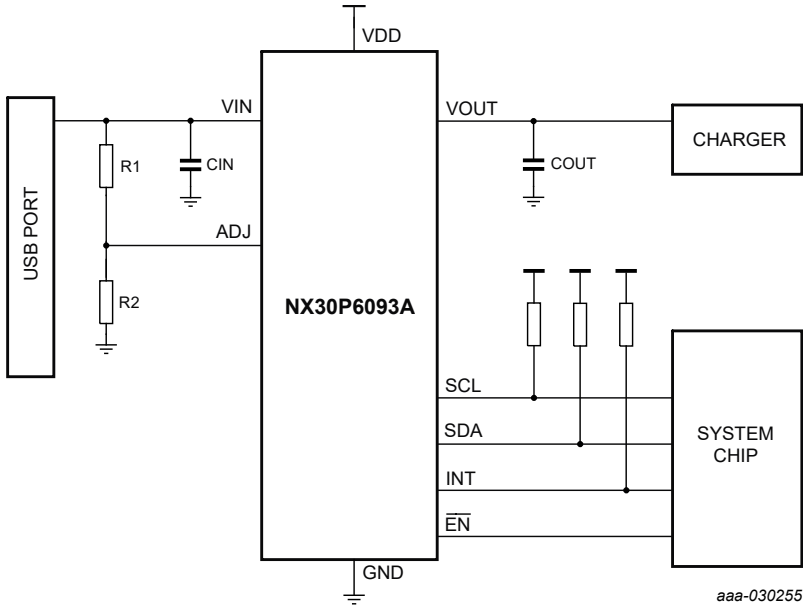
4 Application diagram

The NX30P6093 is typically used on a USB port charging path in a portable, battery operated device. The I^2C signals require an external pull-up resistor which should be connected to a supply voltage matching the logic input pin supply level that it is connected to.

When the default internal OVLO threshold is used, the ADJ pin shall be shorted to GND. While OVLO threshold is adjusted by ADJ pin, a resister divider shall be connected.

In order to have better VIN pin impedance detection range, it is recommended that the total resistance of R1 and R2 are larger than 1MΩ.

For the best performance, it is recommended to keep input and output trace short and capacitors as close to the device as possible. Regarding the thermal performance, it is recommended to increase the PCB area around VIN and VOUT pins.



R1 and R2 are only needed for adjustable V_{OVLO}; To use default V_{OVLO} threshold, connect OVLO to GND

The recommended resistor value R1+R2 > 1MΩ

C_{IN} and C_{OUT} minimum are recommended to be 1µF

Figure 1. NX30P6093A application diagram

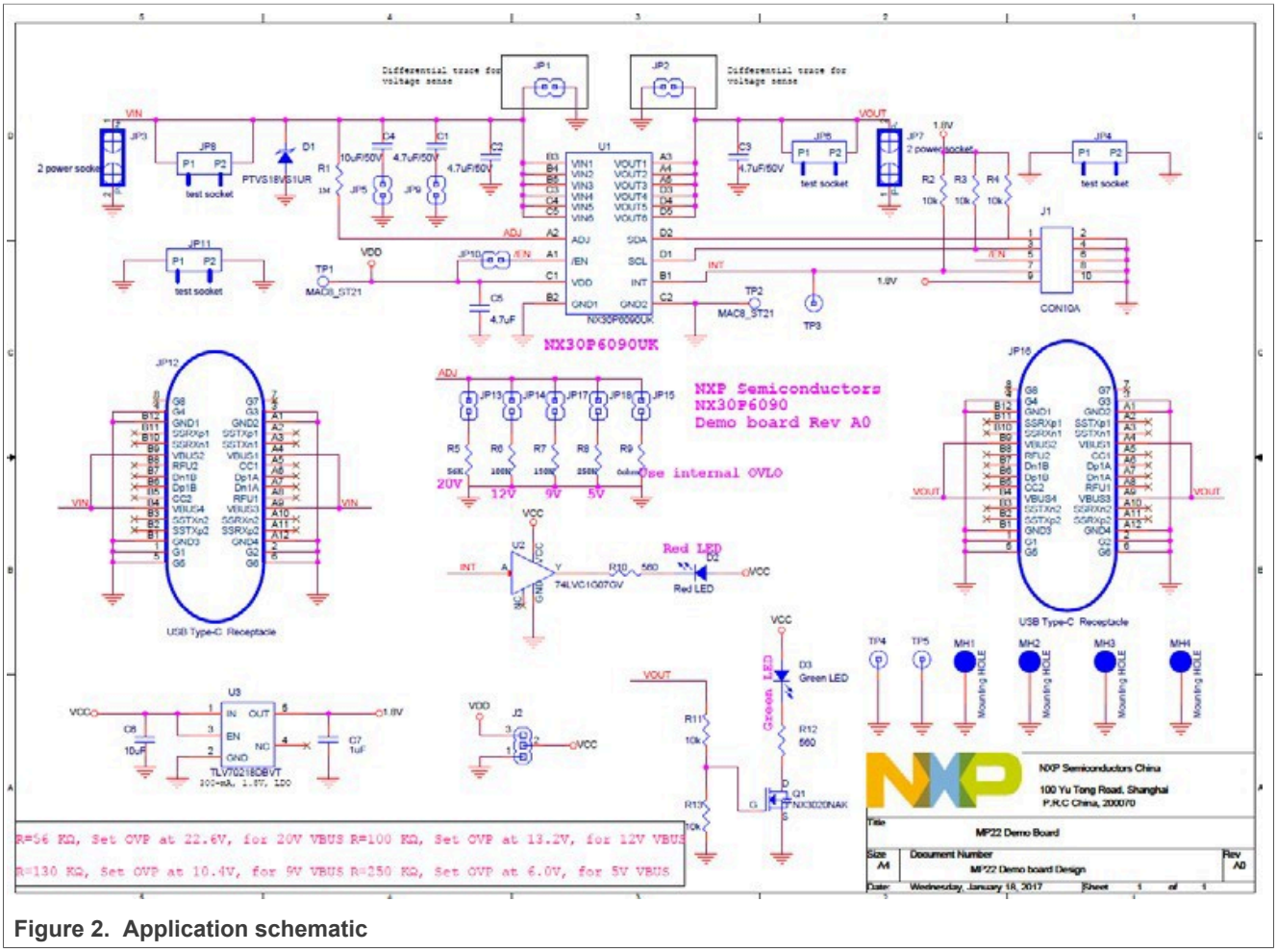


Figure 2. Application schematic

5 System description

NX30P6093A is an integrated device with three major functions: programmable overvoltage protection, VIN pin impedance detection and USB OTG. It protects USB Type-C power supply pin and internal system by isolating high voltage when it is exceeds OVLO threshold. The VIN pin impedance detection provides a status monitoring for system to avoid damage by short circuit of USB Type-C power supply pin.

The impedance detection feature is activated when VIN <V_{UVLO}, in this case NX30P6093A supplied by system power VDD. When VIN>V_{UVLO}, this feature is disabled automatically.

USB OTG is supported when the plugged accessory is recognized as an OTG device by system and a 5V source is applied on VOUT pin of NX30P6093A.

5.1 $\overline{EN}$ input

A HIGH on $\overline{EN}$ disables the channel MOSFET, all protection circuits, and VIN impedance detection circuits, putting the device into a low power mode. A LOW on $\overline{EN}$ enables the protection circuits and the MOSFET. There is an internal 1 MΩ pull-down resistor on

the $\overline{EN}$ pin to ensure the power switch conducting in a dead-battery situation. A 13ms debounce time has been deployed before device turning on.

5.2 OTG mode

USB OTG is supported when the plugged accessory is recognized as an OTG device by system and a 5V source is applied on VOUT pin of NX30P6093A. The $\overline{EN}$ pin and VOUT_EN bit in register 0x01 must to be set LOW to support USB OTG mode. If $\overline{EN}$ pin or VOUT_EN bit is HIGH, the current is conducted by body diode that will induce much higher power dissipation due to body diode forward voltage and more heating in NX30P6093A. The overtemperature protection will not disable the main switch for the same reason, but only report interrupt to system. In this case, the system should turn off the power source of USB OTG to protect the device and system.

5.3 Slew rate tune

The slew rate control is integrated to avoid inrush current when the load switch turns on. It protects the internal circuits or blocks follow NX30P6093A. In order to increase the design flexibility on system level, the slew rate can be tuned through I^2C through register 0x0F as follows:

Table 2. Slew rate tune setting by I^2C register

Register Value SRT[2:0]	Switch turn on slew rate (TYP)
000	0.42ms
001	0.44ms
010	0.5ms
011	0.65ms
100	0.9ms (Default)
101	1.5ms
110	2.8ms
111	5.6ms

5.4 Under-voltage lockout

When EN is LOW and VIN < VUVLO, the under-voltage lockout (UVLO) circuits disable the power MOSFET. Once VIN exceeds VUVLO, if no other protection circuit is active and EN is LOW, the MOSFET is turned on automatically no matter what is the status of VOUT_EN in register 0x01h. If EN is HIGH, the MOSFET remaining at off and at low power mode.

5.5 Over-voltage lockout

When EN is LOW and VIN > VOVLO, the over-voltage lockout (OVLO) circuit will disable the power MOSFET. The OV_FLG in register 0x03h is set as “1” and an interrupt will be issued to notify the host. Once VIN drops below VOVLO and no other protection circuit is active, the power MOSFET will resume operation.

The OVLO feature can be adjusted by both external resistor divider with ADJ pin and internal I2C register. The sequences are:

- When NX30P6093A is powering up, the initial OVLO threshold is set by ADJ pin. If there is a resistor divider connected to ADJ pin, the OVLO threshold is set by resistor divider value; If ADJ is floating or pull to ground, the OVLO threshold is set by default

value. After power up, the OVLO threshold can be adjusted by system through I2C register 0x05h

5.6 Short circuit protection

NX30P6093A has short circuit protection; after the MOSFET is fully turned on and when the current through it exceeds 10.5A typically, it turns the MOSFET off to protect the device and system. An interrupt is issued when short circuit protection is triggered by setting OC_FLG as "1" in register 0x03h. Once the short circuit condition is removed and no other protection circuit is active, the state of the N-channel MOSFET is controlled by the $\overline{EN}$ pin again.

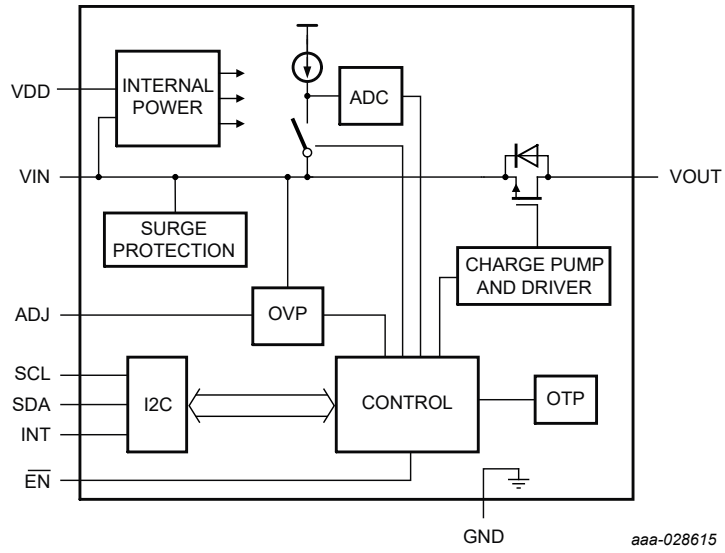


Figure 3. Short circuit protection

5.7 VIN impedance detection

VIN impedance detection function can only begin when EN is LOW and VIN <VUVLO. While in VIN detection mode, at any time when VIN pin exceeds VUVLO, NX30P6093A will exit from VIN detection mode to OVP mode immediately.

With the help of a host, NX30P6093A can start the VIN impedance detection according to the following sequence. First, set both VOUT_EN and DETC_EN bit to “1”. After wake-up time tWAKEUP, the host must then write ISOURCE, tDET, tDUTY and VTAG voltage from registers 0x06h, 0x07h and 0x09h through I2C.

VIN detection ADC result is valid only after tDET times out, setting TMR_OUT_STS to “1” and an interrupt is triggered. The host can also read VIN detected Voltage VIN[7:0] at register 0x08h. At the same time NX30P6093A will compare the detected VIN Voltage against the VTAG Voltage TVIN[7:0] in register 0x09h. When the detected voltage is less than the VTAG voltage, the OVER_TAG_STS sets to “1” in register 0x02h and an interrupt is triggered.

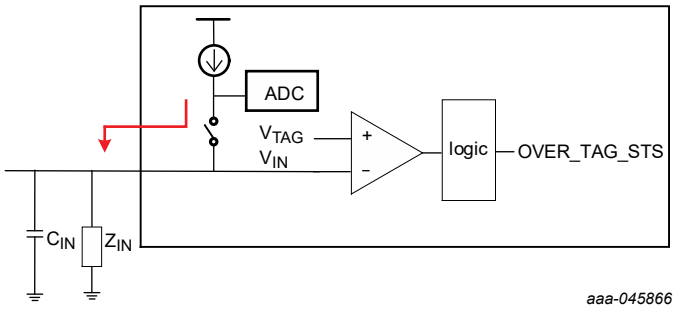


Figure 4. Moisture detection circuit

6 Debugging (or starting parts of) an application circuit

6.1 Moisture detection procedure

When abnormal impedance is detected and reported to the system, the OS can show a warning message for end user:

- Unplug any accessory on USB connector
- Clear the USB connector to remove possible moisture or dust

1. Write Enable Register (0x01h), VOUT_EN=0, DETC_EN=1; (0x40h)

Table 3. Enable Register (address 0x01h)

Bit	Name	Type	Reset Value	Description
7	VOUT_EN	R/W	0h	0h = Main switch MOSFET turned on
				1h = Main switch MOSFET turned off
6	DETC_EN	R/W	0h	0h = ISOURCE VIN impedance detection turn off
				1h = ISOURCE VIN impedance detection turn on
5:0	Reserved	R/W	0h	0h = default

2. Write desired I_{SOURCE} (0x06h) = 100µA (0x09h), I_{SOURCE} Timing (0x07h) = (0x87h) for t_{DET} 100ms (0x8-h), & t_{DUTY} 1000ms (0x-7h) and Tag voltage (0x09h) to 2V = (0xBEh) for 256*(2V/2.7V) = 190 = 0xBE

   This is the register to set I_{source} value for VIN impedance detection.

Table 4. I_{source} to VIN register (address 0x06h)

Bit	Name	Type	Reset Value	Description
7:4	Reserved	R/W	0h	0h = Default
3:0	ISRC[3:0]	R/W	0h	I_{source} current value setting bits

This is the register to set I_{source} timing for VIN impedance detection.

Table 5. I_{source} timing register (address 0x07h)

Bit	Name	Type	Reset Value	Description
7:4	TDET[3:0]	R/W	0h	I_{source} current pulse width setting bits
3:0	DUTY[3:0]	R/W	0h	VIN Impedance detection duty cycle setting bits

This is the register to set the tag of VIN voltage in VIN impedance detection.

Table 6. Set tag on VIN register (address 0x09h)

Bit	Name	Type	Reset Value	Description
7:0	TVIN[7:0]	R/W	00h	Set tag of VIN voltage bits. The TVIN [7:0] can be calculated as: $TVIN[7{:}0] = \frac{V_{TAG}}{2.7} \times 256$ Where, TVIN is decimal data and should be transfer to binary to TVIN[7:0]

3. Poll 3 consecutive times VIN DETECT (0x08h) & Status (0x02h) bit 6 == 1➔ MOISTURE DETECTED

This is the register to store the VIN voltage detection results from ADC.

Table 7. Voltage on VIN register (address 0x08h)

Bit	Name	Type	Reset Value	Description
7:0	VIN[7:0]	R	0h	VIN voltage detection results. The detected VIN voltage can be calculated as: $VIN[7{:}0] = \frac{V_{DET}}{2.7} \times 256$ Where, VIN[7:0] is decimal value of this register.

Table 8. Status register (address 0x02h)

Bit	Name	Type	Reset Value	Description
7	PWRON_STS	R	0h	0h = VIN voltage less than V_{UVLO}
				1h= VIN voltage larger than V_{UVLO}. An interrupt will be issued
6	OVER_TAG_STS	R	0h	0h = VIN detected voltage larger than Tag voltage
				1h = VIN detected voltage less than Tag voltage. An interrupt will be issued
5	TMR_OUT_STS	R	0h	0h = t_{DET} timer is not out
				1h = t_{DET} timer out. An interrupt will be issued
4	SWON_STS	R	0h	0h = The main switch is turn off

Table 8. Status register (address 0x02h)*...continued*

Bit	Name	Type	Reset Value	Description
				1h= The main switch is turn on. An interrupt will be issued
3	OTG_STS	R	0h	0h = The device is not in OTG mode
				1h = The device is in OTG mode
3:0	Reserved	R	0h	0h = default

7 Optional circuit and application tricks

7.1 NX30P6093A USB OTG

USB OTG is supported when the plugged accessory is recognized as an OTG device by system and a 5V source is applied on VOUT pin of NX30P6093A. The $\overline{EN}$ pin and VOUT_EN bit in register 0x01 must to be set LOW to support USB OTG mode. If $\overline{EN}$ pin or VOUT_EN bit is HIGH, the current is conducted by body diode that induces much higher power dissipation due to body diode forward voltage and more heating in NX30P6093A. The over temperature protection will not disable the main switch for the same reason, but only report an interrupt to the system. In this case, the system should turn off the power source of USB OTG to protect the device and system.

To exit USB OTG mode, it is suggested to use $\overline{EN}$ toggling. The VIN, along with VOUT, is discharged by internal ~150ohm resistor when NX30P6093A is disabled ($\overline{EN}$ pulled HIGH) when VDD is present. If the total equivalent capacitance on VIN and VOUT is less than 22uF, the required time of ENB pulling HIGH is 10mS.

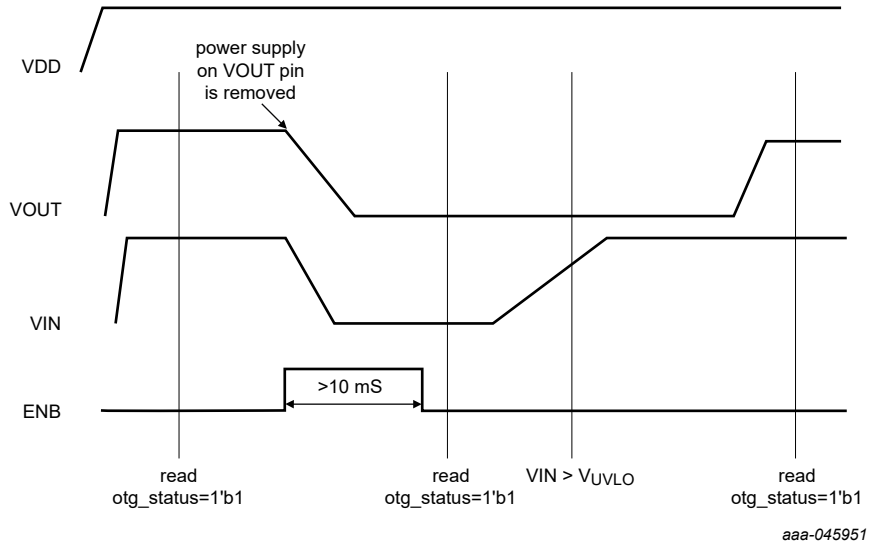


Figure 5. $\overline{EN}$ toggling

7.2 VIN discharge function

Figure 6. VDD= 3.3V, Load Capacitance = 10uF

Figure 7. VBUS pin going down below Vsafe0V and Vsafe5V after VBUS detached and switch disabled. Maximum 650ms below Vsafe0V, and Maximum 275ms below Vsafe5V

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