AN13168

Migration Guide from LPC546xx to LPC54(S)0xx and LPC54(S)0xxJxM

Rev. 2.0 — 22 September 2025 Application note

Document information

Information	Content
Keywords	AN13168, LPC546xx family of MCUs, LPC54(S)0xx, LPC54(S)0xxJxM, Quad SPI Serial Flash, feature comparison, migration guide, application note, Enhanced Code Read Protection (ECRP)
Abstract	This document describes guidelines on migrating a design from LPC546xx to LPC540xx and LPC540xxJxM microcontroller families.

1 Introduction

This document describes how to migrate your design from an LPC546xx to one using LPC540xx and LPC540xxJxM devices. It also focuses on addressing the changes in functionality between these two series of LPC MCUs. For simplicity reasons, this document refers to LPC540xx/ LPC54S0xx and LPC540xxJxM/ LPC54S0xxJxM as LPC54(S)0xx and LPC54(S)0xxJxM respectively.

Note: *LPC54(S)0xx and LPC54(S)0xxJxM are basically the same. The main difference between these devices is that:*

- *LPC54(S)0xx does not have an internal flash.*
- *LPC54(S)0xxJxM has an on-chip Quad SPI flash (connected to the SPI interface internally).*

2 Flash, RAM, and EEPROM2

The LPC546xx family of MCUs include up to 512 kB of flash, up to 200 kB of on-chip SRAM, and up to 16 kB of EEPROM memory.

The LPC540xx/LPC54S0xx family includes 360 kB of on-chip SRAM and it supports Quad SPI Flash XIP. However, it does not have an internal flash.

LPC54018JxM / LPC54S018JxM family includes up to 4 MB of on-chip Quad SPI Serial Flash (connected on SPIFI interface), 360 kB of on-chip SRAM.

Note: *Memory mapping between LPC546xx and LPC540xx/LPC540xxJxM is different. Refer to the corresponding User Manual for details.*

2.1 Package and pinout considerations

LPC546xx and LPC54(S)0xx have the below four packages:

- 100-pin, TFBGA
- 180-pin, TFBGA
- 208-pin, LQFP
- 100-pin, LQFP

Table 1. Pinout comparison

Device feature	LPC546xx	LPC540xx / LPC54S0xx	LPC54018JxM / LPC54S018JxM
Flash	up to 512 kB	None	Up to 4 MB of on-chip Quad SPI Serial Flash
SRAM	up to 200 kB	360 kB	360 kB
EEPROM	up to 16 kB	None	None

Note: *LPC546xx and LPC54(S)0xx devices are pin to pin compatible. However, LPC54(S)0xxJxM is not compatible with them due to the presence of an* ***internal QSPI flash****. Some pins of LPC540xxJxM/ LPC54S0xxJxM are connected with an internal on-chip QSPI flash.*

Table 1 lists the main differences between LPC54(S)0xxJxMET180 and LPC546xx, LPC54(S)0xx. For the hardware design, refer to the LPC54S018M-EVK schematics.

Table 2. Pinout comparison

Symbol	LPC54(S)0xxJxMET180
N7(P0_23)	This pin must be connected to C4(P4_16).
C4(P4_16)	This pin must be connected to N7(P0_23).

Table 2. Pinout comparison*...continued*

Symbol	LPC54(S)0xxJxMET180
A4(P4_15)	This pin is connected to VDD, which is a single 2.7 V to 3.6 V power supply. It powers internal digital functions and I/Os.
K8(PIO0_25)	This pins are not connected pins These pins must be left unconnected (floating).
L9(PIO0_27)	
M7(PIO0_24)	
M9(PIO0_28)	
M13(PIO0_26)	

3 Peripherals and frequency

Both LPC546xx and LPC540xx/LPC540xxJxM devices have the same peripherals. LPC546xx has up to 10 Flexcomm interfaces, whereas LPC540xx/LPC540xxJxM has up to 11 Flexcomm interfaces (Flexcomm 10 is dedicated for SPI).

LPC546xx can run at a frequency of up to 220 MHz, whereas LPC54(S)0xx/LPC54(S)0xxJxM can run at a frequency of up to 180 MHz.

4 Image protection and security

LPC546xx devices support ECRP (Enhanced Code Read Protection). However, the LPC54(S)0xx and LPC54(S)0xxJvM devices do not support this feature. The LPC54S0xx/LPC54S0xxJxM supports cyclic redundancy checks (CRC) integrity verification and secure boot.

Table 3. Image protection and secure boot comparison

	LPC546xx	LPC540xx / LPC540xxJvM	LPC54S0xx / LPC54S0xxJxM
ECRP	√	×	×
CRC image integrity verification	√	√	√
Secure boot	×	×	√

LPC54S0xx and LPC54S0xxJxM have security enhanced features AES and Physically Unclonable Functions (PUF).

The PUF controller provides secure key storage without storing the key. The To achieve this, digital fingerprint of a device derived from SRAM is used. Instead of storing the key, a 'key code' is generated. The key code is used in combination with the digital fingerprint to reconstruct keys that are routed to the AES engine or for use by the software. The PUF controller provides generation and secure storage for keys.

AES can use the key from One-Time Programmable (OTP) or PUF. The OTP can store a scrambled key, and PUF index 0 key is routed to on-chip AES engine through an inaccessible internal bus, protecting or hiding the plain key to runtime software. (AES KEY registers are loaded with the reconstructed PUF key).

Table 4. Security feature comparison

Device feature	LPC546xx	LPC540xx/LPC540xxJvM	LPC54S0xx/LPC54S0xxJxM
Secure Hash Algorithm (SHA1/SHA2)	√	√	√
AES	×	×	√
PUF	×	×	√

5 Conclusion

LPC54(S)0xx/LPC54(S)0xxJxM is recommended to be used on new Security or USB products.

While LPC546xx executes code in an internal flash, LPC54(S)0xx executes code in the Quad SPI flash. Therefore, LPC546xx has better performance than LPC54(S)0xx. Therefore, for LPC54(S)0xx, it is recommended to store the code with high-performance requirements in SRAM.

As described in the above sections, it is easy to migrate from LPC546xx to LPC54(S)0xx/LPC54(S)0xxJxM.

6 Acronyms and abbreviations

Table 5. Acronyms and abbreviations

Acronym/abbreviation	Description
AES	Advanced Encryption Standard
CRC	Cyclic Redundancy Check
ECRP	Enhanced Code Read Protection
EEPROM	Electrically Erasable Programmable Read-Only Memory
LQFP	Low-Profile Quad Flat Package
OTP	One-Time Programmable
PSIRT	Product Security Incident Response Team
PUF	Physically Unclonable Function
QSPI	Quad Serial Peripheral Interface
RAM	Random Access Memory
SHA1	Secure Hash Algorithm 1
SHA2	Secure Hash Algorithm 2
SPI	Serial Peripheral Interface
SPIFI	SPI Flash Interface
SRAM	Static Random Access Memory
TFBGA	Thin Fine-Pitch Ball Grid Array
USB	Universal Serial Bus
VDD	Voltage Drain Drain (Power Supply)
XIP	Execute In Place

7 Revision history

Table 6. Revision history

Document ID	Release date	Description
AN13168 v.2.0	22 September 2025	Aligned to the current NXP document template
AN13168 v.1.0	17 March 2021	Preliminary release

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Contents