AN12836

How to Use the Interconnection of OPAMP, ACMP1 and FDS for S08PB16

Rev. 0 — May 2020 Application Note

1 Introduction

MC9S08PB16 is a low-cost, highly-integrated and low pin count 8-bit MCU. It is based on the enhanced S09L core platform with Operational Amplifier (OPAMP) module, Analog Comparator (ACMP) module, Fault Detection and Shutdown (FDS) module integrated.

S08PB16 contains a set of system-level logics for module-to-module interconnection for flexible configuration. These interconnections provide the hardware trigger function between modules with least software configuration. The interconnection of OPAMP, ACMP1 and FDS modules can be used for low-end motor control and other general-purpose applications to implement overcurrent/overvoltage/over-temperature protection.

This application note introduces the features of OPAMP, FDS how to implement the interconnection of OPAMP, ACMP1, FDS modules.

There also an example code about how to implement the interconnection to implement overvoltage protection. The software in this document is based on CodeWarrior 11.1 IDE (must install the service pack: CodeWarrior MCU 11.1 Service Pack for S08PB and S08PLS), S08PB16-EVK board.

Contents

2 Features

2.1 OPAMP introduction

S08PB16 has one on-chip fixed gain (20x), single-ended input current sense amplifier (OPAMP) module. The positive input OPAMP+ is available on PTA3/KBI0P3/TXD0/SCL/ACMP1IN0/OPAMP+/ADP3 and the negative input OPAMP- is tied to GND.

The OPAMP analog output connects internally to ACMP1 or ADC input channel AD12. The OPAMP analog output is not available on an external pin.

In order to measure both positive and negative currents, an internal reference voltage must be used. Reference voltage VREF is controlled by `SYS_SOPT6_VREFSEL` bit to 1/2 VDDA, 1/4 VDDA or 1/8 VDDA reference level and added it to positive input of amplifier. The current sensor could be enabled independently by `SYS_SOPT6_AMPEN`. Table 1 summarizes the properties.

Table 1. OPAMP properties

Name		Function	
OPAMP signals	OPAMP+	PTA3/KBI0P3/TXD0/SCL/ACMP1IN0/ OPAMP+/ADP3	Default gain: 20 x
	OPAMP-	GND	
	OPAMP output	ACMP1	Only connect internally
		ADC channel 12	

Table continues on the next page...

Table 1. OPAMP properties (continued)

Name		Function	
OPAMP control registers	SYS_SOPT6_VREFSEL	Select Vref for OPAMP module	Default: Vref = 1/2 VDDA
	SYS_SOPT6_AMPEN	Enable or disable OPAMP module	—

There is one current sense amplifier (OPAMP) in S08PB16 to sense the current flowing through the external resistor shunt as a voltage across the resistor. Typical usage is to be used to sense the two phases current or the DC bus current in BLDC motor control application.

The output of OPAMP is connected to the ACMP1 inputs which can be used as over current protection. Users can configure over-current value by setting ACMP1 registers to select the positive and negative inputs. The interrupt output of ACMP1 is connected to FDS module. The outputs of FDS module is connected to PWM channels and control the states of PWM channels.

Figure 1 shows the interconnection of OPAMP and ACMP1.

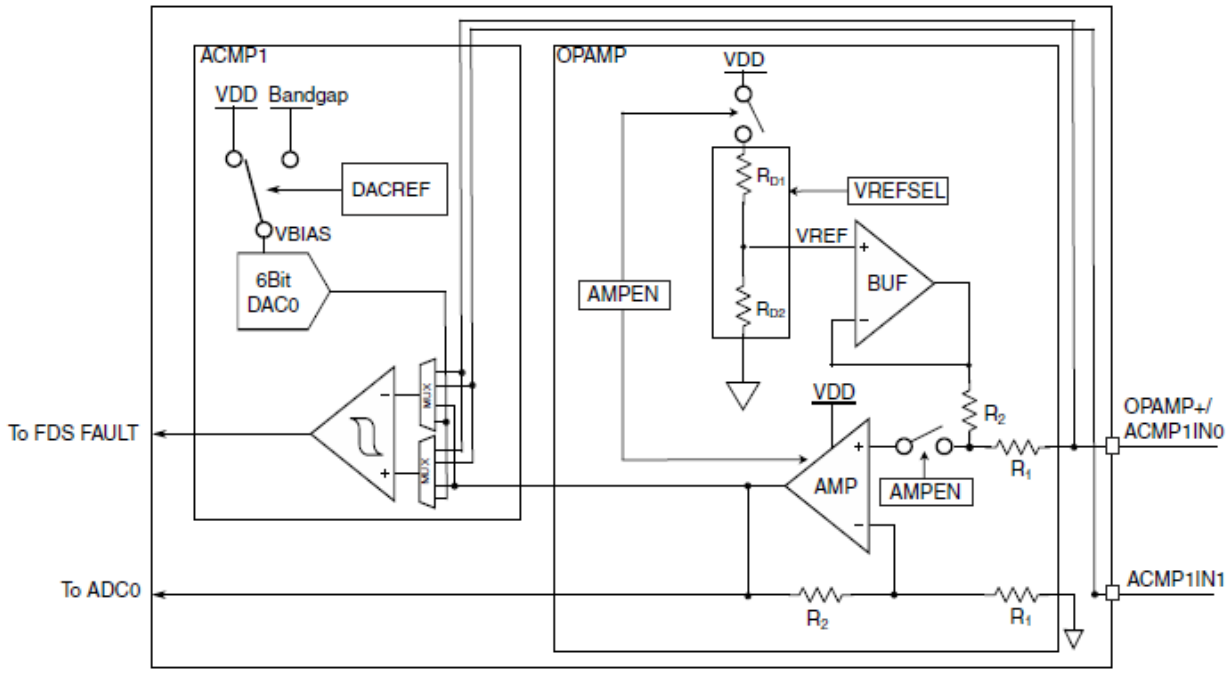

Figure 1. OPAMP and ACMP1 interconnection

2.2 FDS introduction

2.2.1 FDS inputs and outputs

S08PB16 has the Fault Detect and Shutdown (FDS) module which provides a mechanism to immediately place port pins in a pre-defined state when a fault condition occurs. FDS module is configurable with eight fault input sources (as shown in Table 2) and control of eight port pins (as shown in Table 3). The control of eight fault inputs and eight port pins can be independently configured. The FDS provides rapid shutdown for up to eight pins when a fault input is activated.

Table 2. FDS input configurations

Input control channel (FINn)	Input source & description
FIN0	KBIINT (KBI interrupt output)
FIN1	ACMP0INT (ACMP0 interrupt output)
FIN2	ACMP1INT (ACMP1 interrupt output)
FIN3	MTIM0INT (MTIM0 interrupt output)
FIN4	MTIM1INT (MTIM1 interrupt output)
FIN5	PWTRDY (PWT interrupt output)
FIN6	FDSIN (FDS external fault input)
FIN7	Active BDM (Active BDM mode)

Table 3. FDS output configuration

Output control channel (FDSOUTx)	Output controlled function
FDSOUT0	PTC0/FTM2CH0
FDSOUT1	PTC1/FTM2CH1
FDSOUT2	PTC2/FTM2CH2
FDSOUT3	PTC3/FTM2CH3
FDSOUT4	PTB4/FTM2CH4
FDSOUT5	PTB5/FTM2CH5
FDSOUT6	PTA0/KBI0P0/FTM0CH0
FDSOUT7	PTA1/KBI0P1/FTM0CH1

2.2.2 FDS registers

The registers of FDS falls into three parts: FDS general control and status register, input control registers and output control registers. Table 4 lists all the registers.

Table 4. FDS registers table

Registers	Function	Description	
FDS_CS	Control and status register	FDF: Fault input flag FDIE: Fault interrupt enable/disabled FDEN: FDS enable/ disable FORCEF: FDS force fault if writing 1 to the bit.	FDS module enable configuration
FDS_INE	Input enable register	FINEx: This bit can enable or disable each of the eight optional fault inputs (FINn).	FDS input pin enable configuration, select FDS input source
FDS_INL	Input latched register	FINLx: This bit latches the status of fault input channel FINn.	

Table continues on the next page...

Table 4. FDS registers table (continued)

Registers	Function	Description	
FDS_PCE	Output pin configuration register	FPCEx: This bit sets a pin as FDSOUTx function or bypass.	FDS output pin action taken configuration
FDS_PCD	Output pin configuration direction register	FPCDx: This bit sets FDSOUTx as output or high impedance when corresponding FPCEx bit set.	
FDS_PCV	Output pin configuration value register	FPCVx: This bit set the value of FDSOUTx to 0 or 1 when corresoponding FPCDx bit set.	

2.3 FDS input and output configuration

Figure 2 shows the output pin control configuration and realization when a fault is detected.

1. FDS module is enabled by setting the FDS_CS register. Each input signal can be enabled independently by setting FDS_INE register. When a fault occurs in the input channel (FINn), the fault input is latched into the corresponding bit in FDS_INL register and FDF is set.
2. If the FDS_PCE register is set to **1**, the output pin (FDSOUTx) can be shut down and driven to the pre-defined states (output 1, output 0 or high impedance) by setting FDS_PCD and FDS_PCV registers.
3. The output pin is in bypass mode and outputs other functions if the FDS_PCE register is set to **0**. When the fault source (FINn) is removed and the FDF is cleared, the FDS module will release the control on corresponding pin (FDSOUTx) for PWM or other functions.

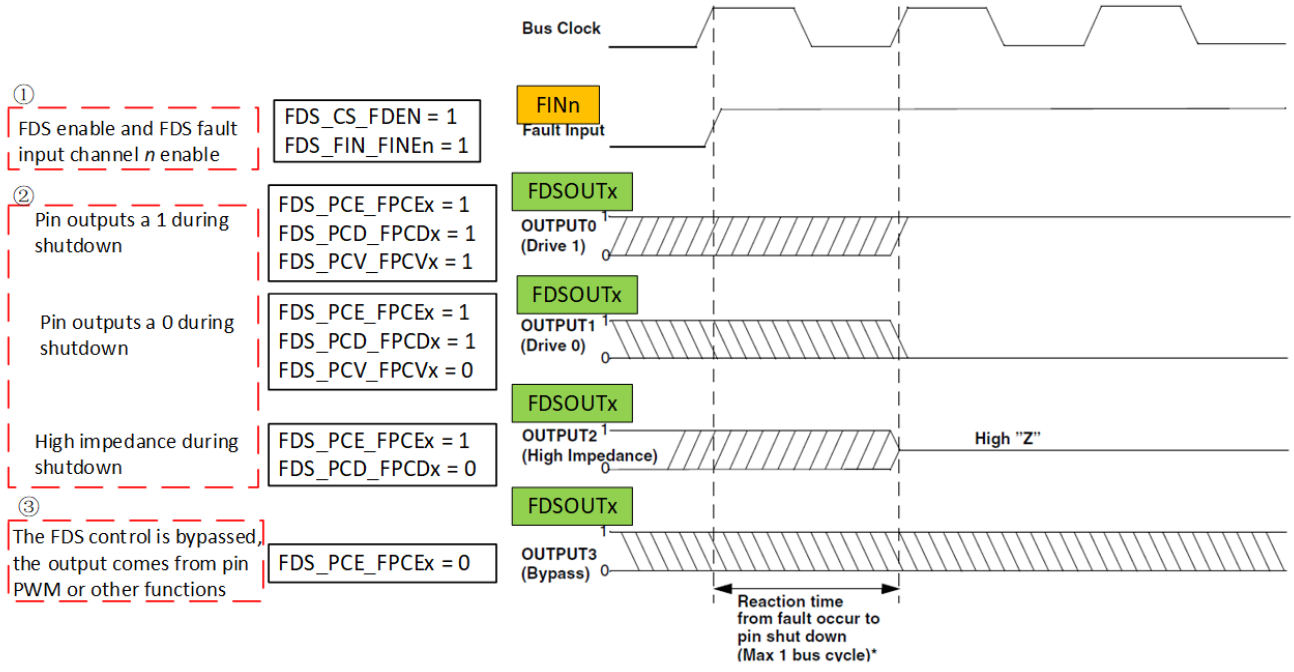

Figure 2. FDS output controlled configuration

2.4 Interconnection of OPAMP, ACMP1 and FDS

The interconnection of OPAMP, ACMP1 and FDS can be used for over current protection in motor control applications. Figure 3 shows the block diagram for the interconnection.

The output of OPAMP is interconnect to ACMP1 input, and it can be configured as the negative or positive input of ACMP1. Normally, use OPAMP output as the input of ACMP1+ and DAC output as the input of ACMP1-. The ACMP1 can be used for current/voltage limitation detection.

ACMP1 compares the OPAMP output with user-defined overcurrent/voltage settings. If there is overvoltage or overcurrent, the ACMP1 interrupt output is the fault input source of the FDS. At this time, a fault will be generated.

The FDS will be delayed by at most one bus clock. It will shut down the output pin. The PWM channel is turned off. The FDS controls the output of this pin and places port pins in a pre-defined state. At this time, the over-current/over-voltage protection function in the motor control is realized.

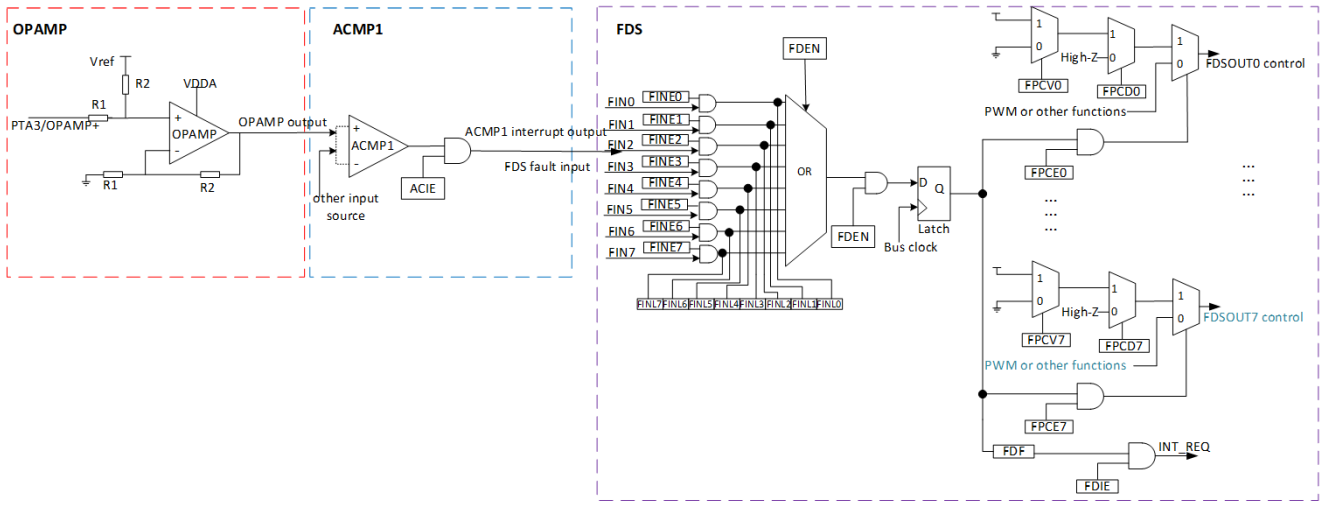

Figure 3. Interconnection of OPAMP, ACMP1 and FDS

3 Implementation details

This is the detailed information on how to use the interconnection of OPAMP, ACMP1, FDS to implement over voltage protection in S08PB16 MCU.

In the use case, FTM0 channel 1 is configured to output PWM signal on the PTA1/KBI0P1/FTM0CH1 pin. The OPAMP, ACMP1, and FDS are configured to protect PWM channel from over-voltage.

When the OPAMP output voltage is higher than the limitation voltage 2.7 V, it causes ACMP1 interrupt generated. The ACMP1 interrupt output is used as FDS fault input source (FIN2). Then FDS will shut down the PWM output of PTA1 pin and place PTA1 pin output value 0.

When the OPAMP input returns to lower voltage than limitation voltage 2.7 V, clear ACMP1 interrupt flag (ACF) and FDS interrupt flag (FDF), and the fault source is removed. The FDS will release the control of PTA1 pin. PTA1 pin restores PWM function. Figure 4 shows the flowchart.

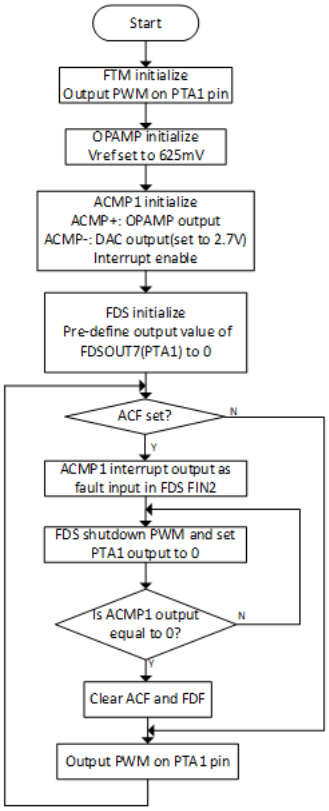

Figure 4. Flowchart

The following is a brief introduction to the `opamp_acmp1_fds` code. The code can be downloaded from http://www.nxp.com.

3.1 PWM signal generation

Configurate FTM0 channel 1 to generate PWM on the PTA1 pin to drive blue LED toggle. The configuration of FTM0 is shown as follows.

```
/* Initialize PTA1/FTM0CH1, PWM output to driver the LED */
void FTM0_Init( void )
{
   SYS_SCGC1_FTM0 =1;           // Bus clock to the FTM0 module is enabled

   FTM0_CNT = 0;                // set count value to 0
   FTM0_MOD = 3905;             // value: 3906
   FTM0_C1SC = 0x28;            // edge aligned FTM
   FTM0_C1V = 1952;             // duty: 50%

   /* FTM frequency = CLKS/PS/MOD = ICSFFCLK/2/4/MOD = 31.25K / 2 /4 /3906 = 1K */
   FTM0_SC = 0x12; // clock source = 10, Fixed Frequency Clock (ICSFFCLK) divided by 4, start the ftm
counter
}
```

3.2 OPAMP configuration

It only needs to configure the two bits of SOPT6 to complete the OPAMP configuration, shown as follows.

```
    /* Configure OPAMP reference to 1/8VDDA, 625mV. */
    SYS_SOPT6_VREFSEL = 0;
    /* Enable OPAMP */
    SYS_SOPT6_AMPEN =1;
```

For the S08PB16-EVK, turn around the Potentiometer R58 can change OPAMP negative input PTA3 when J12 1-2 is connected. In the example code, the reference voltage of OPAMP is 625 mV by setting `SYS_SOPT6_VREFSEL` to **0**. Then the output voltage is calculated by the formula OPAMP output = 625 mV + 20 × V_{PTA3}.

3.3 ACMP1 configuration

The correct configuration of ACMP1 module is an important step to implement voltage or current limiting protection.

In this article, the negative input of ACMP1 is driven by the internal programmable 6-bit DAC by setting `ACMP1_C0_ACNSEL`. The negative input value is set to 2.7 V by setting `ACMP1_C1_DACVAL`. The positive input of ACMP1 is driven by OPAMP output by setting `ACMP1_C0_ACPSEL`.

Note that the interrupt bit must be enabled during ACMP1 configuration. The interrupt output of ACMP1 is interconnect to FDS channel 2 (FIN2). ACMP1 interrupt is generated on ACMP1 output rising or falling edge by setting `ACMP1_CS_ACMOD` to **3**. The specific configuration of ACMP1is shown as follows.

```
/* Initialize ACMP1, ACMP1 interrupt must be enabled when select ACMP1 interrupt as FDS fault input */
void ACMP1_Init ( void )
{
    //ACMP_C1_DACVAL = 33;            //when 3.3V powered: 6bit DAC: (34/64)*3.3 = 1.75V
    ACMP1_C1_DACVAL = 34;             //when 5V powered:  6bit DAC: (35/64)*5 = 2.70V
    ACMP1_C1 |= ACMP1_C1_DACEN_MASK | ACMP1_C1_DACREF_MASK;    // enable DAC, select VDDA as the
reference

    ACMP1_C0_ACPSEL = 2;              // ACMP positive input: OPAMP output
    ACMP1_C0_ACNSEL = 3;              // ACMP negative input: DAC output
//    ACMP1_C2_ACIPE = 0;             // enable ACMP1 input on

    /* for test purpose, output the ACO to check the ACMP result on falling/rising ACMP interrupt */
    ACMP1_CS_ACOPE = 1;                // ACMP output enable, reading ACO can get ACMP result
    ACMP1_CS_ACMOD = 3;                //ACMP interrupt on output falling/rising edge
    ACMP1_CS_ACIE = 1;                 //enable ACMP interrupt to detect the start bit of SCI0 Rx

    ACMP1_CS_ACE = 1;                  // enable ACMP
}
```

The following code is the process that ACMP1 executes the Interrupt Service Routine (ISR)). If the FDS module has been initialized and the ACMP1 interrupt is generated, the FDS will respond and turn off the corresponding pin in less than 1 bus clock cycle.

In the ISR of ACMP1, it is judged whether the circuit is overvoltage/overcurrent according to the output value of ACMP1. If it is in an over-voltage state, the ACMP1 interrupt flag and FDS interrupt flag are not cleared, and overvoltage protection is performed. When the OPAMP output is less than the comparison voltage of 2.7 V, ACF and FDF are cleared, and the fault source will be removed. Then the output pin PTA1 will return to normal state to output PWM.

```
/* ACMP1 generate interrupt on raising / falling edge */
interrupt VectorNumber_Vacmp1 void ACMP1_ISR(void)
{
```

```
    while(!(ACMP1_CS & ACMP1_CS_ACF_MASK));

    while(!(FDS_CS & FDS_CS_FDF_MASK));

    PRINTF("Fault occurs.\r");


    /* when ACMP1 positive input(OPAMP output) smaller than negative input(2.7V), remove fault input
*/
    if(ACMP1_CS_ACO == 0)
    {
        ACMP1_CS_ACF = 0;           // clear ACMP1 interrupt flag
        FDS_CS_FDF = 0;              // clear FDS interrupt flag
        busyWait = 0;
        PRINTF("\n\nRemove fault source 'ACMP1 interrupt' \r\n");
    }
}
```

3.4 FDS configuration

According to the following code, the fault input source FIN2 is enabled, the output control channel FDSOUT7 is configured to output value **0**.

So when the fault source OPAMP output occurs, FDS module detects the fault and shuts down PWM signal (FTM0 channel 1) and places the PTA1/KBI0P1/FTM0CH1 pin to value **0**.

```
void FDS_Init(void)
{
    FDS_INE_FINE2 = 1;           // enable fault input 2, ACMP1 interrupt input

    FDS_PCE_FPCE7 = 1;           // enable FDSOUT7 function, PTA1/KBI0P1/FTM0CH1
    FDS_PCD_FPCD7 = 1;           // output pin FDSOUT7 as output
    FDS_PCV_FPCV7 = 0;           // output 0

    FDS_CS_FDF = 0;              // clear FDS interrupt flag
    FDS_CS_FDIE = 0;             // disable FDS interrupt
    FDS_CS_FDEN = 1;             // FDS enable
}
```

4 Conclusion

This application note explains the features of OPAMP, FDS and how to use the interconnection of OPAMP, ACMP1, FDS to implement over-current protection. Users can easily implement the function by reference to details of configuration. The code can be downloaded at S08PB16-EVK.

5 References

The following references are available on http://www.nxp.com:

1. *MC9S08PB16 Reference Manual* (document MC9S08PB16RM)
2. *How to Use GDU Module in MC9S08SU16* (document AN5395)

How To Reach Us

Home Page:

nxp.com

Web Support:

nxp.com/support

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: May 2020

Document identifier: AN12836

arm