AN12733

DSI3 Communication Procedure Recommendation for FXLS9xxxx

Rev. 1 — 8 January 2021

Application note
COMPANY PUBLIC

1 Introduction

The purpose of this document is to describe the DSI3 power up, initialization and normal mode procedures for the FXLS9xxxx single and dual channel inertial sensors.

2 Applicable Parts

This document applies to the following NXP sensors:

Table 1. Applicable parts

FXLS90xxx	uThornapple	Dual Channel DSI3 Inertial Sensor
FXLS90xxx	uLaurel	Single Channel DSI3 Inertial Sensor

3 Definition List

Table 2. Definition list

Term	Definition
Analog Self-Test	A method to test the acceleration signal chain by electrostatically deflecting the transducer proof mass and measuring the device output.
BRC	Broadcast Read Command. The broadcast read command is a single bit command enabling the Time Division Multiple Access (TDMA) slave transmissions in Periodic Data Collection Mode (PDCM).
CRM	DSI3 Command and Response Mode. A bidirectional communication method enabling communication between a single master and a single slave or multiple slaves. This mode is optimized for programming and control of slave devices and is primarily used for register reads and writes with the FSXL6xxxx devices.
Digital Self-Test	A method to test the digital portion of the acceleration signal chain by forcing a value or a sequence of values at the output of the analog to digital converter and measuring the device output.
Discovery Mode	DSI3 Discovery Mode. An automatic addressing scheme to provide physical addressing by location to a single master, multiple slave bus.
DSI3	Distributed Systems Interface, 3rd Generation. A single master, multiple slave communication interface that provides both slave power and communication on a 2-wire bus.
DSP	Digital Signal Processing Block
PDCM	DSI3 Periodic Data Collection Mode. A bidirectional communication method enabling communication between a single master and a single slave or multiple slaves. This mode is optimized for high speed sensor data transfers from multiple slaves to a single master. Slave responses are time division multiplexed. This mode is used for periodic acceleration data transfers on the FSXL6xxxx devices.
POR	Power On Reset

PSI5	Peripheral Sensor Interface, 5th Generation. A single master, multiple slave communication interface that provides both slave power and communication on a 2-wire bus.

4 Further Assistance

For further assistance please contact your local sales representative.

5 References

- FXLS9xxxx data sheet, latest revision: uThornapple data sheet
- FXLS9xxxx data sheet, latest revision: uLaurel data sheet
- DSI3 Standard, Revision 1.0, dated February 16, 2011
- PSI5 Technical Specification Version 2.1, dated October 8, 2012

6 Revision History

Table 3. Revision history

Rev. No.	Date	Description
1.0	20210108	Created FXLS9xxxx application note from FXLS7xxxx application note

7 Application Schematics

7.1 FXLS9xxxx application schematic

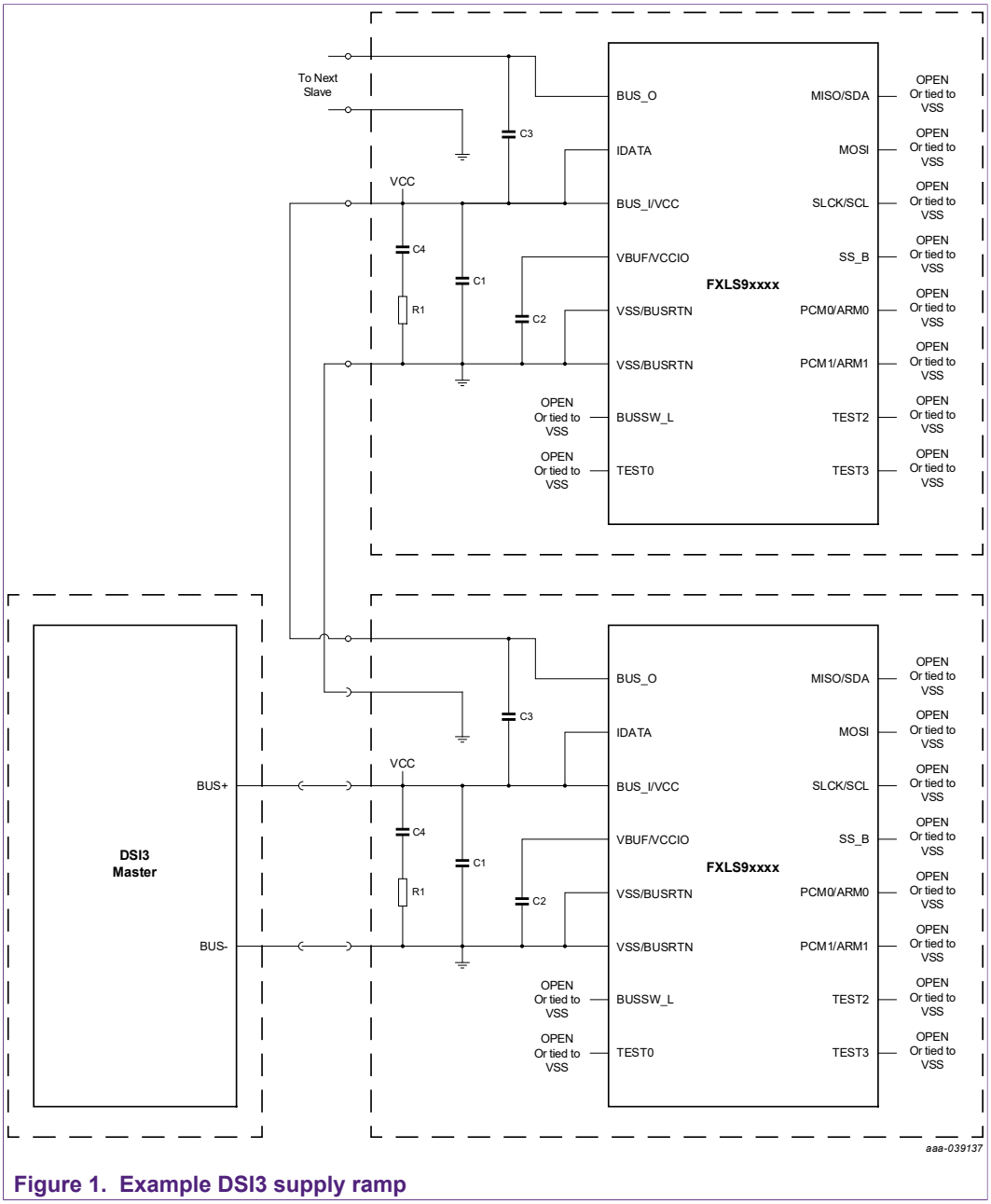

Figure 1. Example DSI3 supply ramp

Table 4. Recommended external components for DSI3 mode

Reference designator	Component type	Description	Comment
R1	General Purpose	330 Ω, 5%, 200 ppm	The optimal value of this component should be determined by the system level communication and EMC testing.
C1	Ceramic	220 pF, 10%, 50 V minimum, X7R	The optimal value of this component should be determined by the system level communication and EMC testing.

Reference designator	Component type	Description	Comment
C2	Ceramic	0.47 µF, 10%, 10 V minimum, X7R	The optimal value of this component should be determined based on the system level micro-cut immunity requirement. To achieve the specified power supply rejection, the minimum value including all tolerances is 0.22 µF. The maximum specified value including all tolerances is 2 µF.
C3	Ceramic	1000 pF, 10%, 50 V minimum, X7R	The optimal value of this component should be determined by the system level communication and EMC testing.
C4	Ceramic	2200 pF, 10%, 50 V minimum, X7R	The optimal value of this component should be determined by the system level communication and EMC testing.

8 Apply Power to the FXLS9xxxx

Power must be applied to the FXLS9xxxx with the ramp rates specified in the datasheet. The device is verified to properly startup with ramp rates from 10 V/s to 10 V/µs.

The device is available for Command and Response Mode commands within 13.5 ms of POR release. If Discovery Mode is planned to be used for physical address assignment, the supply ramp time must be fast enough to allow for the device to participate in Discovery Mode.

From the slave perspective, the Discovery Mode window is from 6.0 ms to 13.5 ms of POR release. From the master perspective, this time must be known within reasonable accuracy. The time from the master enabling the bus until the slave POR release results in a time skew between the master and slave interpretation of the Discovery Mode window start time. With a slow supply ramp time, relative to the Discovery Mode window start time (< 5 V/ms), the time skew between the master and slave could result in the slave(s) missing the Discovery Mode transmissions from the master.

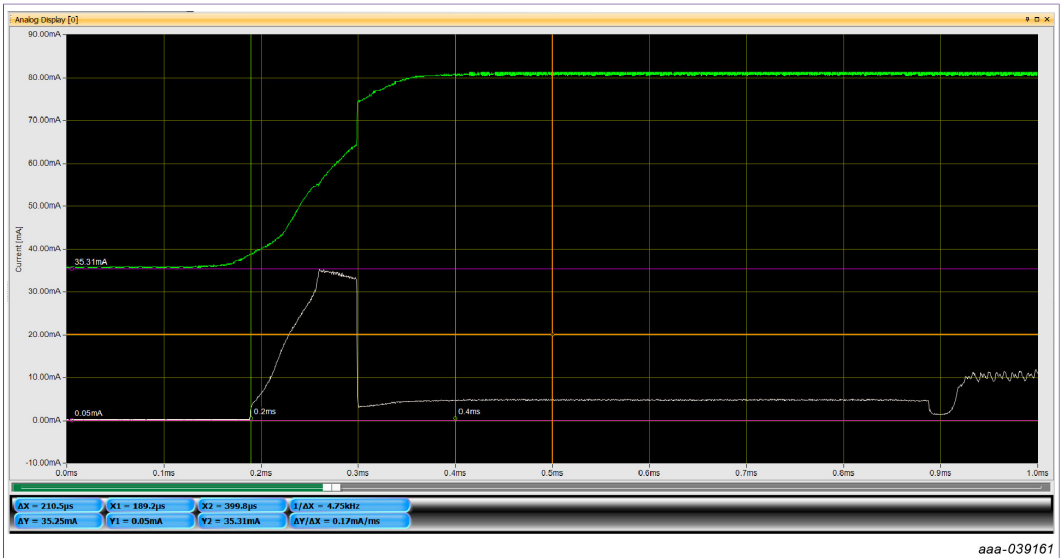

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Figure 2. Example DSI3 supply ramp

9 Assign Addresses to the Slaves

9.1 Single device network

DSI3 supports the capability to connect one slave to a master in a point to point connection. With this connection method, the physical address of the slave must either be 0x00 or be known beforehand by the master.

9.1.1 Unprogrammed physical address (0x00)

A single device network with an unprogrammed physical address can be initialized using either Discovery Mode as documented in Section 9.2 "Multiple slave system connected in a resistor connected daisy chain" or using Command and Response Mode (CRM). The following CRM procedure is necessary to complete address assignment of an unprogrammed slave with a physical address of 0x00.

Delay a minimum of 13.5 ms from applying power ($t_{START\_DISCMAX}$)

Using Command and Response Mode (CRM), send a global write command to the Physical Address register (PHYSADDR), setting the physical address to a non-zero value. The example in Figure 3 shows the command necessary to program the physical address to 0x1.

Table 5. CRM global write command and response

Description	Slave address (Hex)	Command (Hex)	Register address (Hex)	Register data (Hex)	Full message (Hex)
Command	0	8	18	01	0x08180112
Response	1	8	00	01	0x18000152

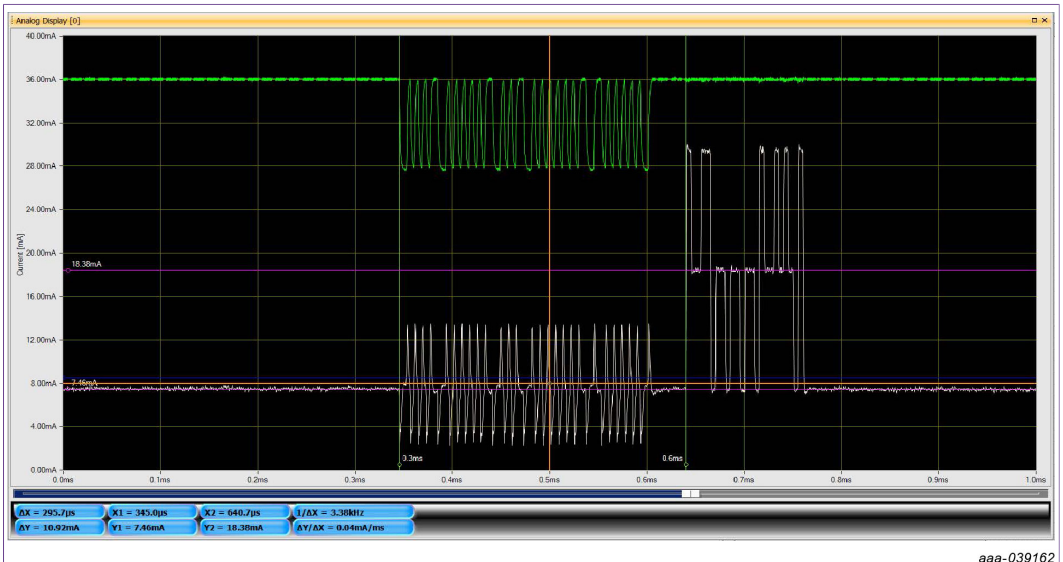

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Figure 3. Master and slave signals for the global write to the PHYSADDR register

9.1.2 Pre-programmed physical address

No action is necessary if the single slave device has a pre-programmed address. Proceed to Section 10 "Initialize and Configure the Devices"

DSI3 supports the capability to connect multiple slaves to a master in a parallel or start connection. With this connection method, the physical addresses of the slaves must be known beforehand by the master. No other action is necessary for address assignment. Proceed to Section 10 "Initialize and Configure the Devices"

9.2 Multiple slave system connected in a resistor connected daisy chain

Discovery Mode follows the sequence listed below. Figure 4 shows a timing diagram of the Discovery Protocol for a four-slave segment.

1. The master powers up the bus segment to a known state.
2. The master transmits the Discovery Command.
3. After a predetermined delay ($t_{START\_DISC\_RSP}$), all slaves without a physical address activate a current ramp to the 2x response current at a ramp rate of i_{DISC_RAMP}.
4. Each slave monitors current through its sense resistor (Δi_{SENSE}).
   a. If the current is above i_{RESP}, the slave disables its response current, increments its physical address counter, and waits for the next Discovery Command.
   b. If the current is low (Δi_{SENSE} less than i_{RESP}), the slave continues to ramp its response current to 2* i_{RESP} in time $t_{DISC\_RAMP\_RSP}$ and maintains the current at 2* i_{RESP} for time $t_{DISC\_IDLE\_RSP}$.
   c. After time $t_{DISC\_IDLE\_RSP}$, if a slave has not detected a current through its current sense resistor of i_{RESP}, the slave accepts physical address '1' and disables its response current.
5. After a pre-defined period (t_{PER_DISC}), the master transmits another Discovery Command.
6. Steps 3 and 4 are repeated, with the slave accepting the address in its address assignment counter if the sense current is low.
7. The master repeats step 5 until it has transmitted Discovery Commands for all the slaves it expects on the bus.

Device initialization can now begin using Command and Response Mode. Proceed to Section 10 "Initialize and Configure the Devices" .

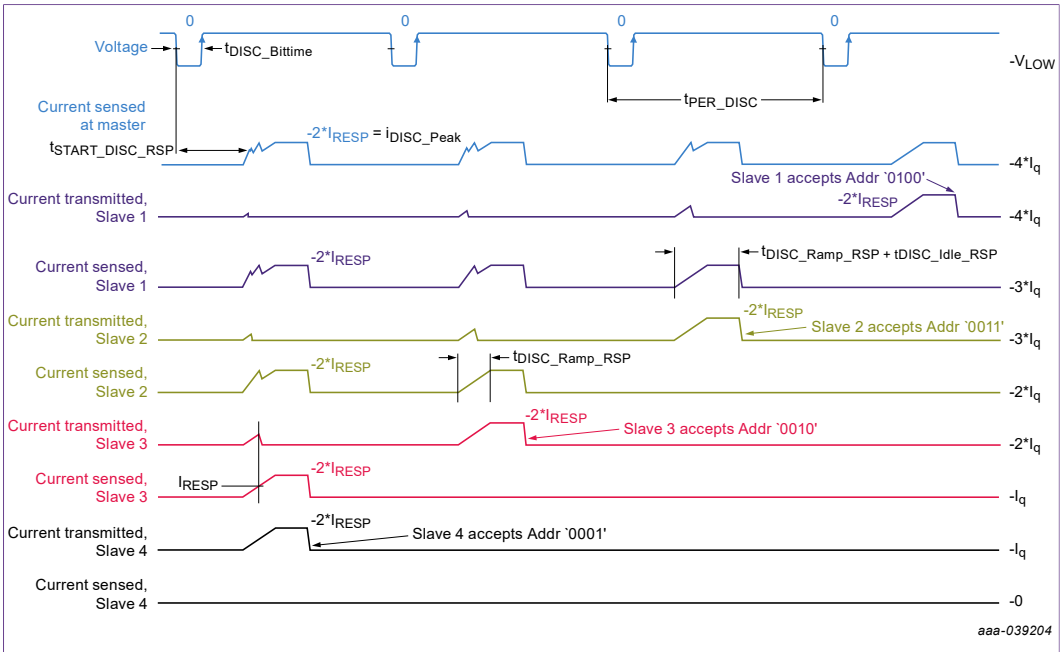

Figure 4. Four device Discovery Mode process

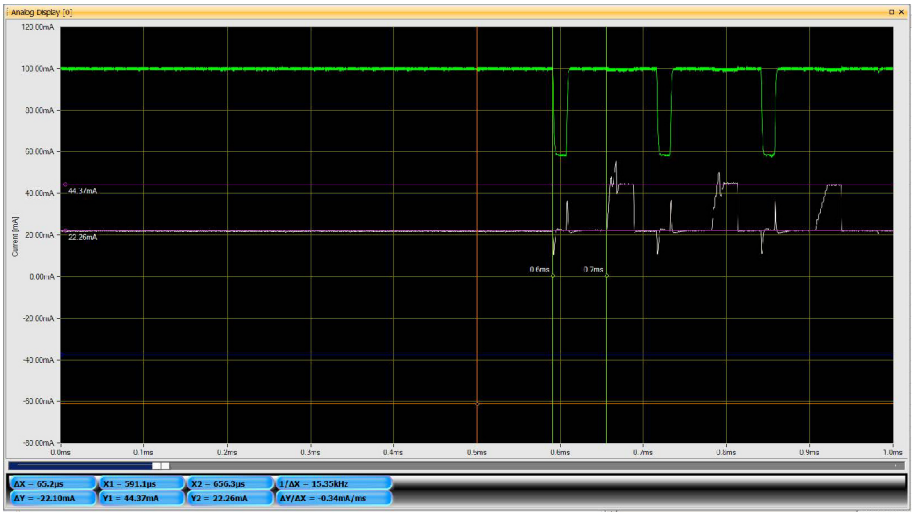

Figure 5. Four example three slave Discovery Mode

9.3 Multiple slave system connected in a high side switch connected daisy chain

The FXLS9xxxx devices do not support the capability to connect multiple slaves to a master in a daisy chain connected by high side bus switches. Contact a local NXP sales representative for alternative options for switch connected daisy chain mode.

10 Initialize and Configure the Devices

Once all slaves on the bus have a unique physical address, the master can initialize and configure the slaves as desired for the application. The following sections describe the recommended CRM commands to initialize, configure and test a bus with two FXLS9xxxx devices.

Figure 6 shows a timing diagram example for SPI Start Up and initialization and how it compares to the internal offset cancellation start up. Table 6 shows a timing table for the procedure used in this application note. Figure 7 shows a high-level flow chart for the procedure used in this application note.

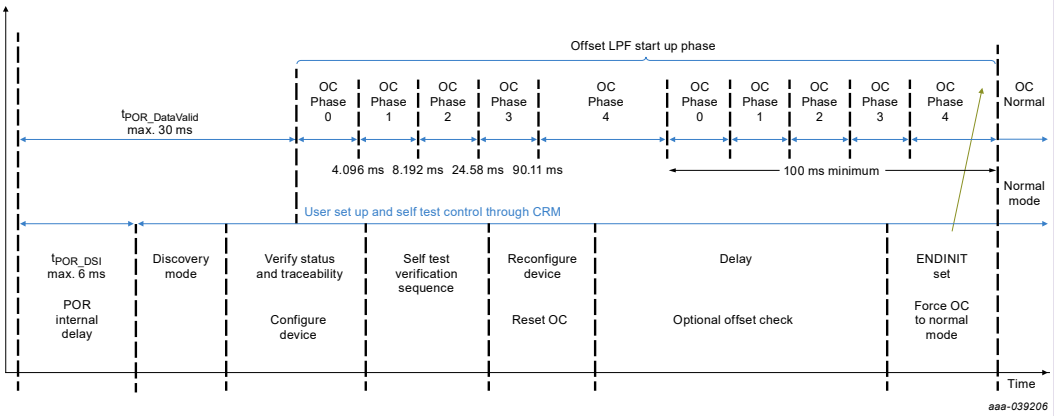

Figure 6. Example DSI3 initialization timing diagram

Table 6. Example DSI3 timing table

Function	Start time	End time	Units
POR	0	5.93	ms
Discovery end	5.93	6.18	ms
CRM start	26.71	26.71	ms
Device status	26.71	29.71	ms
Register pattern write	62.71	66.71	ms
Configuration #1	66.71	78.36	ms
Read self-test stored values	78.36	84.36	ms
Traceability	84.36	91.36	ms
Fixed pattern self-test	91.36	99.36	ms
Offset	99.36	115.36	ms
DIgital self-test	115.36	134.86	ms
Analog self-test: Ch0+, Ch1–	134.86	166.37	ms
Analog self-test: Ch0–, Ch1+	166.37	187.87	ms
Post self-test offset	187.87	209.37	ms
Configuration #2	209.37	221.02	ms
Reset offset cancellation	221.02	322.52	ms
Device satus	322.52	325.52	ms

Function	Start time	End time	Units
Post OC offset	325.52	357.69	ms
ENDINIT	357.69	—	ms

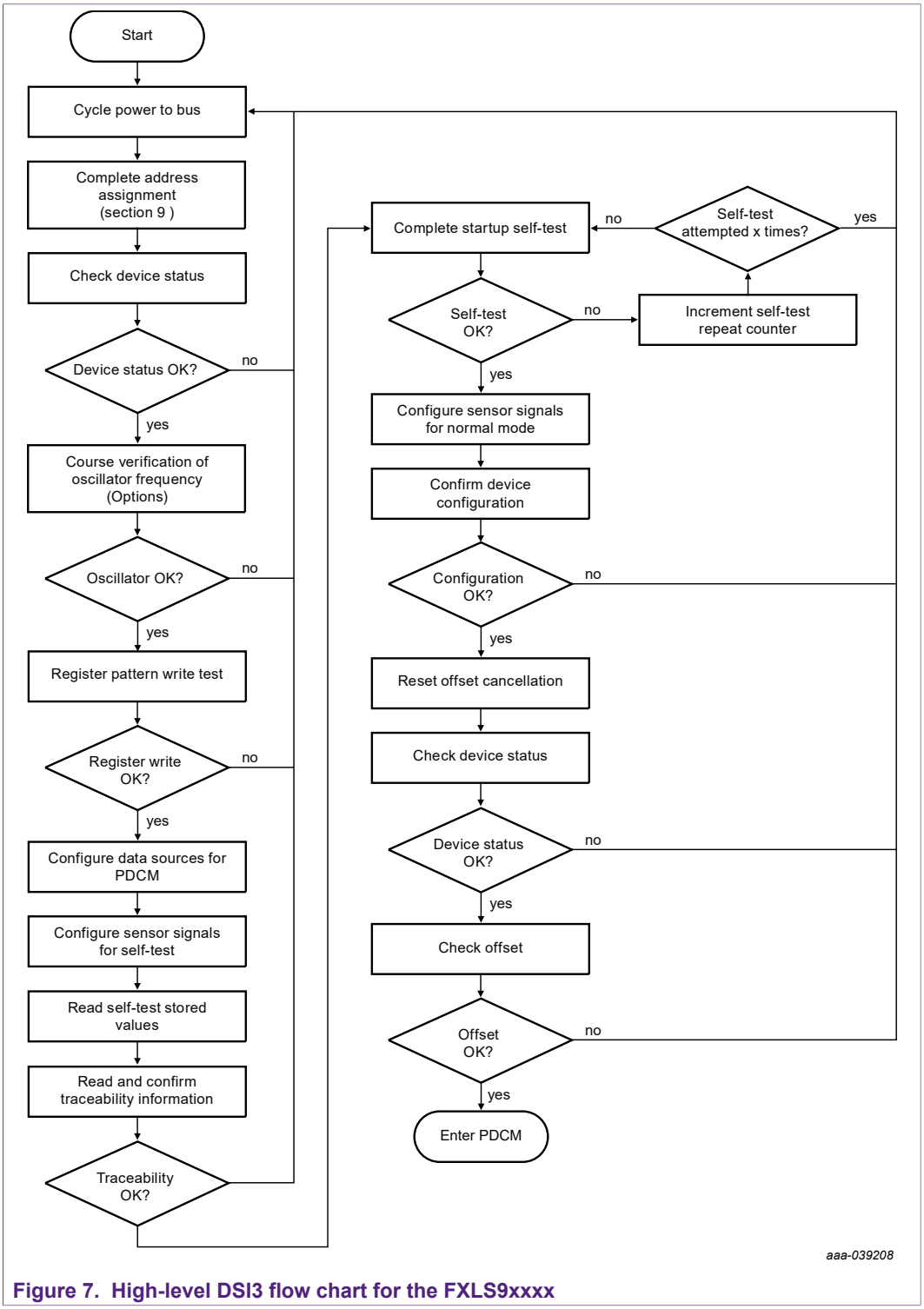

Figure 7. High-level DSI3 flow chart for the FXLS9xxxx

10.1 Confirm device status

The first step after address assignment is to confirm proper CRM communication and the expected status of each device. This is accomplished by reading the DEVSTAT registers of each device as shown in Figure 8. The DEVSTAT register mapping is shown in Figure 9.

Optionally, the user can also complete a course verification of the slave oscillators as shown.

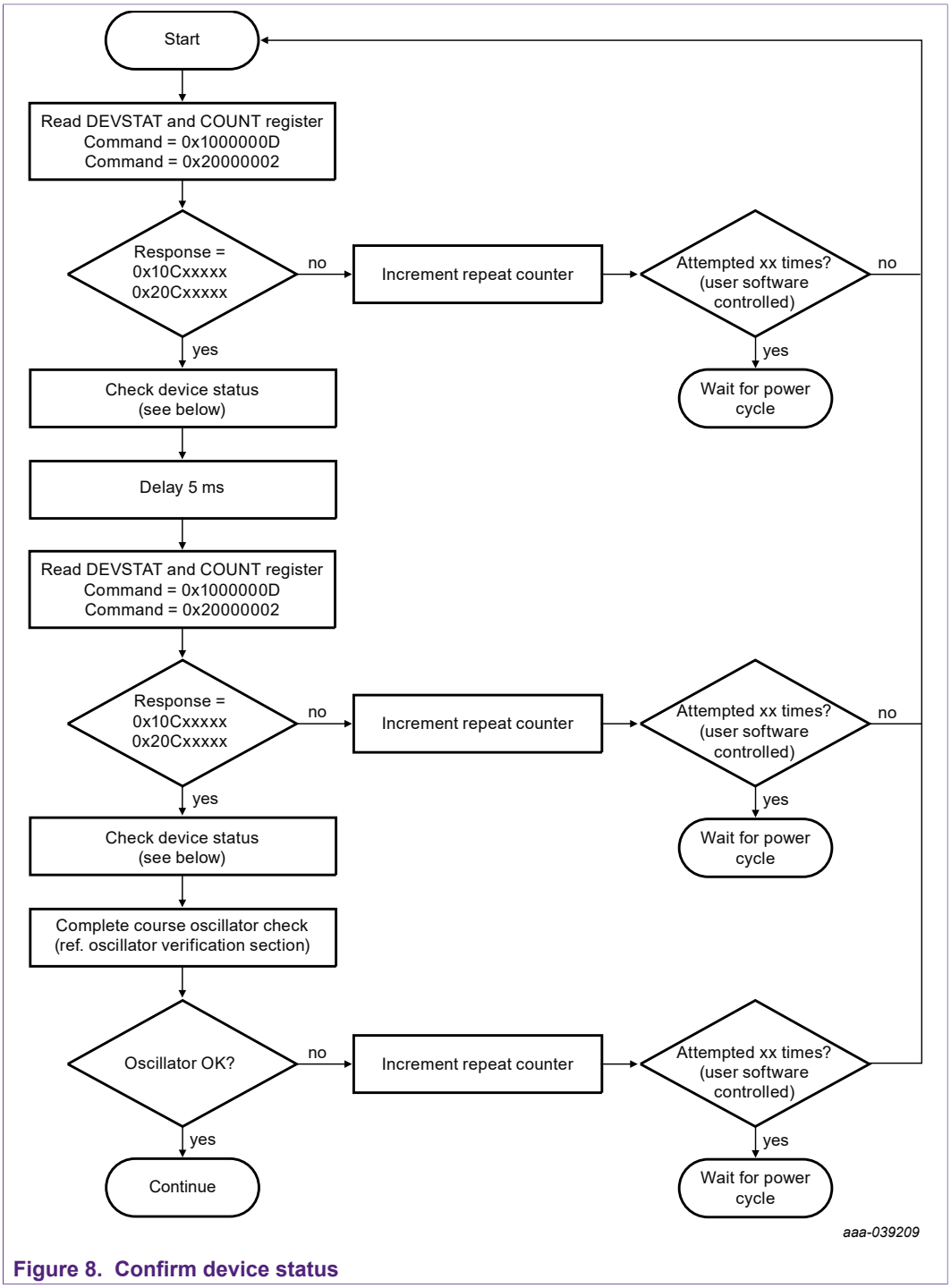

Figure 8. Confirm device status

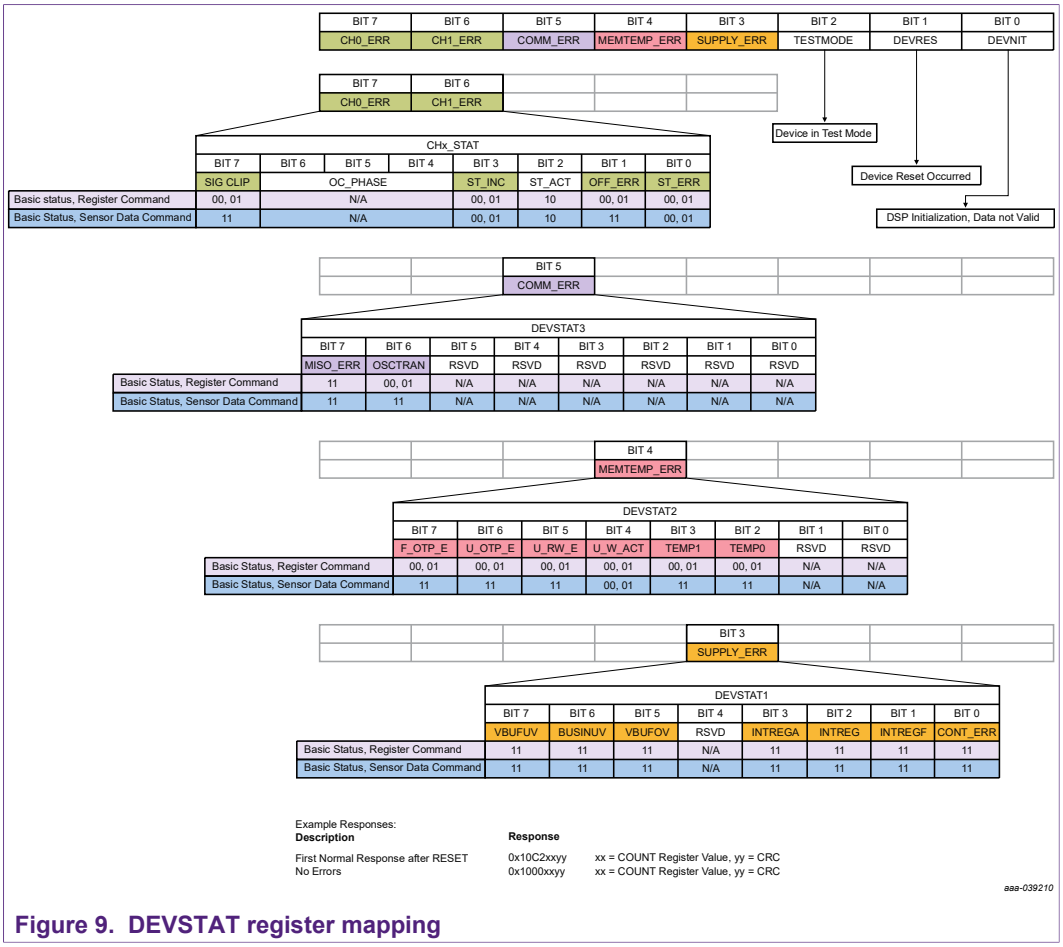

Figure 9. DEVSTAT register mapping

10.2 Optional complete register pattern write verification

The next step is to complete a register pattern write verification. This step is optional and not required to meet the diagnostic coverage as documented in the FMEDA.

The recommended procedure for register pattern write verification is shown in Figure 10. In this example, the PDCM_RSPST0_L register is used for pattern writing. Other registers can be used as long as the function for the register being written to is considered.

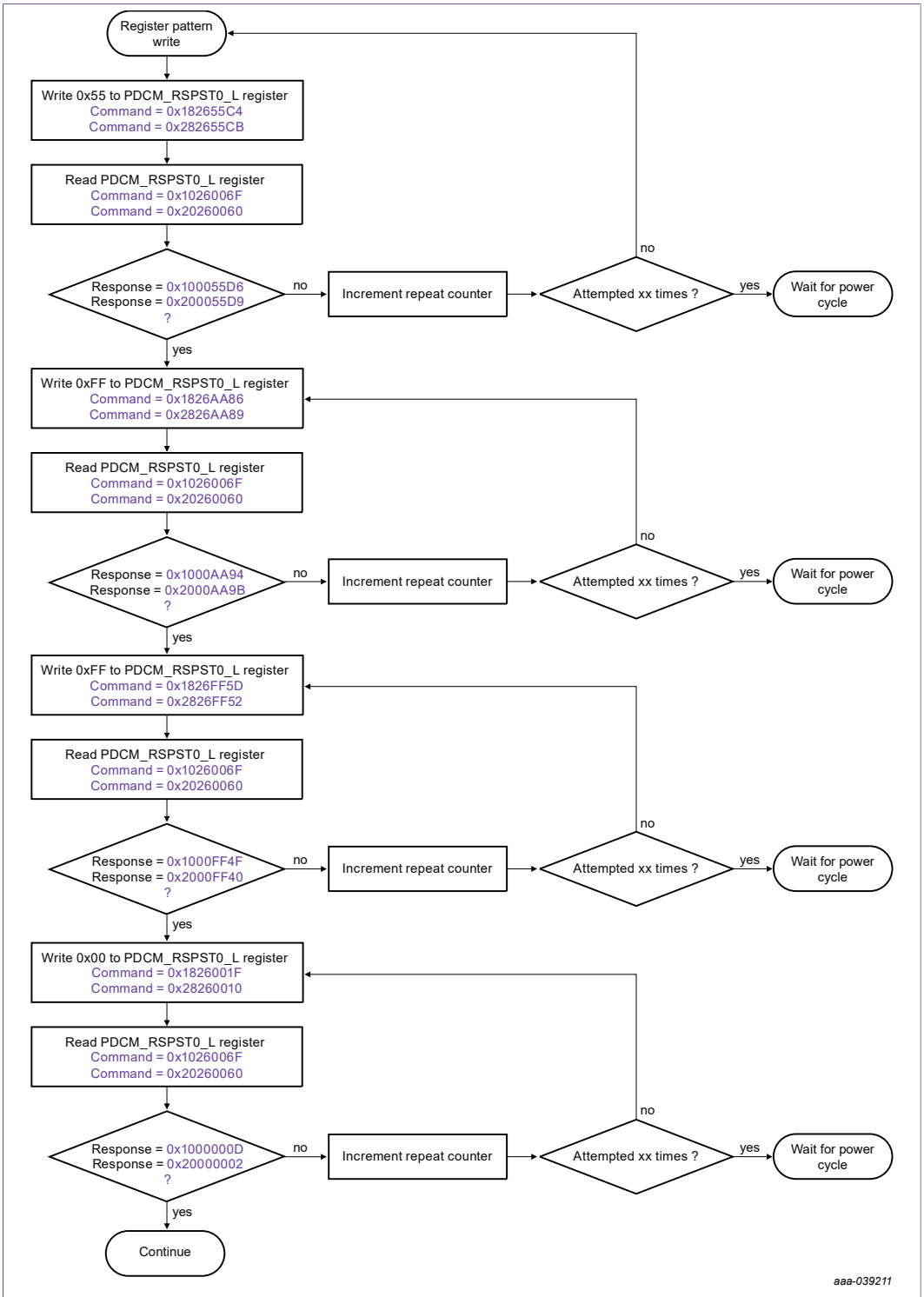

Figure 10. Complete register pattern write verification

10.3 Configure the data sources

The next step is to configure the devices for the desired data sources and source identifiers for Periodic Data Collection Mode (PDCM). Figure 11 shows one example configuration for a 2 slave bus with two data sources for each slave.

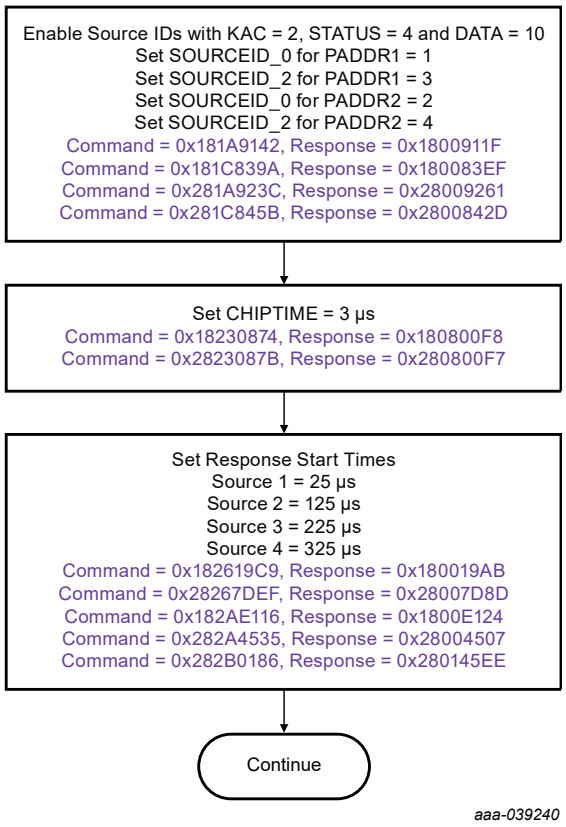

Figure 11. Configure the data sources

Each channel of the FXLS9xxxx devices has the capability for two independently configurable data sources. Figure 12 shows a pictorial mapping of the sources to their Source Identifiers and associated data.

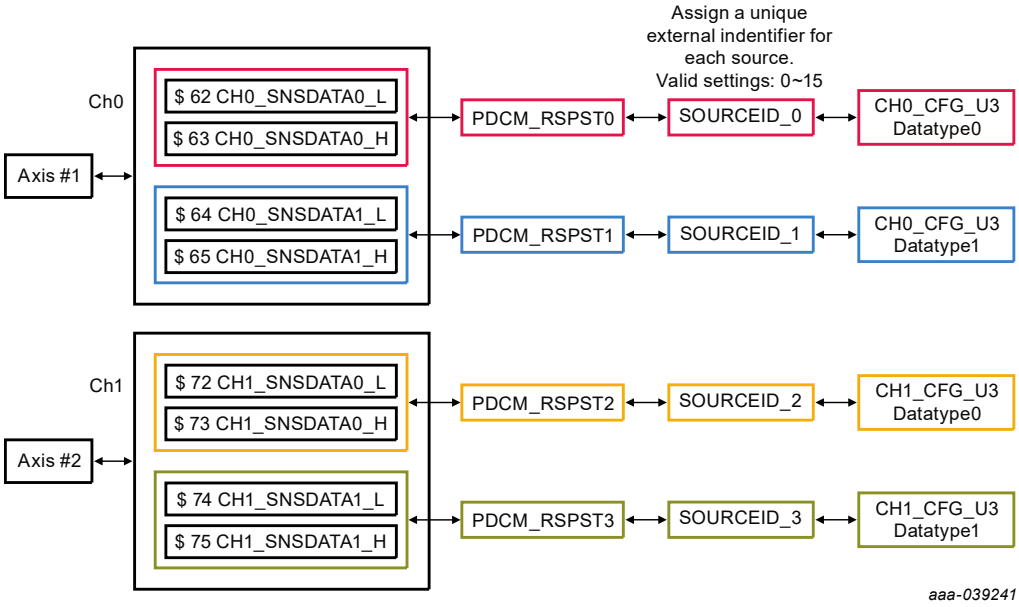

Figure 12. Data source mapping diagram

The sources are enabled and the associated Source Identifiers are set using the registers listed in the table below.

Table 7. Source identifier registers

Register address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
$1A	SOURCEID_0	SID0_EN Enable Channel 0 Source 0, Datatype 0	PDCM_FORMAT[2:0] In this application note, the PDCM format is set to a 28-bit length: • D[27:24] = Source ID • D[23:22] = Source Counter • D[21:18] = 4-Bit Device Status • D[17:08] = 10-Bit Sensor Data • D[07:00] = CRC			SOURCEID_0[3:0] System level source identifier for Channel 0, Datatype 0 Notes: • Each source identifier value for the device must be unique or the device will transmit error messages for the repeated identifier. • For SPI mode, valid source ids are 0x0 to 0x7. No SPI sensor data requests are implemented for 0x8 to 0xF.			
$1B	SOURCEID_1	SID1_EN Enable Channel 0 Source 1, Datatype 1	Reserved	Reserved	Reserved	SOURCEID_1[3:0] System level source identifier for Channel 0, Datatype 1 Notes: • Each source identifier value for the device must be unique or the device will transmit error messages for the repeated identifier. • For SPI mode, valid source ids are 0x0 to 0x7. No SPI sensor data requests are implemented for 0x8 to 0xF.			

Register address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
$1C	SOURCEID_2	SID2_EN Enable Channel 1 Source 2, Datatype 0	Reserved	Reserved	Reserved	SOURCEID_2[3:0] System level source identifier for Channel 1, Datatype 0 Notes: • Each source identifier value for the device must be unique or the device will transmit error messages for the repeated identifier. • For SPI mode, valid source ids are 0x0 to 0x7. No SPI sensor data requests are implemented for 0x8 to 0xF.			
$1D	SOURCEID_3	SID3_EN Enable Channel 1 Source 3, Datatype 1	Reserved	Reserved	Reserved	SOURCEID_3[3:0] System level source identifier for Channel 1, Datatype 1 Notes: • Each source identifier value for the device must be unique or the device will transmit error messages for the repeated identifier. • For SPI mode, valid source ids are 0x0 to 0x7. No SPI sensor data requests are implemented for 0x8 to 0xF.			

10.4 Configure the sensor signal chain

The next step is to configure the sensor signal chain. Figure 13 shows an example configuration. The self-test verification calculations are specific to the configuration selected and must be adjusted if other gains are used.

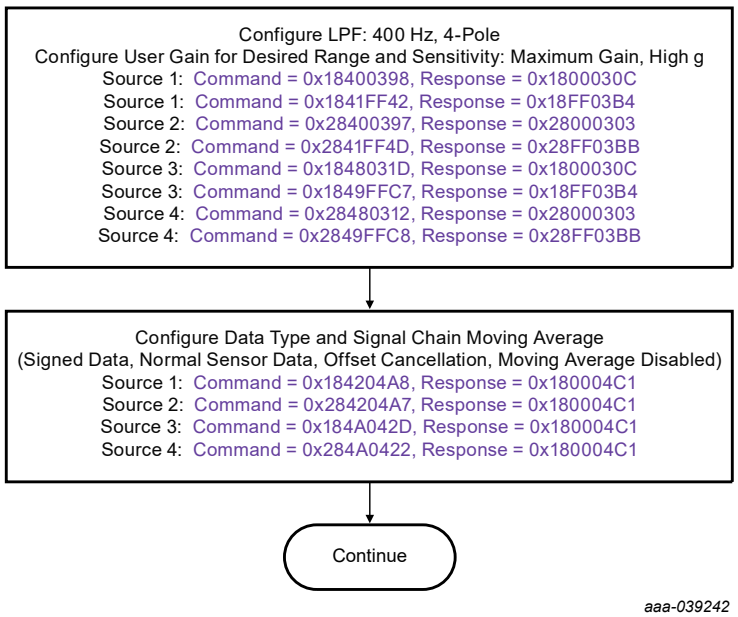

Figure 13. Configure the sensor signal chain

10.4.1 Signal chain low pass filter selection

The signal chain low pass filter is selected by a combination of the LPF bits and the SAMPLERATE bits in the CHx_CFG_U1 register as shown in the datasheet. The LPF selection table is shown in Table 8.

Table 8. Low pass filter selection

LPF[3]	LPF[2]	LPF[1]	LPF[0]	Low pass filter type		
				SAMPLERATE = 00, 01	SAMPLERATE = 10	SAMPLERATE = 11
				16 µs	32 µs	64 µs
0	0	0	0	400 Hz, 4-Pole	200 Hz, 4-Pole	100 Hz, 4-Pole
0	0	0	1	400 Hz, 3-Pole	200 Hz, 3-Pole	100 Hz, 3-Pole
0	0	1	0	400 Hz, 4-Pole	200 Hz, 4-Pole	100 Hz, 4-Pole
0	0	1	1	400Hz, 3-Pole	200 Hz, 3-Pole	100 Hz, 3-Pole
0	1	0	0	325 Hz, 3-Pole	162.5 Hz, 3-Pole	81.25 Hz, 3-Pole
0	1	0	1	370 Hz, 2-Pole	185 Hz, 2-Pole	92.5 Hz, 2-Pole
0	1	1	0	180 Hz, 2-Pole	90 Hz, 2-Pole	45 Hz, 2-Pole
0	1	1	1	100 Hz, 2-pole	50 Hz, 2-Pole	25 Hz, 2-Pole
1	0	0	0	1500 Hz, 4-Pole	750 Hz, 4-Pole	375 Hz, 4-Pole
1	0	0	1	500 Hz, 3-Pole	250 Hz, 3-Pole	125 Hz, 3-pole
1	0	1	0	800 Hz, 4-Pole	400 Hz, 4-Pole	200 Hz, 4-Pole
1	0	1	1	1200 Hz, 4-Pole	600 Hz, 4-Pole	300 Hz, 4-Pole
1	1	0	0	120 Hz, 3-Pole	60 Hz, 3-Pole	30 Hz, 3-Pole
1	1	0	1	20 kHz, 2-Pole	10 kHz, 2-Pole	5 kHz, 2-Pole
1	1	1	0	120 Hz, 2-Pole	60 Hz, 2-Pole	30 Hz, 2-Pole
1	1	1	1	50 Hz, 4-Pole	25 Hz, 4-Pole	12.5 Hz, 4-Pole

10.4.2 Signal chain data type configuration

Each source enabled (as described in Section 10.3 "Configure the data sources") must have its data type configured. Datatype configuration is described in the datasheet. A simplified table is included below:

Table 9. Data type configuration

CHx DATATYPEx[1:0]		Sensor Data Description
0	0	Offset Cancelled Data as Configured by the OC_FILT bits
0	1	Raw Data (No Offset Cancellation)
1	0	Temperature Sensor Data
1	1	Temperature Sensor Data

10.5 Optional read and record stored self-test data

The next step is to read and record the self-test data stored in the device during device manufacturing. Reading this data is only necessary if the optional self-test accuracy verification test is used. The self-test accuracy verification test can be run at each power up as documented here, or one time only during system manufacturing. See Section 10.7 "Complete self-test (self-test overview)" and the associated sub-sections for details on how to use the stored self-test data for additional self-test accuracy.

Figure 14 shows the procedure for reading the stored self-test data.

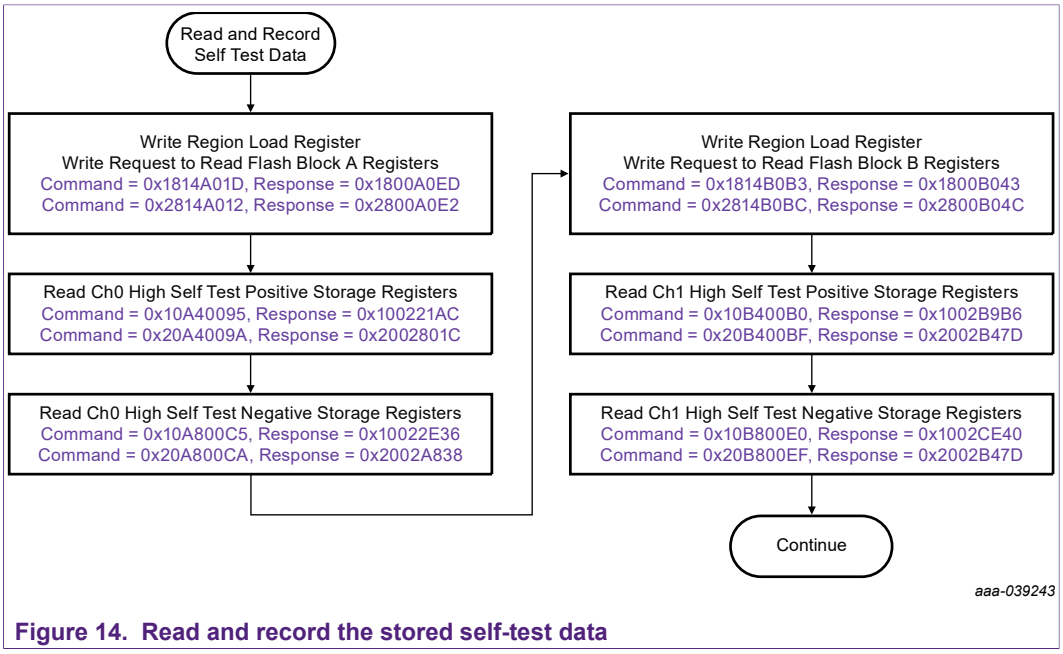

Figure 14. Read and record the stored self-test data

10.6 Confirm traceability information

The next step is to confirm the device level traceability information. The IC type, IC manufacturer ID, IC Part Number and IC Serial Number should be read to confirm that the proper device is connected.

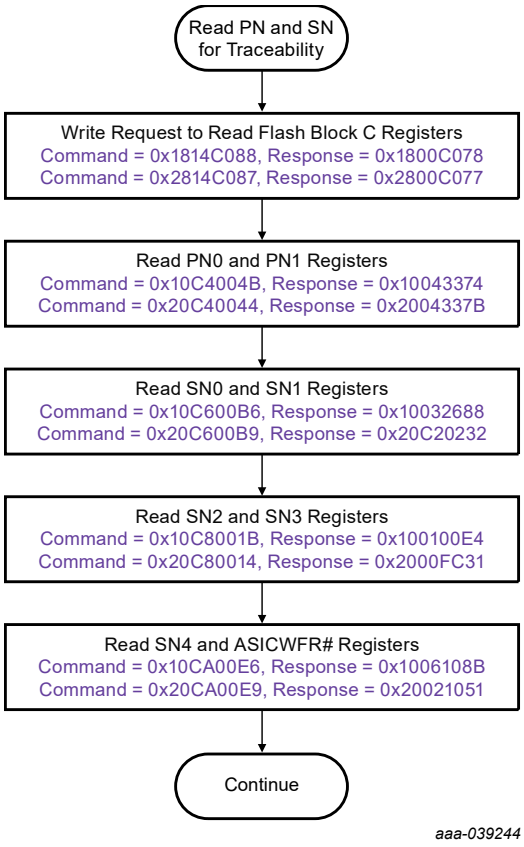

Figure 15. Confirm device traceability information

10.7 Complete self-test (self-test overview)

The next step is to complete the some or all of the various self-test functions available in the device. Figure 16 shows an overview of an example recommended procedure for completing self-test. Test repeats on failure are not shown in the diagrams. The number or test repeats for each test type are determined by the user based on the application. Typically test repeats are included at a minimum for the analog self-test procedures to provide immunity to potential misuse inputs that are common during startup.

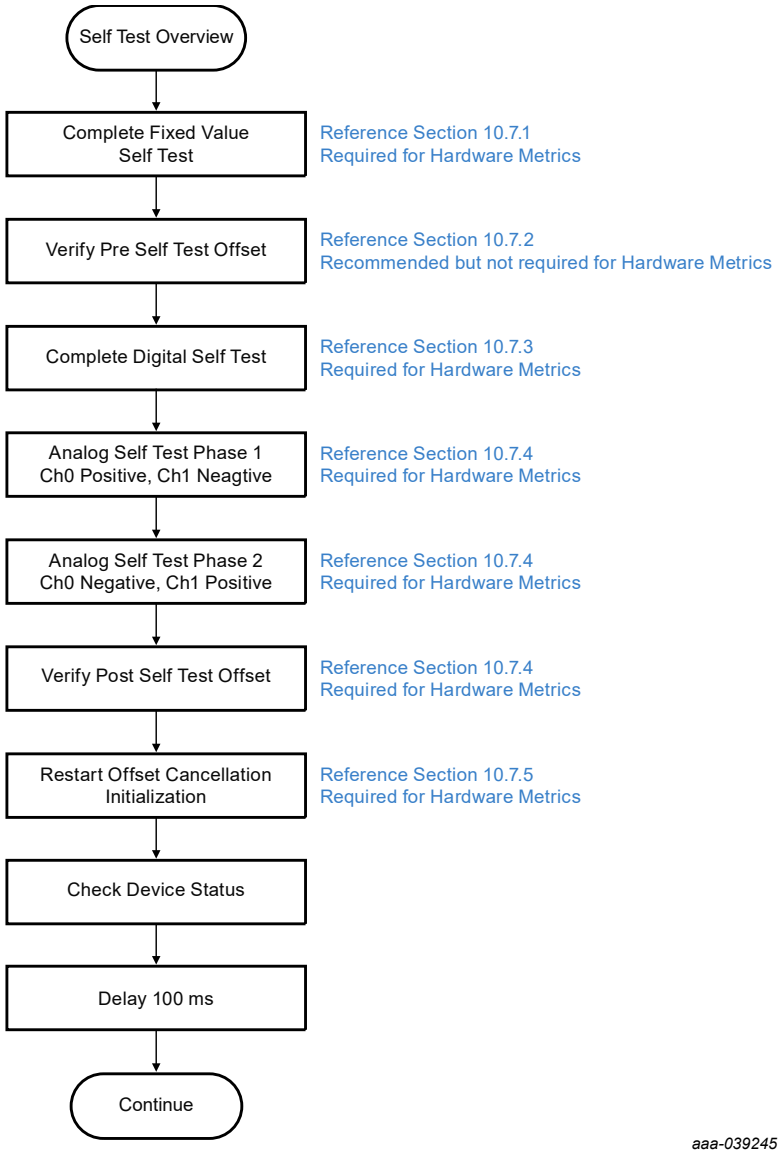

Figure 16. Self-test overview

10.7.1 Complete fixed value self-test

The next step is to complete a fixed value self-test verification for each device. The purpose of the fixed value self-test is to confirm that the output data register and communication block have no stuck bit conditions. Figure 17 shows an example procedure for completing self-test with two fixed values. The example alternates 0x5555 and 0xAAAA by channel to confirm both states of each bit in the data field and to maximize verification of channel independent data. Expected responses are included for each self-test request.

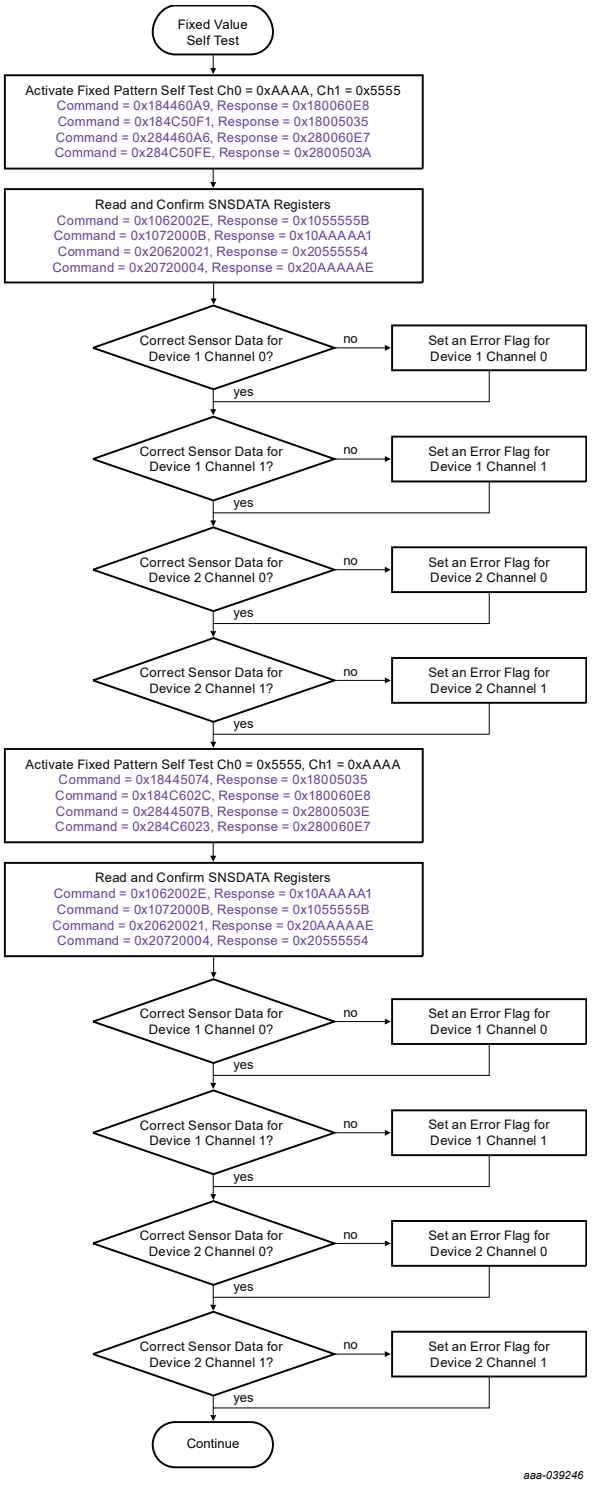

Figure 17. Complete fixed value self-test

10.7.2 Complete pre-self-test offset

The next step is to complete an offset verification. The purpose of the offset verification is to capture the pre-self-test offset that will be subtracted from the measured self-test values during analog self-test.

Figure 18 shows an example procedure for capturing the sensor offset.

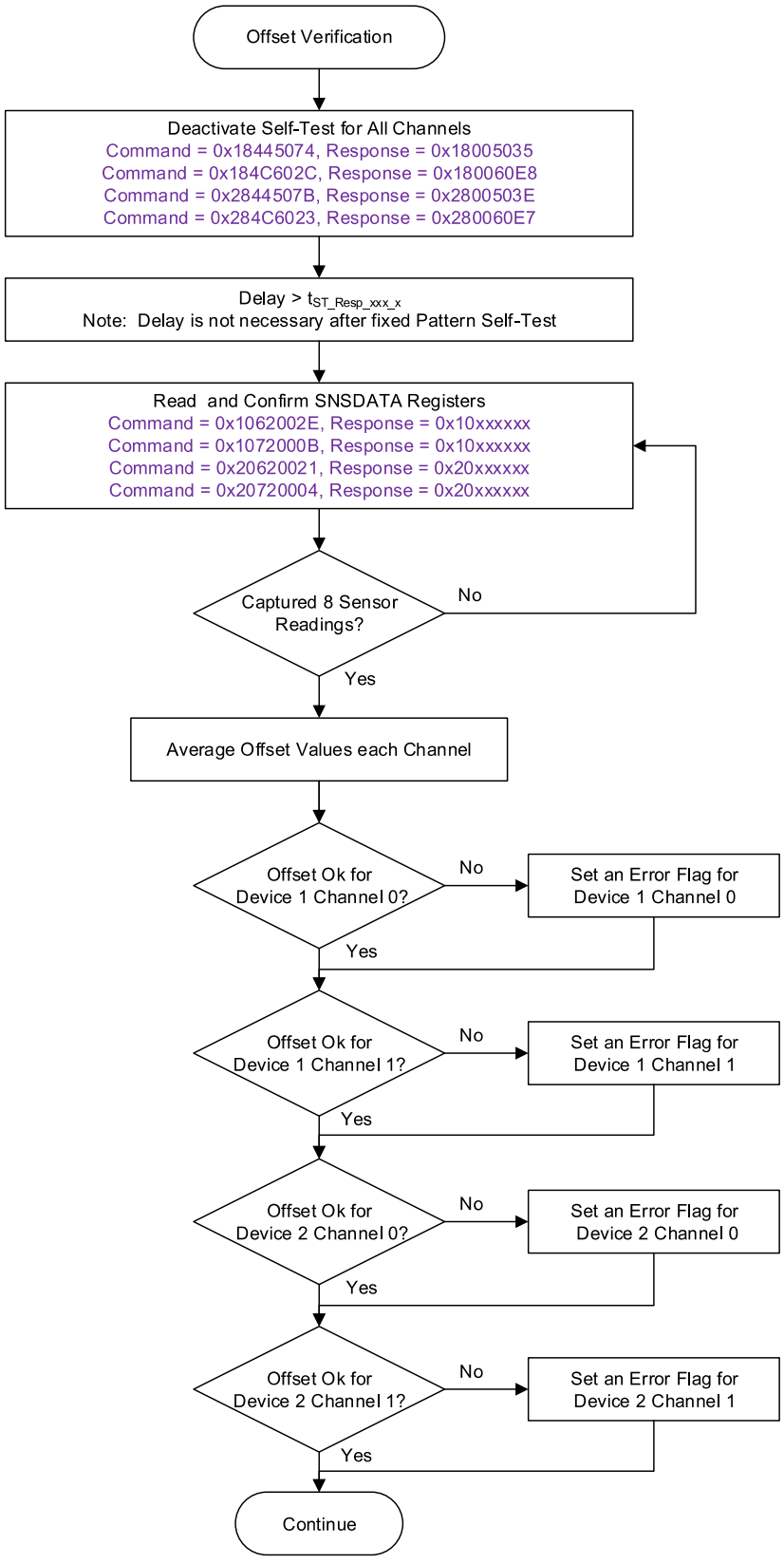

Figure 18. Pre-Self-Test Offset

10.7.3 Complete digital self-test

The next step is to complete a digital self-test verification for each device. The purpose of the digital self-test is to complete a more accurate verification of the digital signal chain. The digital self-test forces a known value into the input of the digital signal chain. After a defined interval of time, dependent on the low pass filter selected, the signal chain output can be verified against an expected value plus or minus a small tolerance. Figure 19 shows an example procedure for completing a self-test of one digital value (Digital Self-Test 0xF) and confirming the expected output value.

If offset cancellation is being used, bypass the offset cancellation filter for digital self-test to eliminate the effects of the filter on the digital self-test result. The procedure below includes offset cancellation bypass during digital self-test.

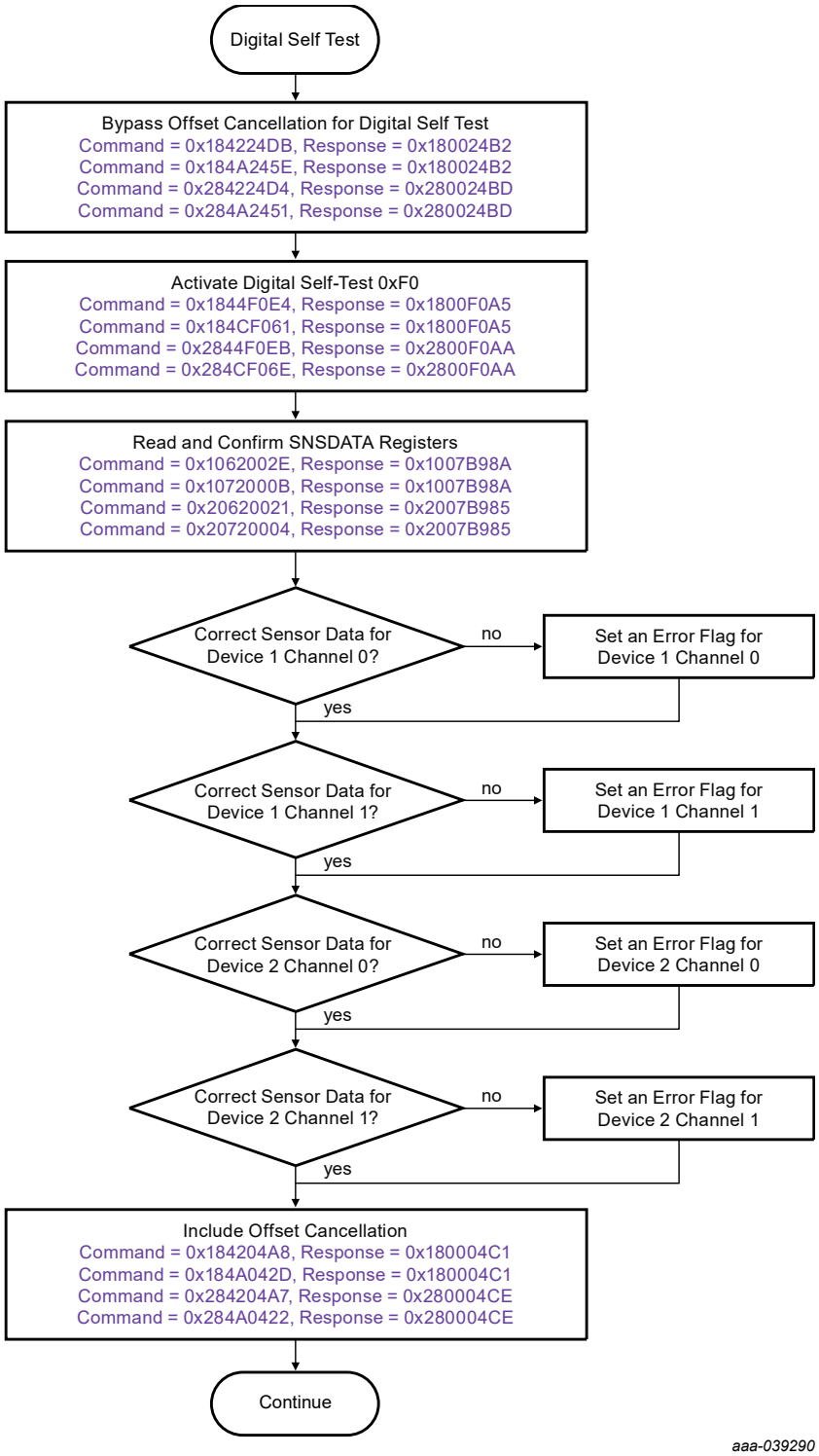

Figure 19. Complete digital self-test

10.7.3.1 Digital self-test limit calculation

The digital self-test provides a constant value to the sensor data output regardless of the user gain settings. The limits for the minimum gain setting are listed in the datasheet and included in the table in Table 10 below.

Table 10. Data sheet digital self-test values with minimum gain

Digital Self-Test Expected Values									
Self-Test ST_CTRL[3:0]	Expected Value CHx_SNSDATAx Register Read (Signed HEX)			Expected Value CHx_SNSDATAx Register Read (Unsigned HEX)			Expected Value CHx_SNSDATAx Register Read (Decimal)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
0xC	E77F	E780	E781	677F	6780	6781	-6273	-6272	-6271
0xD	0FA3	0FA4	0FA5	8FA3	8FA4	8FA5	4003	4004	4005
0xE	EFA2	EFA3	EFA4	6FA2	6FA3	6FA4	-4190	-4189	-4188
0xF	07B7	07B8	07B9	87B7	87B8	87B9	1975	1976	1977

10.7.4 Restart offset cancellation fast startup

Once Self-test is complete, if offset cancellation is enabled, the offset cancellation fast startup is reset to re-zero the offset cancellation. Figure 20 shows the procedure for restarting the fast offset cancellation.

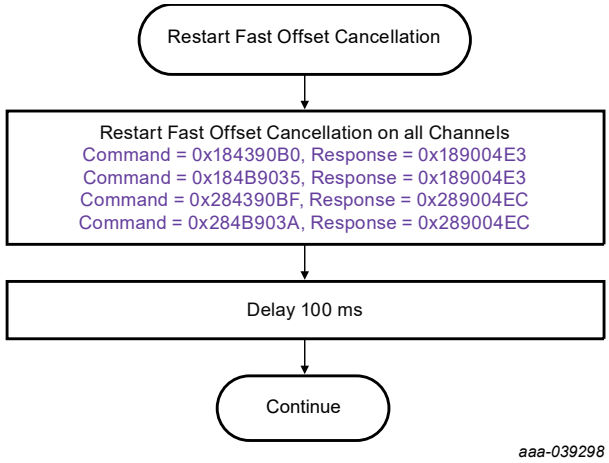

Figure 20. Restart offset cancellation fast startup

10.7.4.1 Verify offset

After the offset cancellation startup delay, the raw and / or offset cancelled offset data is verified using the procedure in Figure 21.

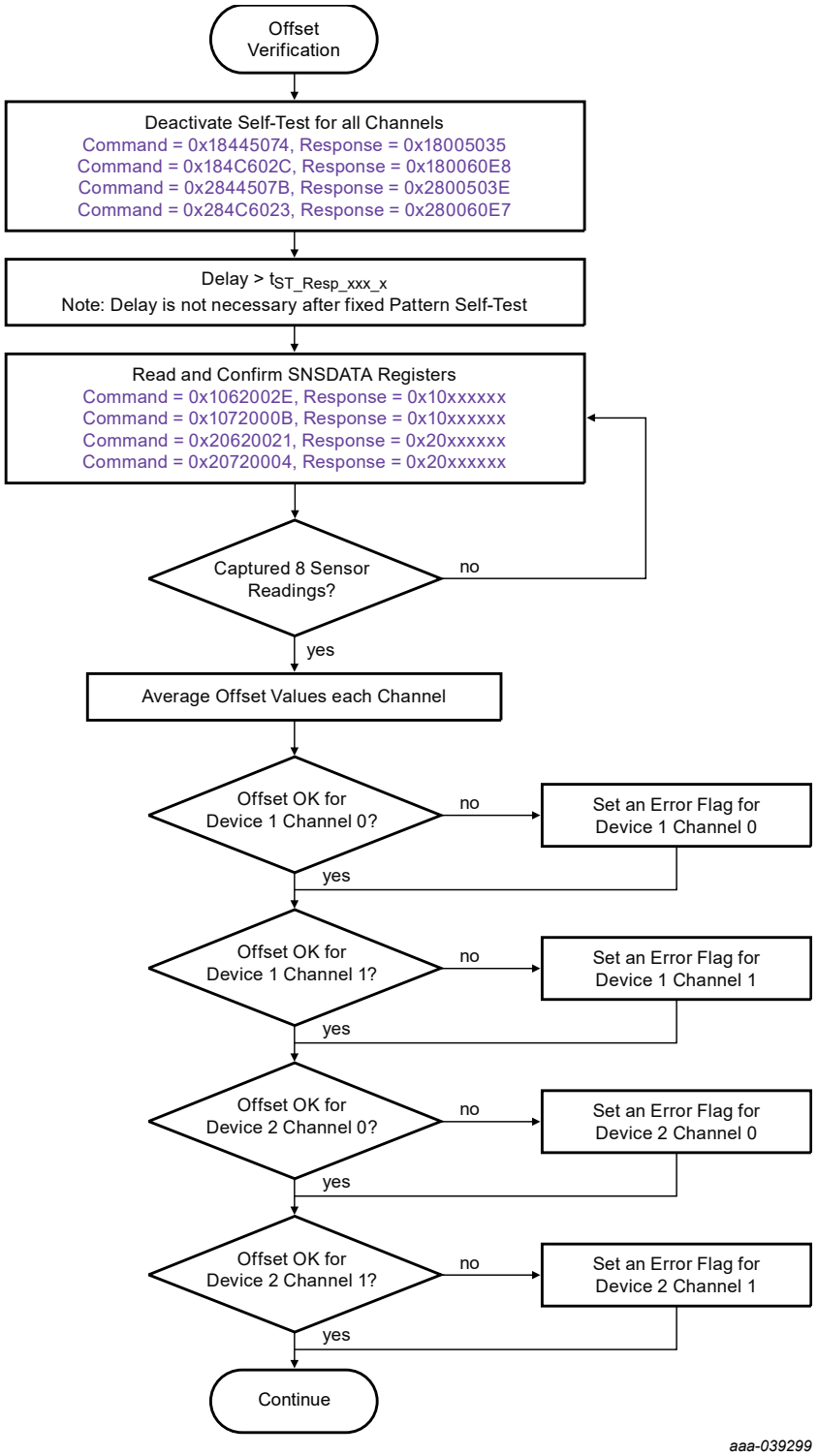

Figure 21. Post restart offset cancellation offset

10.7.4.2 Standard offset verification

The average offset calculated from each data source captured from the test in Figure 21 is compared against the offset limits in the datasheet. If offset cancellation (high pass filter) is not used and a lower range is programmed than the range condition specified for offset (25 g for medium g, 100g for high g), the offset limits must be scaled with the user gain. Table 11 and Table 12 show some example offset test limits for different ranges and settings.

Offset verification in this procedure is included as part of the initialization procedure. If it is more convenient for the user, offset verification can be completed after entering Periodic Data Collection Mode (PDCM).

Table 11. Standard offset verification test limits, medium g

Offset Cancellation Enabled?	User Programmed Range Medium g (g)	Minimum Limit (LSB, 12-Bit)	Maximum Limit (LSB, 12-Bit)	Pass Fail Criteria
Yes	All	-1	+1	Min Limit ≤ Result ≤ Max Limit
No	15.5	-162	+162	
No	16.0	-157	+157	
No	20.0	-126	+126	
No	25.0	-100	+100	
No	35.0	-72	+72	
No	50.0	-50	+50	
No	60.0	-42	+42	
No	62.0	-41	+41	
No	62.5	-41	+41	
No	75.0	-34	+34	
No	85.3	-30	+30	
No	100.0	-25	+25	
No	105.0	-24	+24	
No	112.5	-23	+23	
No	125.0	-21	+21	
No	128.0	-20	+20	
No	150.0	-17	+17	

Table 12. Standard offset verification test limits, high g

Offset Cancellation Enabled?	User Programmed Range High g (g)	Minimum Limit (LSB, 12-Bit)	Maximum Limit (LSB, 12-Bit)	Pass Fail Criteria
Yes	All	-1	+1	Min Limit ≤ Result ≤ Max Limit
No	50.0	-200	+200	
No	60.0	-167	+167	
No	62.0	-162	+162	
No	62.5	-160	+160	
No	100.0	-100	+100	
No	105.0	-96	+96	
No	112.5	-89	+89	
No	125.0	-80	+80	
No	128.0	-79	+79	
No	150.0	-67	+67	
No	187.0	-54	+54	
No	250.0	-40	+40	
No	312.5	-32	+32	
No	375.0	-27	+27	
No	500.0	-20	+20	
No	748.0	-14	+14	

10.8 Complete analog self-test

The next step is to complete analog self-test verification. The purpose of the analog self-test is to:

1. Confirm unimpeded motion of the proof mass in both the positive and negative acceleration directions.
2. Verify the sensitivity accuracy of the device. The FXLS9xxxx devices contain multiple self-test capabilities and procedures that have different sensitivity accuracy verification capabilities.

The flow charts below show an example analog self-test procedure for measuring both positive and negative self-test. Section 10.8.1 "Analog self-test pass fail limits" explains the pass/fail criteria for analog self-test. Analog Self-Test can be affected by external acceleration miss-use events like a door slam. This application note does not cover methods to address immunity to miss-use events. A typical method to increase analog self-test immunity to miss-use events is to repeat the self-test procedure multiple times as shown in the high-level self-test flow chart. On failure, the entire self-test procedure can be repeated, or only the failing self-test phase can be repeated.

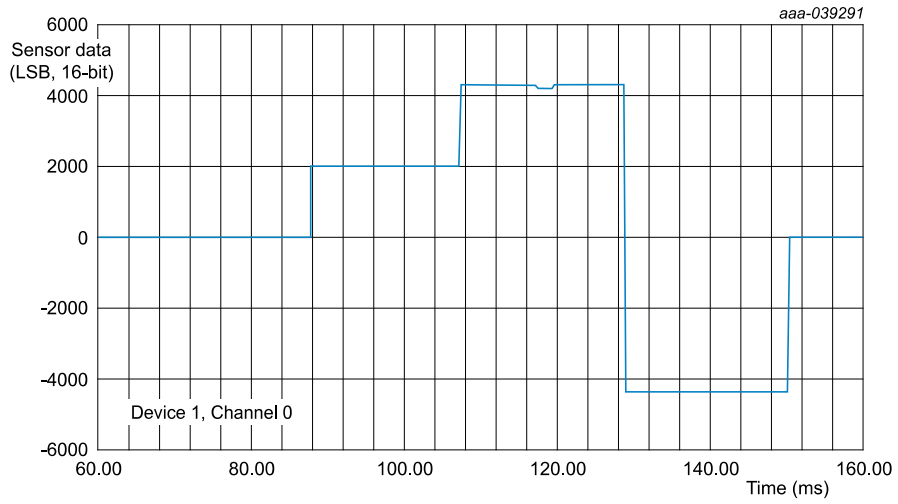

Figure 22. Example analog self-test response, Device 1, Channel 0

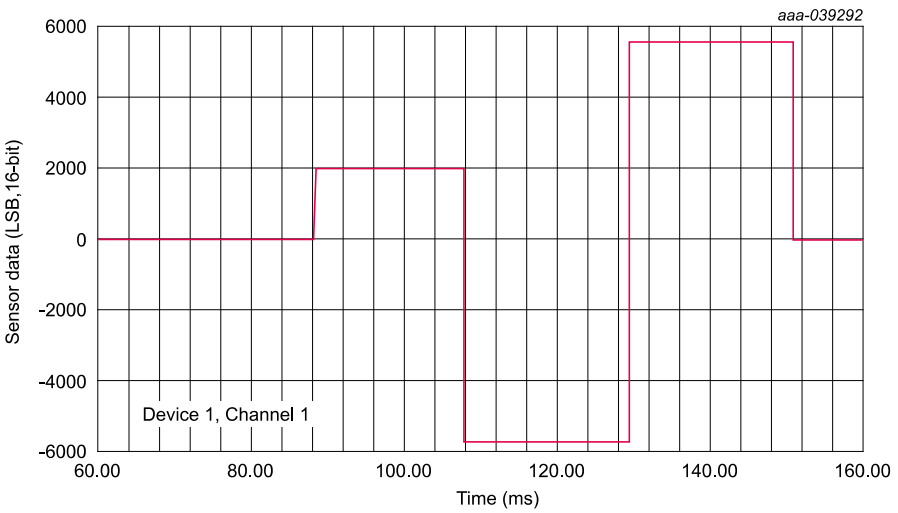

Figure 23. Example analog self-test response, Device 1, Channel 1

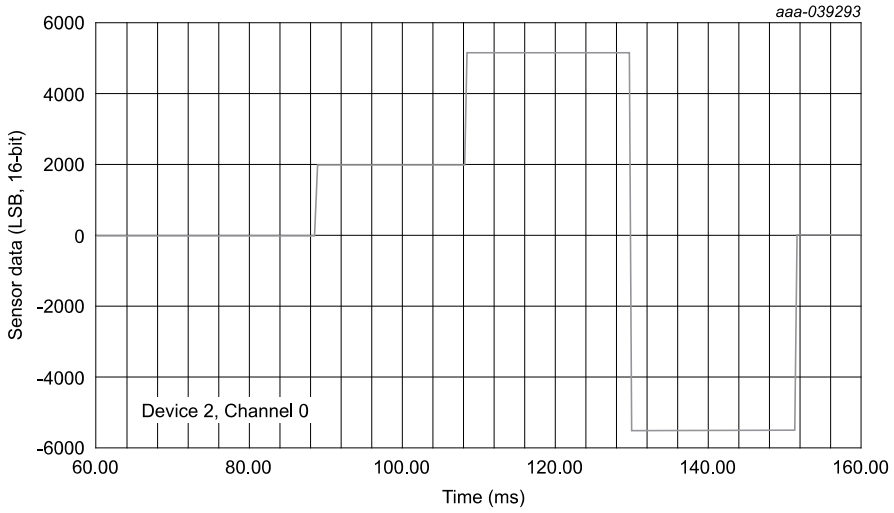

Figure 24. Example analog self-test response, Device 2, Channel 0

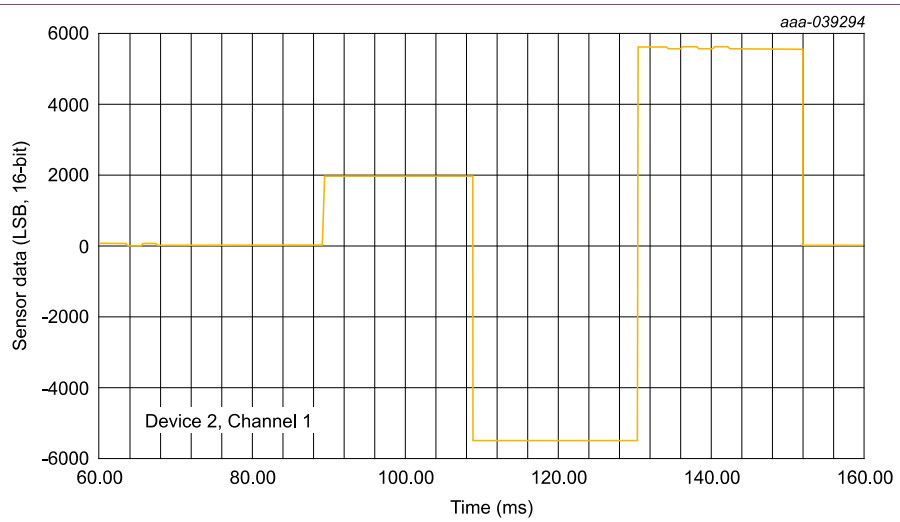

Figure 25. Example analog self-test response, Device 2, Channel 1

Table 13. Analog self-test statistics

Parameter	Device 1		Device 2		Units
	Channel 0	Channel 1	Channel 0	Channel 1	
Part Number	0433	—	0433	—	Hex
Serial Number	1001000326	—	1000FCC202	—	Hex
Device Status	02	—	02	—	Hex
Channel Status	40	40	40	40	Hex
Channel Gain	3.9922	3.9922	3.9922	3.9922	NA
Sensitivity	87.4010	87.4010	87.4010	87.4010	LSB/g, 16-bit
Device Range	46.8530	46.8530	46.8530	46.8530	g
Stored Self-test Value (+)	1090	1394	1280	1384	LSB, 16-Bit, Unity Gain
Stored Self-test Value (-)	-1116	-1430	-1360	-1384	LSB, 16-Bit, Unity Gain
Pre-Self-Test OC Output	-8.38	60.50	8.88	95.32	LSB, 16-bit
Post-Self-Test OC Output	-6.29	53.67	11.29	78.95	LSB, 16-bit
Post Reset OC Ouput	-0.25	0.68	0.45	1.54	LSB, 16-bit
Normal Mode OC Output	-2.68	-3.57	-4.70	-3.70	LSB, 16-bit
Fixed Pattern Self-Test 1	5555	aaaa	5555	aaaa	HEX, 16-Bit
Fixed Pattern Self-Test 2	aaaa	5555	aaaa	5555	HEX, 16-Bit
Digital Self-Test	1977	1977	1977	1977	Decimal, 16-Bit
Digital Self-Test	07b9	07b9	07b9	07b9	HEX, 16-Bit
Analog Self-Test (+)	4348.78	5649.56	5147.44	5642.56	LSB, 16-Bit
Analog Self-Test (+) Gain Adj	1089.32	1415.15	1289.38	1413.40	LSB, 16-Bit
Analog Self-Test (-)	-4467.11	-5675.22	-5435.22	-5457.89	LSB, 16-Bit
Analog Self-Test (-) Gain Adj	-1118.96	-1421.58	-1361.46	-1367.14	LSB, 16-Bit
Delta from Stored ST (+)	-0.06%	1.52%	0.73%	2.12%	%
Delta from Stored ST (-)	0.27%	-0.59%	0.11%	-1.22%	%

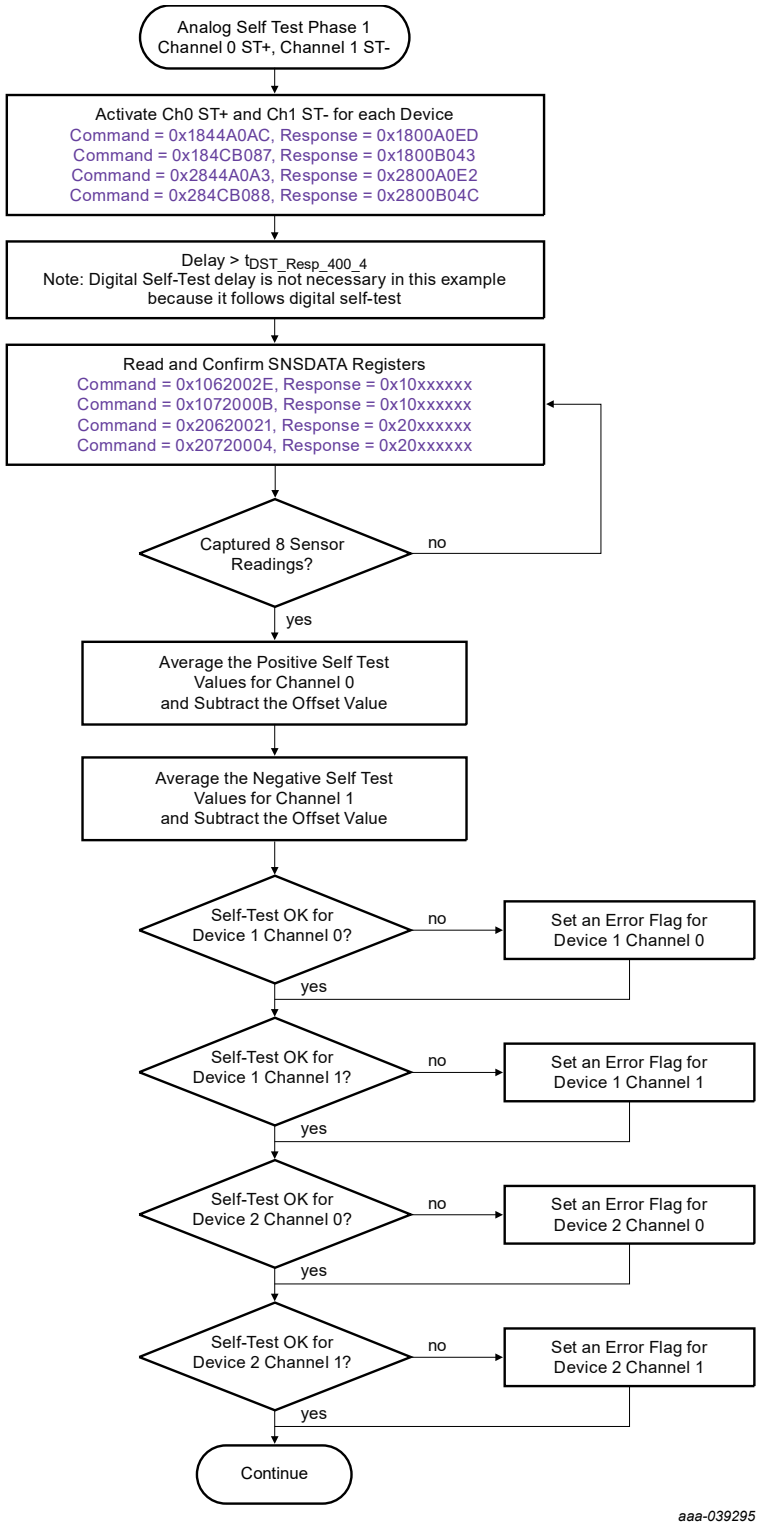

Figure 26. Channel 0 positive self-test, Channel 1 negative self-test

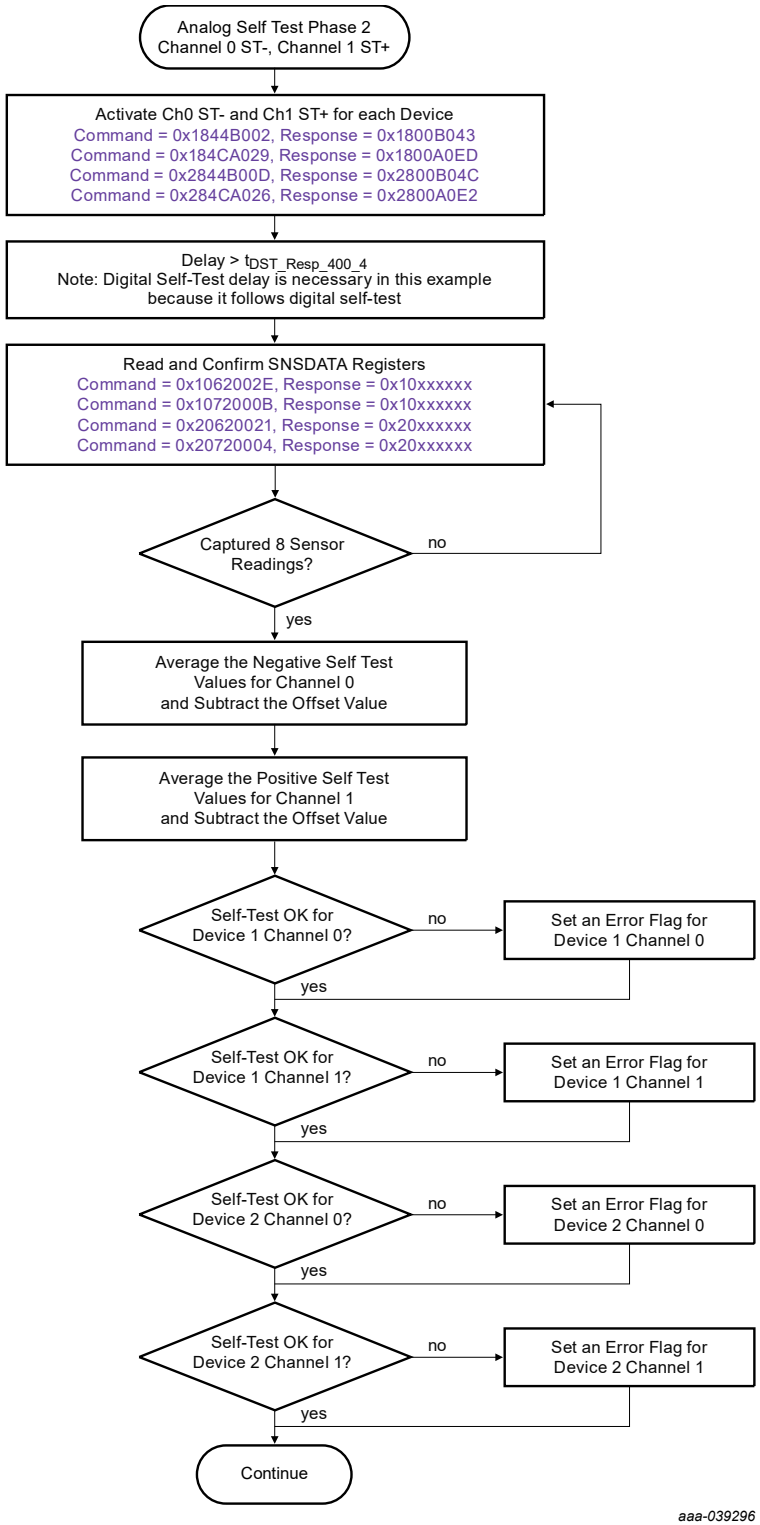

Figure 27. Channel 0 negative self-test, Channel 1 positive self-test

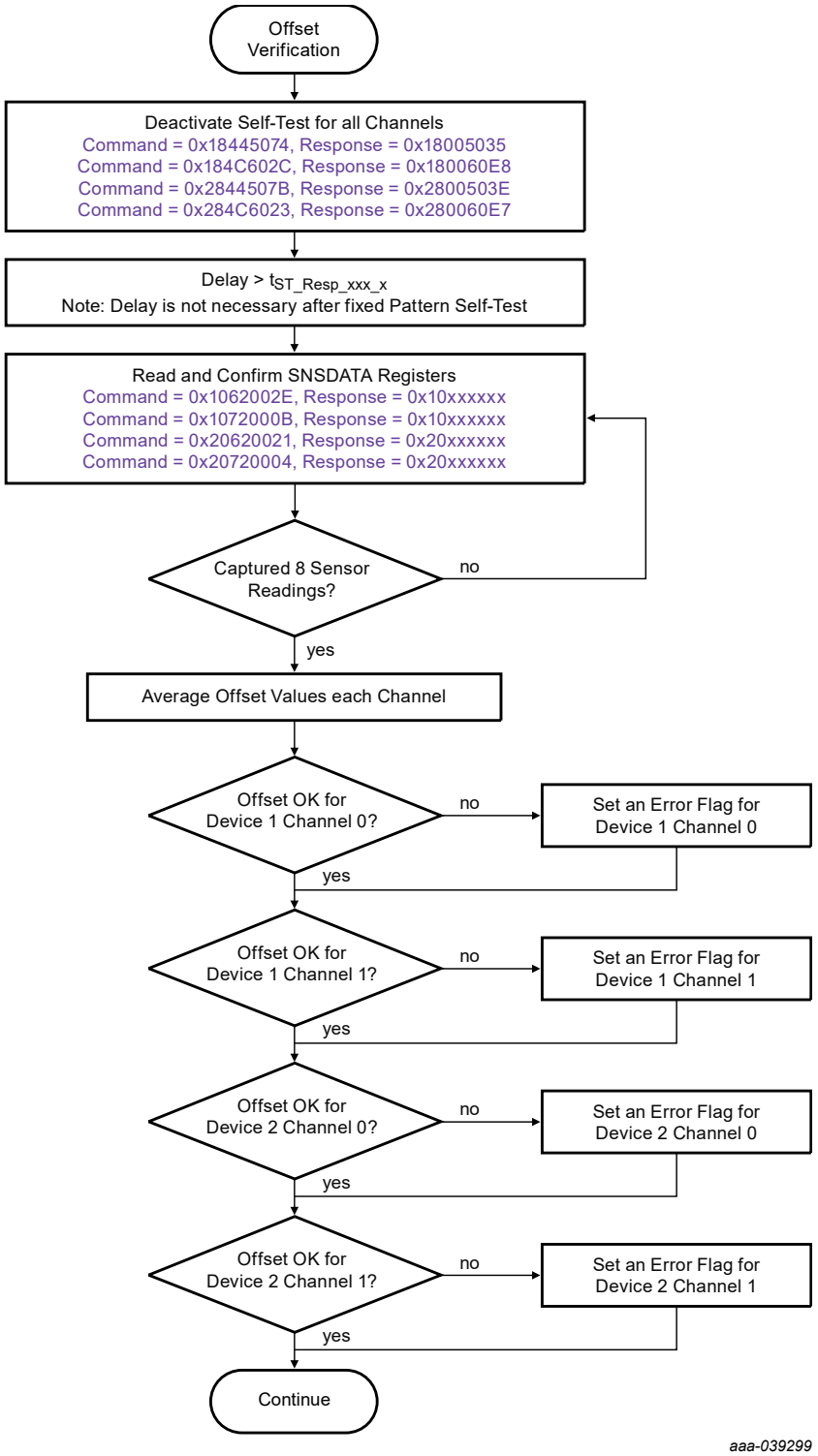

Figure 28. Post self-test offset

10.8.1 Analog self-test pass fail limits

Several methods can be used to evaluate the analog self-test results. This section covers the various methods for evaluating the offset and self-test results to improve diagnostic

coverage. The tests described in Section 10.8.1.1 "Standard self-test verification" are required to meet the diagnostic coverage as documented in the FMEDA. The additional tests improve diagnostic coverage.

10.8.1.1 Standard self-test verification

The resulting positive and negative self-test values from the tests in Figure 26 through Figure 28 are compared against the self-test limits in the datasheet. The self-test limits must be scaled with the user gain. The equation used to convert the specified self-test in g to minimum and maximum self-test limits is shown below. Table 14 through Table 17 shows some example self-test limits for different ranges and settings.

$$AnalogSelfTest_{Min@UserGain} = Truncate\left[ST_{HH\_187X\_13min} * (UserGain)\right]$$

$$AnalogSelfTest_{Max@UserGain} = RoundUp\left[ST_{HH\_187X\_13max} * (UserGain)\right]$$

Where:

- $AnalogSelfTest_{Min@UserGain}$ = The SNSDATAx register analog self-test minimum limit for the configured user gain
- $AnalogSelfTest_{Max@UserGain}$ = The SNSDATAx register analog self-test maximum limit for the configured user gain
- $ST_{HH\_187X\_13min}$ = The min med g SNSDATAx register self-test delta from offset for a user gain of 1
- $ST_{HH\_187X\_13max}$ = The max med g SNSDATAx register self-test delta from offset for a user gain of 1
- *UserGain* = The configured gain, calculated as shown in Section 11 "Signal chain user gain selection"

Table 14. Standard self-test verification test limits, medium g X-axis

Device Type	NXP Trim Value (LSB/g)	User Programmed Range (g)	User Programmed Gain	Self-Test Limits, SNSDATA Register Value (LSB)		Pass Fail Criteria
				Minimum	Maximum	
Medium g X	33.0161	15.5	3.9922	7038	16428	Min Limit ≤ Result ≤ Max Limit
		16.0	3.8750	6831	15946	
		20.0	3.1016	5468	12763	
		25.0	2.4766	4366	10192	
		35.0	1.7695	3119	7282	
		50.0	1.2383	2183	5096	
		60.0	1.0352	1824	4260	
		62.0	1.0000	1763	4115	
		62.5	0.9922	1749	4083	
		64.0	0.9688	1707	3987	
		75.0	0.8262	1456	3400	
		85.3	0.7266	1280	2990	
		100.0	0.6191	1091	2548	
		105.0	0.5898	1039	2428	
		112.5	0.5508	971	2267	
		125.0	0.4961	874	2042	
		128.0	0.4844	853	1994	
		150.0	0.4131	728	1700	
		248.0	0.2500	440	1029	

Table 15. Standard self-test verification test limits, medium g Z-axis

Device Type	NXP Trim Value (LSB/g)	User Programmed Range (g)	User Programmed Gain	Self-Test Limits, SNSDATA Register Value (LSB)		Pass Fail Criteria
				Minimum	Maximum	
Medium g Z	33.0161	15.5	3.9922	3421	7993	Min Limit ≤ Result ≤ Max Limit
		16.0	3.8750	3320	7758	
		20.0	3.1016	2658	6210	
		25.0	2.4766	2122	4959	
		35.0	1.7695	1516	3543	
		50.0	1.2383	1061	2480	
		60.0	1.0352	887	2073	
		62.0	1.0000	857	2002	
		62.5	0.9922	850	1987	
		64.0	0.9688	830	1940	
		75.0	0.8262	708	1654	
		85.3	0.7266	622	1455	
		100.0	0.6191	530	1240	
		105.0	0.5898	505	1181	
		112.5	0.5508	472	1103	
		125.0	0.4961	425	994	
		128.0	0.4844	415	970	
		150.0	0.4131	354	827	
		248.0	0.2500	214	501	

Table 16. Standard self-test verification test limits, high g X-axis

Device Type	NXP Trim Value (LSB/g)	User Programmed Range (g)	User Programmed Gain	Self-Test Limits, SNSDATA Register Value (LSB)		Pass Fail Criteria
				Minimum	Maximum	
High g X	10.9465	46.875	3.9922	2886	6743	Min Limit ≤ Result ≤ Max Limit
		50	3.7422	2705	6321	
		60	3.1172	2253	5265	
		62	3.0156	2180	5094	
		62.5	2.9922	2163	5054	
		100	1.8711	1352	3161	
		105	1.7813	1287	3009	
		112.5	1.6641	1203	2811	
		125	1.4961	1081	2527	
		128	1.4609	1056	2468	
		150	1.2461	900	2105	
		187	1.0000	723	1689	
		250	0.7480	540	1264	
		312.5	0.5977	432	1010	
		375	0.4990	360	843	
		500	0.3740	270	632	
		748	0.2500	180	423	

Table 17. Standard self-test verification test limits, high g Z-axis

Device Type	NXP Trim Value (LSB/g)	User Programmed Range (g)	User Programmed Gain	Self-Test Limits, SNSDATA Register Value (LSB)		Pass Fail Criteria
				Minimum	Maximum	
High g Z	10.9465	46.875	3.9922	3329	7773	Min Limit ≤ Result ≤ Max Limit
		50	3.7422	3120	7287	
		60	3.1172	2599	6070	
		62	3.0156	2515	5872	
		62.5	2.9922	2495	5826	
		100	1.8711	1560	3644	
		105	1.7813	1485	3469	
		112.5	1.6641	1387	3240	
		125	1.4961	1247	2913	
		128	1.4609	1218	2845	
		150	1.2461	1039	2427	
		187	1.0000	834	1947	
		250	0.7480	623	1457	
		312.5	0.5977	498	1164	
		375	0.4990	416	972	
		500	0.3740	311	729	
		748	0.2500	208	487	

10.8.1.2 Optional self-test accuracy verification

The resulting positive and negative self-test values from the tests in Figure 26 through Figure 28 can also be compared against the self-test values stored in the device OTP (see Section 10.5 "Optional read and record stored self-test data"). This method provides a much tighter accuracy of the self-test limits. Independent positive and negative self-test values are stored for each channel. The stored values are equal to the absolute value of the difference between the self-test and offset values measured during the NXP factory trim/test at nominal temperature. Self-test stored values are captured with the user gain set to 1. Thus, the self-test limits must be calculated and then scaled with the user gain. The equation used to convert the stored self-test value to minimum and maximum self-test accuracy limits for the SNSDATA register values is shown below. Table 18 shows some example self-test accuracy limits for different ranges and settings.

$$AnalogSelfTest_{AccMin@UserGain} = Truncate[ST_{Stored}*2*(1-\Delta STACC\_T)*(UserGain)]$$

$$AnalogSelfTest_{AccMax@UserGain} = RoundUp[ST_{Stored}*2*(1+\Delta STACC\_T)*(UserGain)]$$

Where:

- $AnalogSelfTest_{AccMin@UserGain}$ = The SNSDATA register self-test accuracy min limit for the configured user gain
- $AnalogSelfTest_{AccMax@UserGain}$ = The SNSDATA register self-test accuracy min limit for the configured user gain
- ST_{Stored} = The stored self-test value for the associated channel and self-test
- $\Delta STACC\_T$ = The self-test accuracy specified tolerance
- *UserGain* = The configured gain, calculated as shown in Section 11 "Signal chain user gain selection"

Table 18. Self-test accuracy verification example test limits

Device Type	User Programmed Range (g)	User Programmed Gain	Example Self-Test Stored Value (LSB)	Self-Test Accuracy Limits SNSDATA Register Value (LSB)		Pass Fail Criteria
				Minimum	Minimum	
Medium g X	62	1	1000.00	1800	2200	Min Limit ≤ Result ≤ Max Limit
	62	1	1470.00	2646	3234	
	62	1	1800.00	3240	3960	
	125	0.4961	1000.00	892	1092	
	125	0.4961	1470.00	1312	1605	
	125	0.4961	1800.00	1607	1965	
	25	2.477	1000.00	4458	5450	
	25	2.477	1470.00	6554	8011	
	25	2.477	1800.00	8025	9809	
	15	3.875	1000.00	6975	8525	
	15	3.875	1470.00	10253	12532	
	15	3.875	1800.00	12555	15345	

10.8.1.3 Optional self-test cross-coupling verification

The self-test cross-coupling values can also be compared against the specified self-test cross-coupling output limits specified in the datasheet. The limits are independent of range, so the cross-coupling values are directly compared against the specified limits: ΔSTCh0_1 and ΔSTCh1_0.

10.8.1.4 Optional post self-test delta offset verification

The post self-test offset values can also be compared against the specified self-test delta offset limits specified in the datasheet. The limits are independent of range, so the post self-test offset delta values are directly compared against the specified limits: ΔSTOFF_T.

11 Signal chain user gain selection

The signal chain user gain is selected by a combination of the U_SNS_SHIFT bits in the CHx_CFG_U1 register and the U_SNS_MULT bits in the CHx_CFG_U2 register. The equation and some example user range and sensitivities are included in the datasheet. The process and equations for determining the U_SNS_SHIFT and U_SNS_MULT settings from desired range and sensitivity values is also listed below along with a medium g example.

1. Determine the overall sensitivity adjustment factor:
   - Desired Typical User Range = ±100 g with 12-bit data
   - Calculate Desired Sensitivity

$$Sense_{Typical\ \ Desired} = \frac{2^{11}\text{-}1}{Range_{Typical\ \ Desired}} = \frac{2047}{100} = 20.47\ \ LSB\Big/g$$

- Calculate the required sensitivity adjustment for a medium g device

$$SENSE_{Adjust\ \ Total} = \frac{Sense_{Typical\ \ Desired}}{Sense_{Typical\ \ NXP\ \ Trim}} = \frac{20.47}{33.0161} = 0.6200$$

1. Determine the best U_SNS_SHIFT setting:

Table 19. U_SNS_SHIFT settings

$Sense_{AdjustTotal}$	U_SNS_SHIFT Gain	U_SNS_SHIFT Setting
$Sense_{AdjustTotal} < 0.25$	Invalid Range	Invalid Range
$0.25 \le Sense_{AdjustTotal} < 0.50$	0.25	00
$0.50 \le Sense_{AdjustTotal} < 1.00$	0.50	01
$1.00 \le Sense_{AdjustTotal} < 2.00$	1.00	10
$2.00 \le Sense_{AdjustTotal} < 4.00$	2.00	11
$4.00 \le Sense_{AdjustTotal}$	Invalid Range	Invalid Range

1. Determine the U_SNS_MULT setting:

$$U\ \ SNS\ \ MULT = ROUND\left[\left(\frac{Sense_{Typical\ \ Desired}}{Sense_{Typical\ \ NXP\ \ Trim}{}^{*}U\ \ SNS\ \ SHIFT} - 1\right)*256\right] = \left(\frac{0.62}{0.50} - 1\right)*256 = \ \ 61decimal$$

U_SNS_MULT = 0x3D

12 Transition to Periodic Data Collection Mode (PDCM)

Once all self-test procedures are complete and verified, the system can transition the device from Command and Response Mode (CRM) to Periodic Data Collection Mode (PDCM). This can be done by two methods:

1. Send a CRM command to each device setting the ENDINIT bit.
2. Send the global Enter PDCM command.

The example in this application note uses the global “Enter PDCM” command.

Figure 29 shows the global command to enter PDCM and the Normal PDCM sequence.

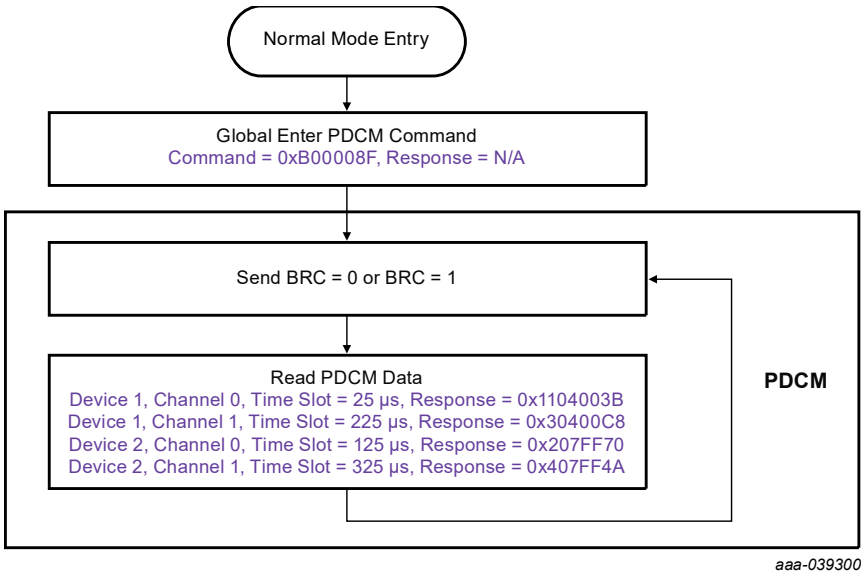

Figure 29. Transition to Periodic Data Collection Mode (PDCM)

13 Optional User Diagnostics

This section describes some additional system level diagnostics that are recommended to improve the safety performance of the device in its intended application. These diagnostics are not inherent in the device and, if used, must be conducted externally.

13.1 Startup configuration register verification

Before entering PDCM, all registers that impact the communication or signal chain configuration can be read to confirm the expected values. This is not necessary if the response to all register write commands is verified for the correct values. The response to a register write does read back the register value before transmission and is equivalent to a register read.

13.2 Continuous railed output detection

Using the sensor data from each source collected during normal mode, the following procedure can be used to detect a railed output. The example procedure uses the

configurations described in this application note and is documented for only one data source, although recommended to be completed on each data source.

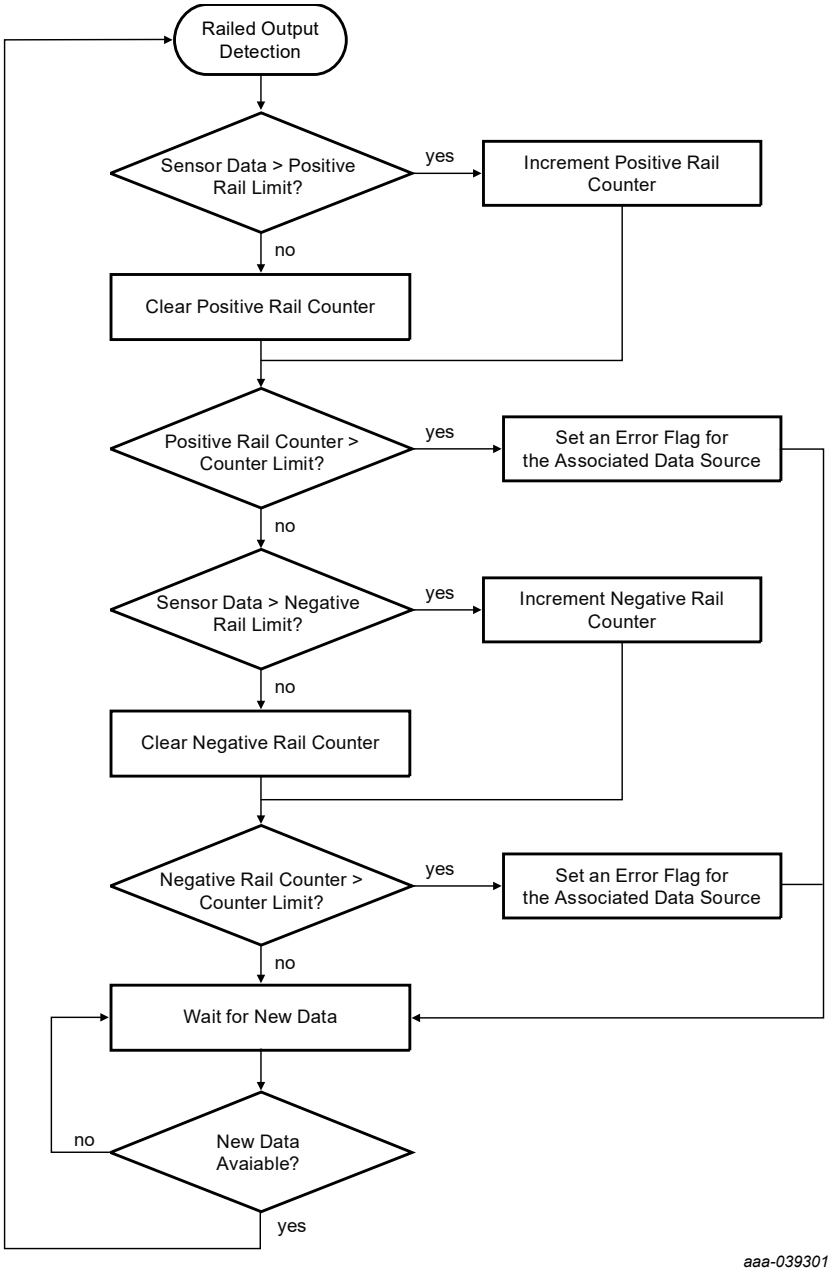

Figure 30. Continuous railed output detection

13.3 Continuous sustained step detection

Using the sensor data from each source collected during normal mode, the following procedure can be used to detect a sustained step on the output. The example procedure uses the configurations described in this application note. Step detection limits are gain, range and application dependent. Therefore, the limits for the step detection must be determined by the user based on the application.

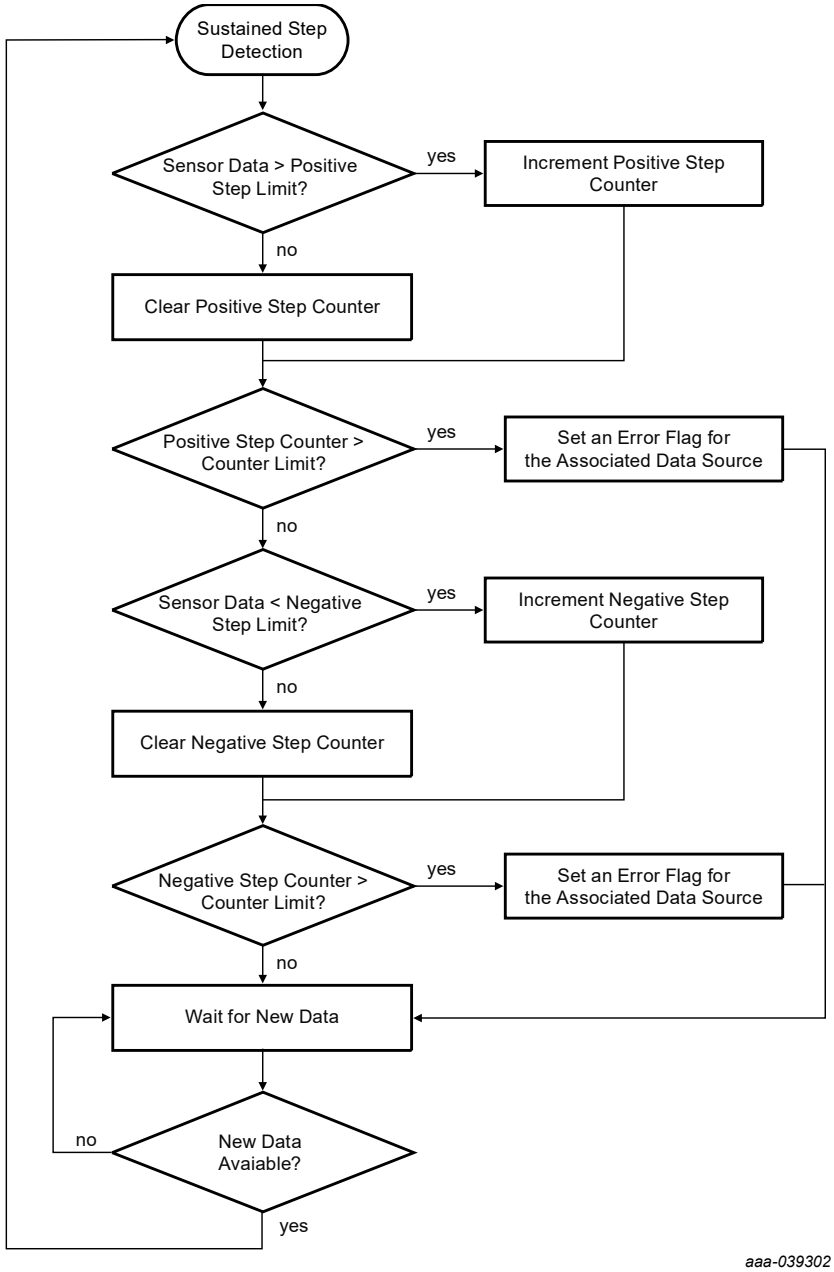

Figure 31. Continuous sustained step detection

14 Summary and Conclusion

This application note describes the recommended procedures for initializing and configuring FXLS9xxx devices on a DSI3 bus, completing self-test on the devices and finally, transitioning the devices to Normal Mode. These recommended procedures are important to meet the functional safety requirements of the intended system.

15 Appendix

15.1 DSI3 state transition diagram

Figure 32 shows a state transition diagram for the internal DSI3 controller.

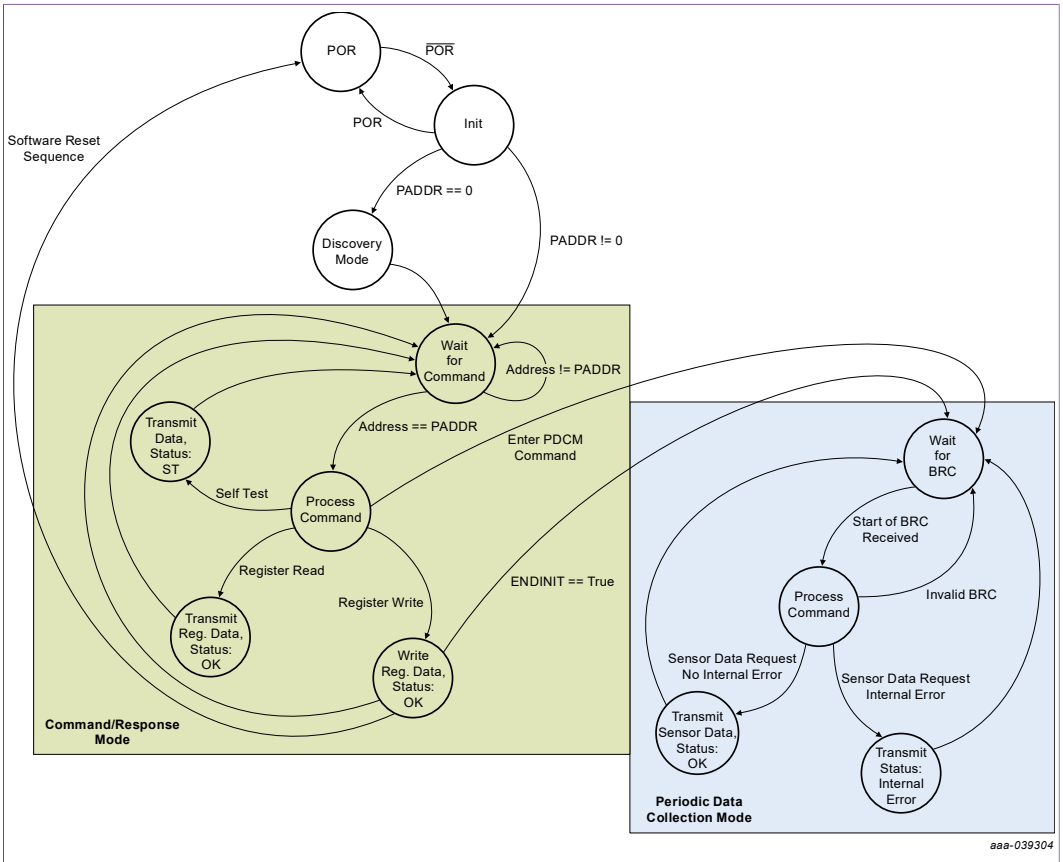

Figure 32. DSI3 state transition diagram

15.2 CRC calculation example

15.2.1 8-bit CRC

Figure 33 shows some example visual basic to calculate the DSI3 8-bit CRC.

- Function DSICRMCRC(Data32 As String, Poly As String, SEED As String) As String
  - Data32 is the 24-bit message in binary to be verified with 8 zeroes appended in place of the CRC

Example: Command = 0x0106200xx: Data32 = 0001 0000 0110 0010 0000 0000 0000 0000

- Poly is the 9-bit CRC polynomial in binary

Example: Polynomial = $X^8+X^5+X^3+X^2+X+1$ Poly = 1 0010 1111

- SEED is the 8-bit CRC Initial value in binary

Example: Seed = 0xFF SEED = 1111 1111

In this example, the CRC = 0x2E

```
Function DSICRMCRC(Data32 As String, Poly As String, SEED As String) As String
Dim i As Integer
Dim m As Integer
Dim n As Integer
Dim k As Integer
Dim bit As Integer
i = 1
m = 1
n = 1
k = 1
bit = 0
Dim CRC(1 To 8) As String
Dim CRC_old(1 To 8) As String
For i = 1 To 8
   CRC(i) = Mid(SEED, i, 1)
   CRC_old(i) = Mid(SEED, i, 1)
Next i

For n = 1 To 32
   bit = Mid(Data32, n, 1)
   For k = 1 To 8
      CRC_old(k) = CRC(k)
   Next k

   For m = 1 To 8
      If Mid(Poly, m + 1, 1) = 0 Then
         If m = 8 Then
            CRC(m) = bit
         Else
            CRC(m) = CRC_old(m + 1)
         End If
      Else
         If m = 8 Then
            If CRC_old(1) = 1 Then
               If bit = 1 Then
                  CRC(m) = 0
               Else
                  CRC(m) = 1
               End If
            Else
               If bit = 1 Then
                  CRC(m) = 1
               Else
                  CRC(m) = 0
               End If
            End If
         Else
            If CRC_old(1) = 1 Then
               If CRC_old(m + 1) = 1 Then
                  CRC(m) = 0
               Else
                  CRC(m) = 1
               End If
            Else
               If CRC_old(m + 1) = 1 Then
                  CRC(m) = 1
               Else
                  CRC(m) = 0
               End If
            End If

         End If
      End If
   Next m
Next n
DSICRMCRC = CRC(1) & CRC(2) & CRC(3) & CRC(4) & CRC(5) & CRC(6) & CRC(7) & CRC(8)
End Function
```

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Figure 33. DSI3, 8-bit CRC Visual Basic

16 Legal information

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