AN12579

Using SLCD Controller on K32L2B3 MCU

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Document information

Information	Content
Keywords	AN12579, SLCD, K32-L2
Abstract	This document describes the usage of the on-chip SLCD controller by enabling an SLCD device called S401M16KR.

1 Introduction

Customized Segment Liquid Crystal Displays (SLCD) technologies are available everywhere. For example:

- Pool maintenance: Devices that measure the pH level of swimming pools.
- Industrial safety: Monitors that detect specific gases in mine.
- Healthcare: Digital thermometers that check if a child has a fever.

SLCD is one of the oldest and most popular technologies, due to its low price and power consumption.

Segment LCDs, also called static or glass-only displays, consist of two pieces of Indium Tin Oxide (ITO) glass with a twisted nematic fluid sandwiched between them. A static display is a segment display with one pin for each segment. A segment is any line, dot, or symbol that can be turned on and off independently.

NXP K32L2B3 MCU integrates an SLCD controller module with up to eight backplanes and 47 frontplanes, such as 8 × 47 or 4 × 51.

This document describes the usage of the on-chip SLCD controller by enabling an SLCD device called S401M16KR. The S401M16KR is a four-digit 0.17-inch seven-segment LCD panel that interfaces with the K32L2B MCU through a matrix of common (COM) and data pins, enabling individual segment control for numeric display applications.

2 Hardware

This section describes the hardware components used in the SLCD implementation, including the S401M16KR SLCD device specifications and its connection to the FRDM-K32L2B development board.

2.1 S401M16KR SLCD device

The S401M16KR SLCD device contains four digits displayed on the panel. Each digit is shown with seven segments and single dot or colon, as shown in Figure 1.

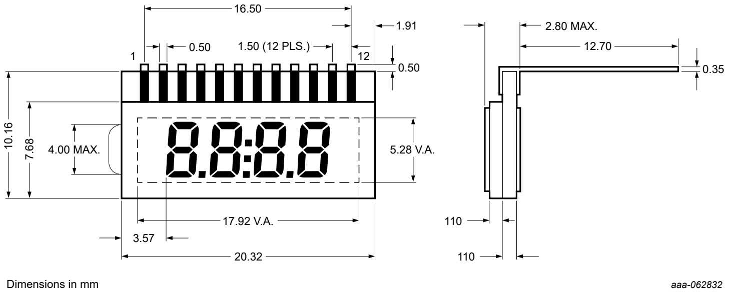
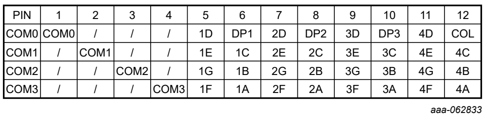


Figure 1. S401M16KR SLCD physical dimension

The S401M16KR SLCD device contains four COM pins and eight data pins as the control signals. COM pins and data pins control a matrix indicating which segments are powered on and which are powered off at a specific time, as shown in Figure 2.



PIN	1	2	3	4	5	6	7	8	9	10	11	12
COM0	COM0	/	/	/	1D	DP1	2D	DP2	3D	DP3	4D	COL
COM1	/	COM1	/	/	1E	1C	2E	2C	3E	3C	4E	4C
COM2	/	/	COM2	/	1G	1B	2G	2B	3G	3B	4G	4B
COM3	/	/	/	COM3	1F	1A	2F	2A	3F	3A	4F	4A

Figure 2. S401M16KR SLCD schematic diagram

COM pins are enabled one-by-one for each step. In each step, activated by their own COM pin, the eight data pins output the control-level signals to turn on and off the segments. The segments for each COM are switched on and off, line by line. When the four-step cycle runs rapidly, certain segments light up simultaneously, creating a combined display, even though they are not aligned in the same row of the matrix.

Consider controlling signals as an activating matrix, see Table 1.

Table 1. Activating matrix for controlling signals

nCS	D0	D1	D2	D3	D4	D5	D6	D7
COM0	1D	1DP	2D	2DP	3D	3DP	4D	4DP
COM1	1E	1C	2E	2C	3E	3C	4E	4C
COM2	1G	1B	2G	2B	3G	3B	4G	4B
COM3	1F	1A	2F	2A	3F	3A	4F	4A

For each digit position, various segments assemble the different numbers. Figure 3 shows 0 to 9 numbers in a direct segment way.

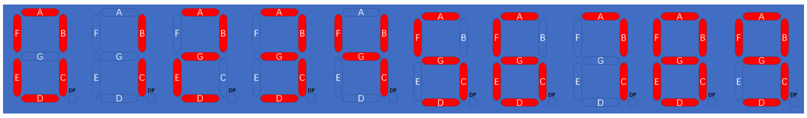


Figure 3. SLCD digits

Table 2 describes relationship between the display digits and the segment enable bits.

Table 2. SLCD digit information

Number	Segment	COM0 (.D)	COM1 (CE)	COM2 (BG)	COM3 (AF)
0	ABCDEF	0x01	0x03	0x02	0x03
1	BC	0x00	0x02	0x02	0x00
2	ABDEG	0x01	0x01	0x03	0x02
3	ABCDG	0x01	0x02	0x03	0x02
4	BCFG	0x00	0x02	0x03	0x01
5	ACDFG	0x01	0x02	0x01	0x03
6	ACDEFG	0x01	0x03	0x01	0x03
7	ABC	0x00	0x02	0x02	0x02
8	ABCDEFG	0x01	0x03	0x03	0x03
9	ABCDFG	0x01	0x02	0x03	0x03
None	—	0x00	0x00	0x00	0x00
Dot	DP	0x02	0x00	0x00	0x00

As shown in Table 2, we can get the code to show different numbers for each period activated by the indicated COMx pin.

The code array is available in the source file:

```
#define SLCD_ON_SHOW_COUNT 11u

const uint8_t SLCD_NUMBER_TABLE[][SLCD_COMx_COUNT] =
{
/* COM0, COM1, COM2, COM3 */
{ 0x1, 0x3, 0x2, 0x3 }, /* SLCD_ON_SHOW_NUMBER_0 */
{ 0x0, 0x2, 0x2, 0x0 }, /* SLCD_ON_SHOW_NUMBER_1 */
{ 0x1, 0x1, 0x3, 0x2 }, /* SLCD_ON_SHOW_NUMBER_2 */
{ 0x1, 0x2, 0x3, 0x2 }, /* SLCD_ON_SHOW_NUMBER_3 */
{ 0x0, 0x2, 0x3, 0x1 }, /* SLCD_ON_SHOW_NUMBER_4 */
{ 0x1, 0x2, 0x1, 0x3 }, /* SLCD_ON_SHOW_NUMBER_5 */
{ 0x1, 0x3, 0x1, 0x3 }, /* SLCD_ON_SHOW_NUMBER_6 */
{ 0x0, 0x2, 0x2, 0x2 }, /* SLCD_ON_SHOW_NUMBER_7 */
{ 0x1, 0x3, 0x3, 0x3 }, /* SLCD_ON_SHOW_NUMBER_8 */
{ 0x1, 0x2, 0x3, 0x3 }, /* SLCD_ON_SHOW_NUMBER_9 */
{ 0x0, 0x0, 0x0, 0x0 }, /* SLCD_ON_SHOW_NONE */
{ 0x2, 0x0, 0x0, 0x0 }, /* SLCD_ON_SHOW_DP */
};
```

Note: *The array only contains two pins for each digit. A four-digit parallel can be extended or duplicated with eight pins. The following section describes the usage of four digits.*

2.2 FRDM-K32L2B3 development board

On the FRDM-K32L2B3 development board, the SLCD device is connected to the MCU with the pins. The schematic is shown in Figure 4.

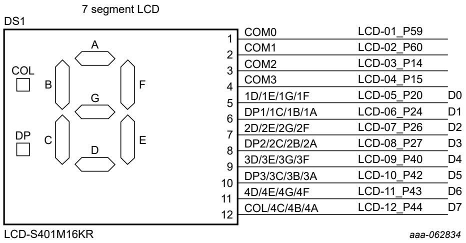


Figure 4. SLCD connections

Table 3 shows the functional information about pin settings.

Table 3. Functional information about pin settings

Functional ID	SLCD pin	MCU pin	ALT	Comments
LCD-01	P59	PTE20	ALT0	COM0
LCD-02	P60	PTE21	ALT0	COM1
LCD-03	P14	PTB18	ALT0	COM2
LCD-04	P15	PTB19	ALT0	COM3
LCD-05	P20	PTC0	ALT0	D0
LCD-06	P24	PTC4	ALT0	D1
LCD-07	P26	PTC5	ALT0	D2
LCD-08	P27	PTC6	ALT0	D3
LCD-09	P40	PTD0	ALT0	D4
LCD-10	P42	PTD2	ALT0	D5
LCD-11	P43	PTD3	ALT0	D6
LCD-12	P44	PTD4	ALT0	D7

Considered as a bus, the data signals are assembled through eight separate pins, named from D0 to D7. Coding is performed to control these signals, and the signals from each pin are treated as a complete set of data through the bus.

To operate all the control signals like a bus, the signal indexes are arranged into two arrays in the source code:

```
/* Define the sync bus and the data bus. */ #define SLCD_COMx_COUNT 4u
#define SLCD_DATA_BUS_WIDTH 8u
/* Define the pins for sync bus and data bus. */
const uint8_t SLCD_PIN_COMx[SLCD_COMx_COUNT] =
{
59, /* COM0. */
60, /* COM1. */
14, /* COM2. */
15 /* COM3. */
};
const uint8_t SLCD_PIN_DATA[SLCD_DATA_BUS_WIDTH] =
{
20, /* D0. */
24, /* D1. */
26, /* D2. */
27, /* D3. */
40, /* D4. */
42, /* D5. */
43, /* D6. */
44 /* D7. */
};
```

3 Basic usage

The SLCD controller on K32L2B is easy to use. After enabling the clock and setting up the pin mux functions, only one control register, the LCD General Control Register (LCD_GCR), is required to initialize the controller for basic usage without the blink and fault detection features.

The following code snippet provides a group of typical settings:

```
/* Setup slcd controller.
*/LCD->GCR = LCD_GCR_DUTY(3) /* Selects the duty cycle of the LCD controller
 driver. 3: 4 COMx
lines. */
| LCD_GCR_LCLK(2) /* Clock divider for clock source. 0-7 */
| LCD_GCR_SOURCE(0) /* LCD clock source. 1:use MCGIRCLK. 0:OSC32K */
| LCD_GCR_LCDEN(0) /* Disable the controller during setting. */
| LCD_GCR_LCDSTP(0) /* Keep LCD module alive in STOP modes. */
| LCD_GCR_LCDDOZE(1) /* Keep LCD module alive in DOZE mode. */
| LCD_GCR_FFR(0) /* Select the frame rate mode. 0:standard frame rate. */
| LCD_GCR_ALTSOURCE(0) /* Select the alternate clock source. no available when
 using default
clock source.*/
| LCD_GCR_ALTDIV(0) /* Clock divider for alternate clock source. no available
 when using
default clock.*/
| LCD_GCR_FDCIEN(0) /* Enables an LCD interrupt event when fault detection is
 completed.
*/
| LCD_GCR_PADSAFE(0) /* Force safe state on LCD pad control, locking all LCD
 control bits.
*/
| LCD_GCR_VSUPPLY(0) /* Select the power voltage supply. 0: from internal Vdd.
 */
| LCD_GCR_LADJ(1) /* Configures SLCD to handle different LCD glass
 capacitance.*/
```

```
| LCD_GCR_CPSEL(1) /* Selects the LCD controller charge pump or a resistor
 network to
supply the LCD voltages V_LLx. */
| LCD_GCR_RVTRIM(8) /* Regulated Voltage Trim. no available when disabled.*/
| LCD_GCR_RVEN(0) /* Regulated Voltage Enable. disabled. */
;
```

The MCU pins must be mapped to the SLCD control bus for the COMx and Dx signals:

- Configure the COMx signal mappings as back panel pins.
- Configure the Dx signal mappings as front panel pins.
- Initialize the used pins with the LCD Pin Enable registers (LCD_PEN0, LCD_PEN1) and the LCD Backpanel Enable registers (LCD_BPEN0, LCD_BPEN1). The LCD_PENx registers enable all pins in use, while the LCD_BPENx registers select them as front panel or back panel.
- Use the LCD_WF8Bx registers for the signal timing sequence of each pin.

The usage of LCD_WF8Bx registers is described as follows:

- Each register in the LCD_WF8Bx array corresponds to one LCD signal pin and the array index indicates the functional pin of the SLCD module. For example, LCD_WF8B[59] corresponds to the SLCD signal pin LCD_P59.
- Each bit in the LCD_WF8Bx register corresponds to a pin state, and the bit index indicates the step number. For example, bit 2 in LCD_WF8B[59] controls the state of pin LCD_P59 during step 2 of the entire cycle (which can include four or eight steps).

In software, controlling data signals differs slightly from hardware. The software first searches for the parallel pins and then arranges the data timing sequence. In contrast, the hardware searches the data timing for each pin first and then assembles the parallel pins into an 8-bit bus. Therefore, a conversion function is designed in the source code project.

```
/**
* @brief Set the data on SLCD control bus
* @param com_idx The index of step (COMx), 0-3.
* @param show_dat The display code to the bus for current step.
*/
void slcd_set_bus_data(uint8_t com_idx, uint8_t show_dat)
{
uint8_t bit_mask = (1u << com_idx);
for (uint8_t i = 0u; i < SLCD_DATA_BUS_WIDTH; i++)
{
if (show_dat & 0x1)w
{
LCD->WF8B[SLCD_PIN_DATA[i]] |= bit_mask;
}
else
{
LCD->WF8B[SLCD_PIN_DATA[i]] = ~bit_mask;
}
show_dat >>= 1u;
}
}
```

An API function is created to assemble the segment codes into the display matrix for the four digits. With this API, complex matrix conversion is not required. You only specify the number to display and its position to the MCU, as the software handles the conversion automatically.

```
/* keep the unchanged displaying code in the matrix. */
```

```
static uint8_t slcd_on_show_numbers[SLCD_COMx_COUNT];
/**
* @brief Set the displaying number in the digital position of SLCD device.
* @param index The index of digital position, 0-3.
* @param number The value of showing number, 0-10, while 10 is "none".
* @param en_dp Enable showing the dop in current digital positon, true or false.
*/
void slcd_set_number(uint8_t index, uint8_t number, bool en_dp)
{
uint8_t tmp8 = 0u;
for (uint8_t i = 0u; i < SLCD_COMx_COUNT; i++)
{
tmp8 = slcd_on_show_numbers[i] & (~(0x3 << (2 * index))); /* clear old setting
 code.*/
tmp8 |= (SLCD_NUMBER_TABLE[number][i] << (2 * index)); /* add new setting code.
 */
if (en_dp)
{
tmp8 |= SLCD_NUMBER_TABLE[SLCD_ON_SHOW_NUMBER_DP][i] << (2 * index); /* add new
 setting
for dot point. */
}
slcd_on_show_numbers[i] = tmp8; slcd_set_bus_data(i, slcd_on_show_numbers[i]);
}
}
```

In the main() function of the application, the following source code displays changing numbers on the target SLCD:

```
int main(void)
{
bool en_dp;

/* init board hardware. */ BOARD_InitPins(); BOARD_BootClockRUN();
 BOARD_InitDebugConsole();

PRINTF("slcd basic example.\r\n");
/* init the clock and pins for slcd, setup the controller for slcd. */
 slcd_init();

en_dp = false; while (1)
{
for (uint8_t i = 0u; i < SLCD_ON_SHOW_COUNT; i++)
{
GETCHAR();

slcd_stop(); /* stop the slcd controller before updating displaying. */
 slcd_set_number(0, i , en_dp);
slcd_set_number(1, (i+1)%SLCD_ON_SHOW_COUNT, en_dp); slcd_set_number(2, (i
+2)%SLCD_ON_SHOW_COUNT, en_dp); slcd_set_number(3, (i+3)%SLCD_ON_SHOW_COUNT,
 en_dp); slcd_start();
}
en_dp = !en_dp;
}
}
```

Download the project and run it on the FRDM-K32L2B development board. The numbers are displayed on the SLCD, as shown in Figure 5.

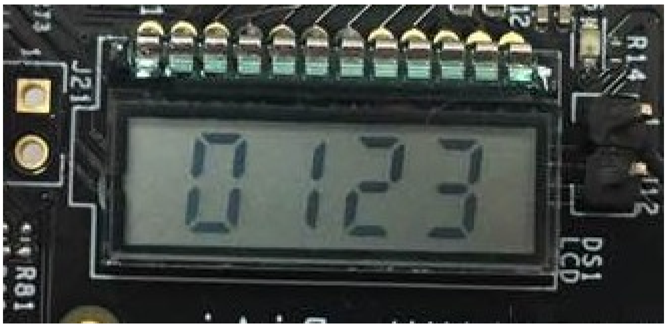


Figure 5. SLCD displaying numbers

4 Usage in low power mode

On MCUs equipped with an SLCD controller, certain low-power Stop modes provide special support for the SLCD. In these modes, most hardware components are powered down to minimize energy consumption. However, the SLCD controller controls its pins to refresh the SLCD and maintain the display on the panel.

The SLCD can work in almost all the power modes except the VLLS0 mode. For details, refer to the chapter 'Power Management' in *K32 L2B Sub-Family Reference Manual* (document K32L2B3xRM).

Table 4. SLCD in low power mode

Modules	VLPR	VLPW	Stop	VLPS	LLS	VLLSx
Segment LCD	FF Async operation in CPO	FF	Async operation FF in PSTOP2	Async operation	Async operation	Async operation, OFF in VLLS0

To keep the SLCD operational in low-power modes, the critical settings are as follows:

- Clock source: Keep the clock source for the SLCD controller active in the target low-power mode. For example, if the SLCD controller uses the 32 kHz oscillator, verify that this clock source is enabled in all modes, including VLLSx.
- Pin mux: Configure SLCD controller pins for the analog function (ALT0) and lock the pins for other digital functions (their voltage levels cannot change) in VLLSx mode. The SLCD controller can output waves and the SLCD panel can display digits only when these pins remain active.
- Low-power mode settings: Enable low-power support for the SLCD controller by setting the LCD_GCR[LCDSTP] and LCD_GCR[LCDDOZE] bits to 0 to keep the SLCD controller operational in Stop and Wait modes.

After configuring the above parameters, set up the SLCD controller to display content, and then enter the low-power Stop mode. In this mode, the display on the SLCD panel remains on because the controller continues to output refresh signals.

Figure 6 shows the example project in VLLS3 mode, with the RTC and SLCD controller running. The measuring current on the FRDM-K32L2B development board is as low as 7 µA.

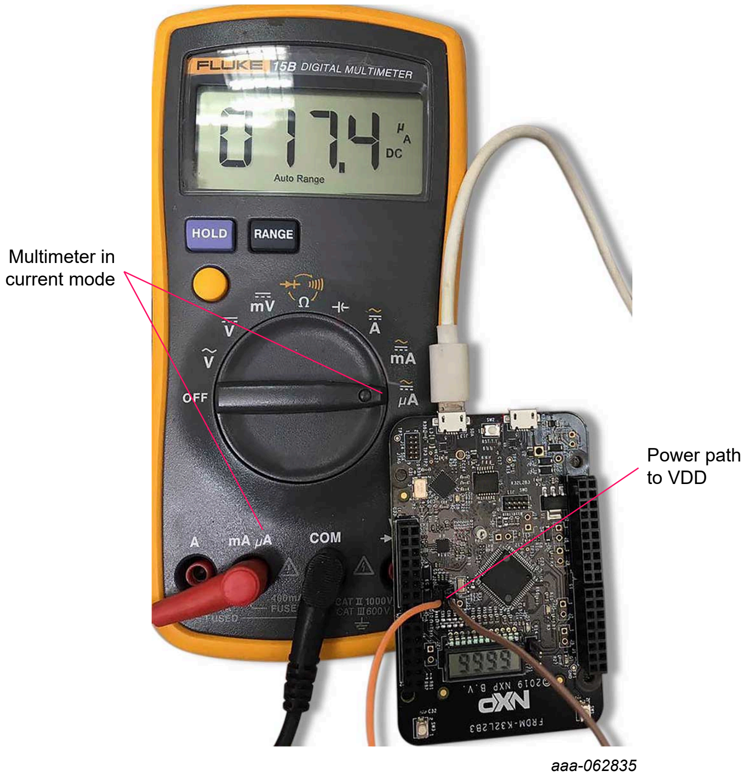


Figure 6. SLCD low power display

5 Conclusion

This document describes basic usages of the on-chip SLCD controller on the K32L2B MCU, with the example projects based on the FRDM-K32L2B development board. The SLCD controller can control the SLCD device to display the contents on its panel automatically with suitable configurations on the hardware. Even in the low power modes, the SLCD controller can still work with low energy, therefore, indicating that the K32L2B with an on-chip SLCD controller can be used in the energy-sensitive application field.

6 Acronyms

Table 5 lists the acronyms used in this document.

Table 5. Acronyms

Term	Description
API	Application Programming Interface
GPIO	General-Purpose Input/Output
ITO	Indium Tin Oxide
LCD	Liquid Crystal Display
MCU	Microcontroller Unit
RTC	Real Time Clock
SLCD	Segment Liquid Crystal Display

7 References

Table 6 lists the references used to supplement this document.

Table 6. References

Reference	Link/how to obtain
Custom Segment LCDs	https://focuslcds.com/segment-lcd/
Ultra-Low-Power, Highly Integrated MCU	https://www.nxp.com/products/K32-L2
K32 L2B Sub-Family Reference Manual (document K32L2 B3xRM)	https://www.nxp.com/webapp/sps/download/preDownload.jsp?render=true

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9 Revision history

Table 7 summarizes the revisions to this document.

Table 7. Revision history

Document ID	Release date	Description
AN12579 v.1.0	30 September 2025	• Updated Table 2 in Section 2.1 • Added Section 8 • Updated document to latest style sheet
0	12 December 2019	Initial public release

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