AN12549

PN5190 antenna design guide

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Document information

Information	Content
Keywords	PN5190, NFC antenna design, NFC antenna tuning
Abstract	This document describes the NFC antenna design and tuning related to the PN5190. This includes the Dynamic Power Control 2.0 functionality. It gives some layout recommendations as well some guidelines, how to adjust (“calibrate”) the DPC.

1 Introduction

The antenna design for the PN5190 is not much different than the antenna design for most of the other NXP reader ICs in general. However, some PN5190 specific details need to be considered to get an optimum performance.

This document describes the generic NFC and RFID antenna design as simple as possible, focusing on the requirements for EMVCo POS design.

1.1 Dynamic Power Control 2.0

The Dynamic Power Control (DPC 2.0) feature of the PN5190 allows an improved antenna design with an improved transfer function. It is required to configure ("calibrate") the DPC properly to get the optimum performance.

The NFC Cockpit (PN5190 GUI) supports the process of the DPC calibration, which includes:

- The adjustment of the basic settings
- The step-by-step calibration
- The PCD TX shaping

The steps to calibrate the DPC and optimize the PN5190 registers are described in Section 5.

Note: *A wrong antenna tuning or a bad DPC calibration can drive a too strong HF field and can even destroy the PN5190.*

1.2 Prerequisites

The NFC antenna design requires a basic understanding of analog electronic design. The tuning procedure is simple and explained in detail, and therefore does not require any specific RF know-how.

The NFC antenna is one part of an RF transformer rather than a typical RF antenna. Therefore, some typical antenna definitions do not apply for NFC antennas:

The NFC antenna changes its impedance during normal operation and for this reason, a 50 Ω design does not make sense.

The NFC Reader is an RF device that requires a careful design, especially for the layout as:

- Power levels of up to 2 W are driven.
- The receiver circuit must detect data signals in the mV range.

The design of the environment is part of the antenna design. Especially, the metal design influences the antenna behavior, and so the NFC performance. Without the environment design, no antenna design can be done. That means, the mechanical frame conditions must be known and considered. The housing and mounting places also influence the overall performance.

Note: *The use of a Vector Network Analyzer (VNA) is required for proper antenna tuning.*

2 NFC reader antenna design

For the NFC operation three different communication modes are specified in [4]:

1. In the **card emulation mode (CM)** the NFC device can be used in (existing) NFC reader infrastructure. In the CM the NFC device behaves in principle like a PICC, as defined in [2]. This mode is optional.
2. In the **card reader mode (RM)** the NFC device can be used with (existing) NFC cards. In the RM the NFC device behaves in principle like a PCD, as defined in [2]. This mode is mandatory.
3. In the **peer to peer mode (P2P)** the NFC device can communicate to other NFC devices, either being the initiator, starting the communication, or being the target, answering the communication.

For the communication between two NFC devices the two different P2P modes are available:

1. **Active P2P**: Both NFC devices, the initiator as well as the target, are required to generate their own magnetic field, when sending data. This mode is optional.
2. **Passive P2P**: The initiator always generates the magnetic field, while the target uses the load modulation principle to send its data. This mode is mandatory.

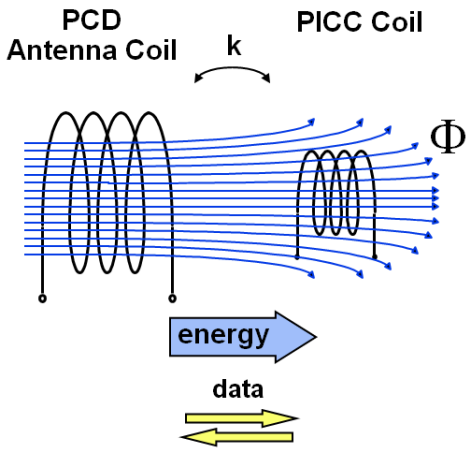
2.1 ISO/IEC 14443 specifics

The ISO/IEC 14443 (called “ISO” in the following, details see [2]) specifies the contactless interface as widely being used with contactless smartcards like MIFARE product-based cards.

The ISO/IEC 14443 defines the communication between a reader (“proximity coupling device” = PCD) and a contactless smart card (“proximity chip card” = PICC). The four parts describe the physical characteristics (the size of the PICC antennas), the analog parameters such as modulation and coding schemes, the card activation sequences (“Anticollision”), and the digital protocol. The ISO/IEC 10373-6 (see [3]) describes as well the test setup as well as all the related tests for cards and the reader.

The ISO/IEC 14443 reader antenna consists of an antenna coil, which is matched to the reader IC. This antenna coil, as shown in Figure 1,

1. generates the magnetic field to provide the power to operate a card (PICC),
2. transmits the data from the reader (PCD) to the card (PICC), and receives the data from the card (PICC) to the reader (PCD).

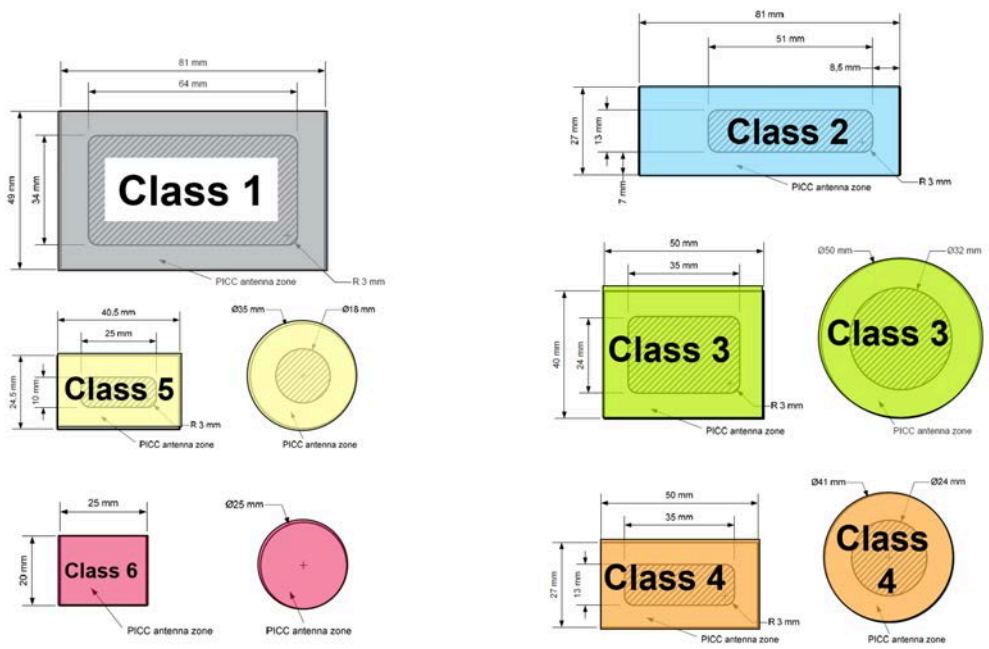


1. k = coupling coefficient
2. Φ = magnetic flux

Figure 1. Magnetic coupling between reader (PCD) and card (PICC)

According to the ISO/IEC 14443 the PICC antenna coils can be categorized into the classes 1 …6, as shown in Figure 2.

The PCD antenna is not defined as such, but the PCD must support the classes 1, 2, and 3. The support of the classes 4, 5, and 6 is optional.



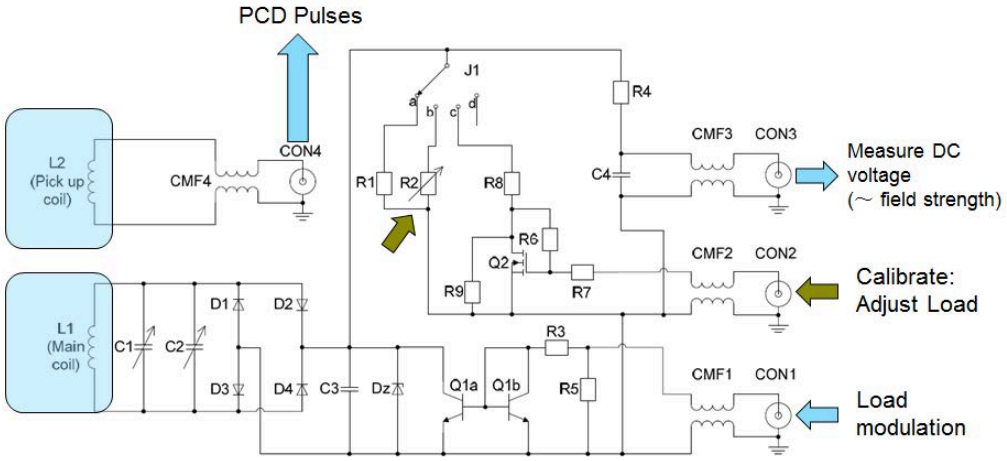
1. A PCD must always support the classes 1, 2, and 3. The Classes 4, 5 and 6 are optional.

Figure 2. PICC Classes according to the ISO/IEC 14443

The PCD antenna coil sizes are not specified. So for ISO/IEC 14443 compliant readers all different sizes of antenna coils from a few 10 mm^2 up to 20 cm diameter can be found in various shapes.

The ISO/IEC 14443 does not specify an operating volume. The reader manufacturer needs to guarantee that within the operating volume - that they themselves define - all related ISO/IEC 10373-6 tests can be passed.

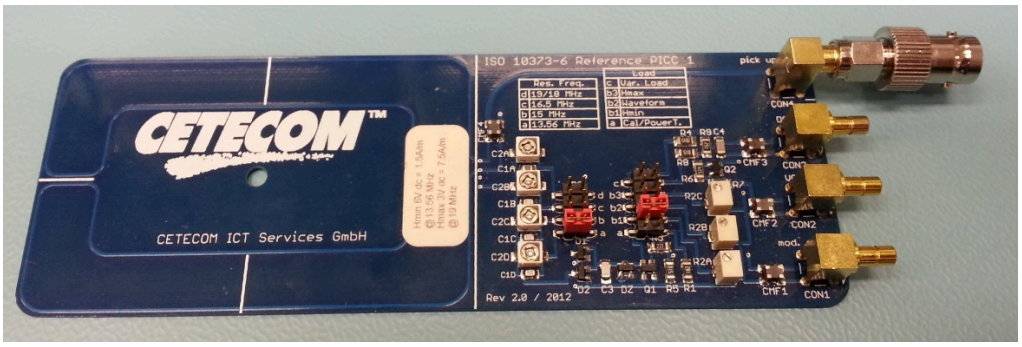
The compliance tests require calibrated ReferencePICCs, as defined in ISO/IEC10373-6. The schematic of such ReferencePICC is shown in Figure 3. For each PICC Class there is one Reference PICC, which needs to be calibrated according to the required measurement. Practically it makes sense to use one calibrated ReferencePICC for each measurement case.



1. Details see [3].

Figure 3. Schematics of the ISO/IEC 10373-6 ReferencePICC

Some commercially available ReferencePICCs (for example Figure 4), are pre-calibrated and equipped with several jumper options to address the most relevant tests with a single ReferencePICC.



1. The jumper settings allow the use of different pre-calibration settings.

Figure 4. ISO/IEC 10373-6 Reference PICC Class 1

For each PICC Class, a separated ReferencePICC is required.

The **most** relevant analog tests for PCDs are:

1. Field strength test (min and max)
2. Wave shape tests (for all bit rates)
3. Load modulation amplitude tests

Note: *This application note does not replace the detailed test description in the ISO/IEC 10373-6.*

There is no common certification process for ISO/IEC14443 compliance in place, even though many national bodies use the ISO/IEC 14443 to operate the electronic passports and electronic ID cards. For these programs, some nations have established a certification process to guarantee interoperability. An example is given in [5].

2.1.1 Field strength

For the field strength test it is preferred to have the PCD send a continuous carrier. That is, PCD performs no modulation.

The field strength tests require the calibrated ReferencePICC and a DC voltage measurement device (volt meter or oscilloscope). The field strength is equivalent to the calibrated (and required) voltage level. The ISO/IEC 10373-6 defines:

- Minimum voltage levels that correspond to the minimum required field strength.
- Maximum voltage levels that correspond to the maximum allowed field strength.

The measured voltage levels must stay within the two limits.

2.1.2 Wave shapes

The PCD must send the related pulses: either an ISO/IEC 14443 REQA and / or REQB with the required bit rate, as specified in [5]. Any other command fits the purpose.

The standard way of activating higher bit rates is not useful for the wave shape test as the ReferencePICC for ISO/IEC 14443-2 tests does not allow the protocol layer required to switch to higher bit rates.

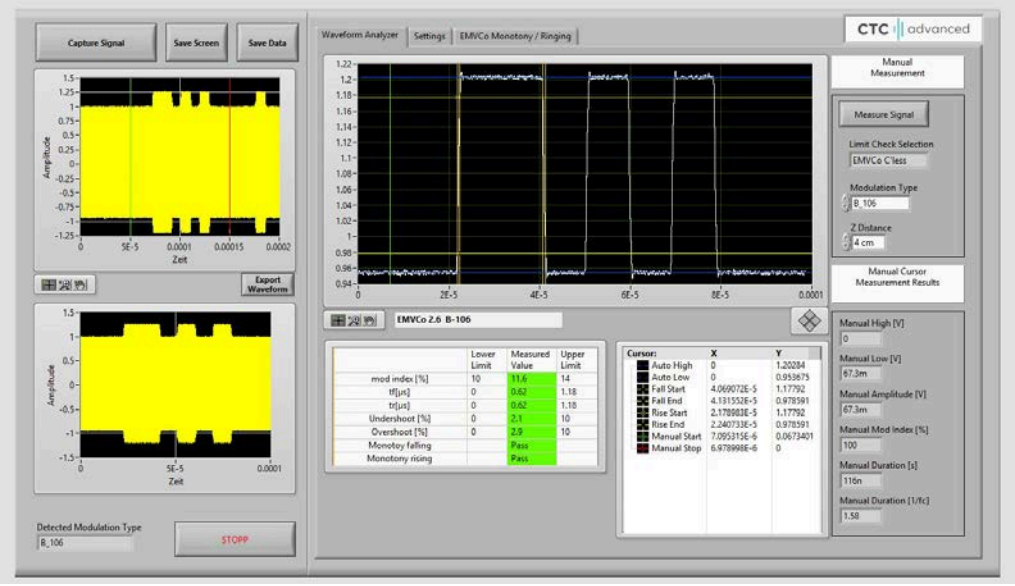
Note: *For the test of higher bit rates, it makes sense to implement some specific test commands. The test commands send artificial commands such as REQA and / or REQB, using the coding and modulation of the corresponding higher bit rates. This feature is provided via the NFC Cockpit, where the REQA or REQB polling can be done with any of the supported data rates. The NFC Cockpit allows to easily test the analog performance as such, ignoring the high-level features, which are required to activate the protocol layer.*

The wave shape tests require

1. A calibrated ReferencePICC, which is placed at the position of the calibrated field strength (corresponding to the DC voltage as measured in Section 2.1.1),
2. A digital oscilloscope with a measurement bandwidth of 500Msamples or higher, and
3. A tool that filters and transforms the oscilloscope data into the envelope signal according to the ISO/IEC 10373-6.

The tool returns: the filtered and transformed envelop, the corresponding values of rise and fall times, residual carrier levels, and over- and undershoots, which must be kept within the given limits.

The CTC Advanced WaveChecker tool can be used for the tests (Figure 5).



1. Example of EMVCo type B signal

Figure 5. CTC Advanced WaveChecker

2.1.3 Load modulation

The PCD needs to send a test command, which allows to check a response from the ReferencePICC. The response from ReferencePICC then needs to be properly received by the NFC Reader.

The load modulation tests require

1. A calibrated ReferencePICC, which is placed at the position of the calibrated field strength (corresponding to the DC voltage as measured in Section 2.1.1),
2. A signal generator with a pattern generator (Arbitrary Wave Generator, AWG), that provides the load modulation input signal as a response to the PCD test commands.

The response must be triggered by the PCD test command, i.e. the signal generator needs a delayed trigger input either from the field or from the PCD itself. The voltage level of the load modulation input signal for each test case must be (pre-) calibrated in the TestPCD set up.

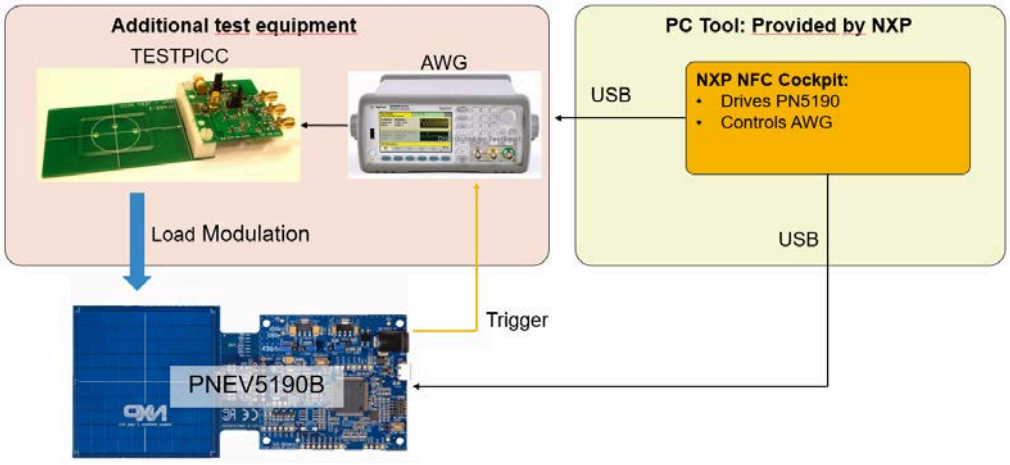
The PCD must be able to receive all the responses with the given minimum load modulation signal level. The Figure 6 shows a minimum required setup to test and optimize the load modulation performance of the PN5190 NFC Reader. The NFC Cockpit controls the PN5190 in the PNEV5190B (or in any customer design).

The AWG (Keysight 33511B with arbitrary license) can easily be controlled by:

1. The **NXP NFC Cockpit**: this feature is provided by the NXP NFC Cockpit, if the AWG support is selected during the installation of the NFC Cockpit. However, there is no direct information available about the required LMA level, since there is no calibration procedure available.
2. The **CTC Advanced WavePlayer** (see [15]): this PC tool is provided by CTC Advanced. It is available in combination with calibration data for ISO ReferencePICCs and EMVCo TestPICCs. This allows an accurate ISO and EMVCo Pretest.

The AWG needs to be triggered to send the “card response”. This trigger can be derived in different ways:

1. From a sniffer device that traces the PCD commands, for example the FIME Smartspy Contactless (see [14]).
2. From a trigger output of an oscilloscope, which triggers itself by the sent waveshapes. The waveshapes (RF trace) can be traced with a simple pickup coil.
3. From a PN5190 test signal, which indicates that the command has been sent (falling edge of TxActive).



1. The NFC Cockpit supports the Keysight 33511B series (see [13]), if the arbitrary function is enabled.

Figure 6. Minimum test setup for LMA tests

2.2 EMVCo specifics

EMVCo specifies a contactless interface for point of sales (POS) terminals (= PCD) and the corresponding contactless payment cards (= PICC) in [6]. This interface is similar to the interface defined ISO/IEC 14443, but it uses its own set of requirements and specification details. Especially, the EMVCo test equipment and the way of testing differ from the test specification defined in ISO/IEC 10373-6.

On the one hand, EMVCo specifies and requires only the bit rate of 106 kbit/s for both types A and B. No higher bit rates are required, which simplifies the design.

On the other hand, EMVCo specifies an operating volume and intensive analog and digital tests. The tests require the software implementation of a specific test transaction ("EMVCo loopback").

The advantage of this way of testing is that the test parameters can be tested "from the outside". That is, it is not required to access the POS terminal to check that the POS as received the card response.

The disadvantage of such a test is that multiple parameters must pass the test. The test fails if a single parameter fails. The debug is complex, and parameter optimization is impossible.

As an example, the LMA test fails if the EMD handling is not well implemented, or if the wave shapes are not good enough.

2.2.1 EMVCo analog test with version 3.0

With the introduction of the version 3.0 of the EMVCo contactless specification, the test effort has increased a lot. For the reader tests three calibrated EMVCo TestPICCs are required. These EMVCo TestPICCs can be bought only from one of the accredited laboratories.

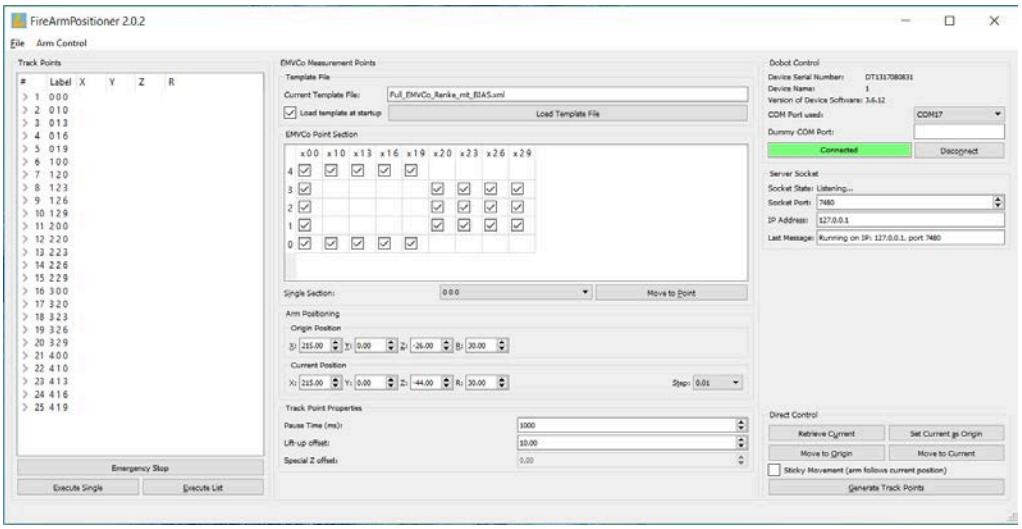
The relevant analog tests for PCDs are:

1. PCD power test (field strength)
2. Modulation PCD-> PICC tests (wave shape tests)
3. Load modulation tests (PICC -> PCD tests)

Note: *This application note does not replace the detailed test description in the EMVCo specification.*

The EMVCo version 3.0 adds several tests. The design is not changed, but the effort is increased, especially the test effort. For the debug and optimization of parameters, it is recommended to use a robot to cover the operating volume.

NXP provides FireArmPositioner tool ([16]) to control of a low-cost robot to step through the defined positions of the EMVCo operating volume. The tool requires the Dobot Magician and a fixture to fix the EMVCo TESTPICCs to robot arm.

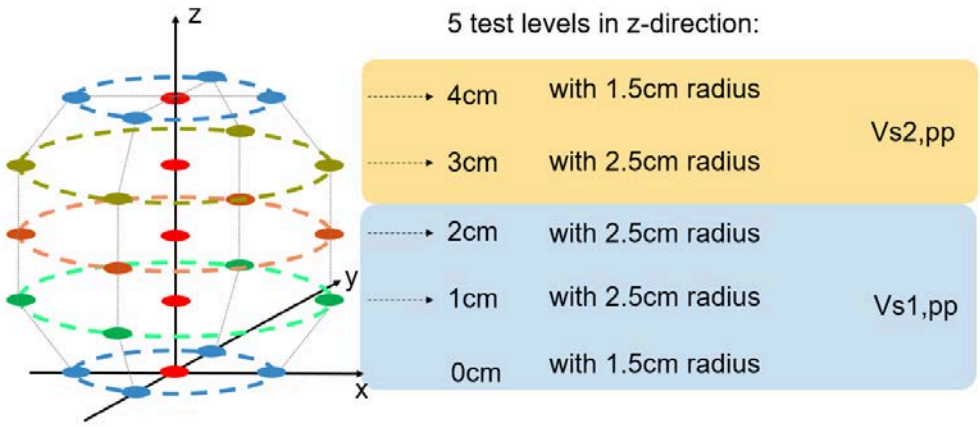


1. This tool controls the Dobot Magician (see [16])

Figure 7. NXP FireArmPositioner

2.2.2 EMVCo operating volume

One main difference for the tests between ISO/IEC and EMVCo is the definition of an operating volume, as shown in Figure 8. This volume is tested with the EMVCo TestPICCs.



1. 25 positions in total: position 000 is defined by the landing zone
2. Details see [6]

Figure 8. EMVCo POS operating volume requirement

Within this volume, the given parameters must be fulfilled.

It helps to use a robot to position the TestPICCs in any of the defined 25 positions.

2.2.3 EMVCo field strength (= “power transfer”)

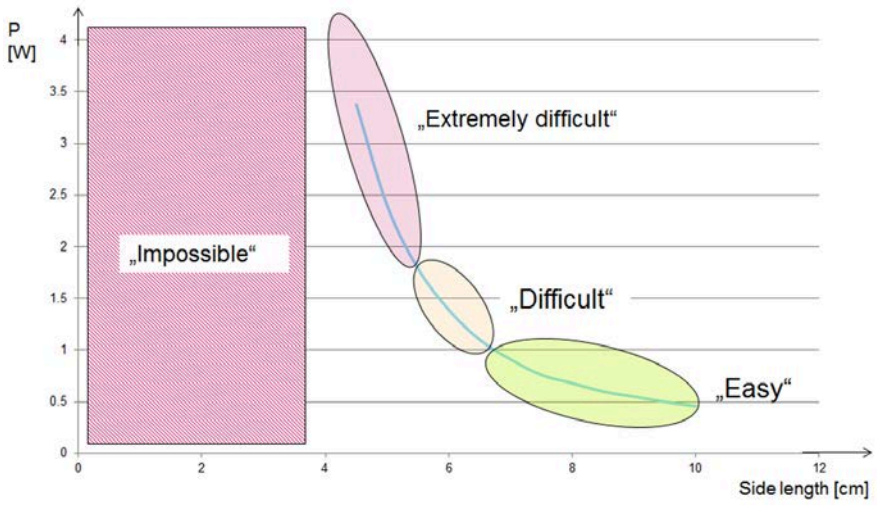
For the manual field strength test, it is preferred to have the PCD send a continuous carrier, that is, it performs no modulation.

The voltage level can be measured in all positions with all three TestPICCs. The value must be between the minimum and maximum limits given in [6].

Due to the operating volume, it can become challenging to meet the EMVCo requirements with small antennas.

The Figure 9 shows the required power as a function of the antenna size. The curve is based on an antenna simulation with a few simplifications, so it does not consider the loading effect of the EMVCo TestPICCs. Yet, the simulation was done under ideal environmental conditions, with no influence of the metal environment on the antenna. The simulation results can be taken as a reference to estimate the design effort, especially for small antennas compared to "normal" antenna sizes.

Note: *The PN5190 allows a more flexible antenna design because it drives more power into the antenna compared to other NFC Reader ICs. But at the same time, the DPC 2.0 controls the power transfer and the TxShaping at closer distances. Still, even the PN5190 cannot overcome the physical limitations. Especially, the Interoperability tests reveal the gaps of the compliance tests when test cards with small half-size antennas are tested. In such cases, and if the POS antenna is small, the coupling in some of the operating volume positions can be (close to) zero. Then no communication is possible.*



1. Simulation of a square antenna
2. These simulation results do not take any specific environment or loading effects into account.

Figure 9. EMVCo POS Reader antenna size

2.2.4 EMVCo wave shapes

The PCD must send the related pulses: It can send an EMVCo WUPA and / or WUPB (or standard REQA / REQB).

The wave shape tests require:

1. Three calibrated EMVCo TestPICCs, which are placed at each of the given positions (see [6]).
2. A digital oscilloscope with a measurement bandwidth of 500Msamples or higher.
3. A tool that filters and transforms the oscilloscope data into the envelope signal according to the EMVCo test requirement.

The tool normally returns: the filtered and transformed envelop, the corresponding values of rise and fall times, residual carrier levels, and over- and undershoots, which must be kept within the given limits. An easy solution is the CTC Advanced WaveChecker (see [12]).

Note: *In some positions, the signal level, as picked up by the defined Pick-Up coil, can be in the range of 10 mV (= noise level). Low signal levels can happen even though the power transfer indicates enough field in the position of the TESTPICC. For example, if the field distribution becomes inhomogeneous in that position, the Pick-Up coil cannot work properly. In such a case, the geometry of the POS antenna, or at least the position of the landing zone must be changed, since the EMVCo test does not allow a pickup with external sniffer coil.*

2.2.5 EMVCo LMA

The PCD sends a test command to check the reception of a response from the TestPICC. In the official tests, the EMVCo loop back command sequence is used.

Note:

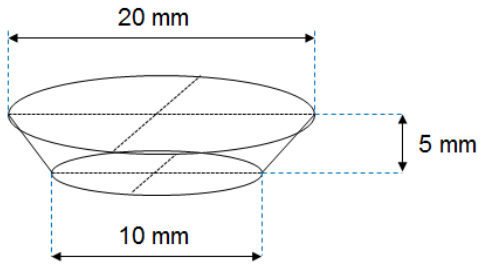
1. *Official tests do not provide useful debugging or optimization. Simple test commands are more useful than the full EMVCo test sequence. These commands can be debugged easily and the triggering is easier. The NFC Cockpit allows such simple tests, including the use of an Arbitrary Wave Generator (AWG) to drive the card response. The principle is described in Section 2.1.3. For EMVCo, use only the calibrated EMVCo TESTPICCs instead of the ISO ReferencePICCs.*
2. *>EMVCo tests both negative and positive load modulations. The CTC Advanced WvePlayer tool generates both signal forms according to the EMVCo specification, but the AWG support of the NFC Cockpit does not. The PN5190 does not distinguish negative and positive load modulations, so either can be tested. However, due to a bad saturation and heating effect of the TESTPICC, the negative load modulation can only be applied for a short period. The test tool has to switch the load before and after the response. The load switch causes EMD events that the PCD must handle before these tests can be applied.*

2.3 NFC specifics

The standard NFC device must fulfill the reader mode (PCD), the passive target, and the passive initiator. The passive target, from an antenna point of view, is similar to the optional card mode (PICC).

2.3.1 NFC operating volume

The NFC Forum specifies an operating volume as shown in Figure 10. All specified parameters are tested at given test points within the operating volume. This is valid for all tests including reader mode tests.



1. Details see NFC Analog Technical Specification, [4]

Figure 10. NFC operating volume

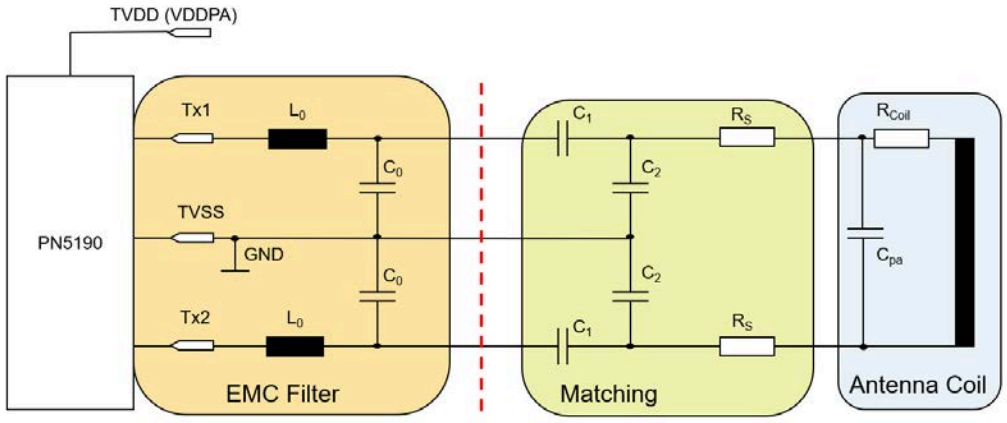
3 PN5190 antenna requirements

The PN5190 uses the NXP NFC standard antenna circuit, as well known with other NFC NXP reader ICs.

The PN5190 is optimized to support the NFC, ISO and EMVCo with a minimum of additional components. The PN5190 simply requires the antenna matching circuitry, some block capacitors and the crystal.

However, the calculation and tuning of the matching components as well as the setting adjustment need to be done carefully to provide the full performance as well as to meet CE and FCC regulations.

The design starts with the TX part, as shown in Figure 11.



1. The circuit is shown simplified.

Figure 11. TX part of the PN5190 antenna circuit

Note: *It makes sense to foresee two parallel footprints for each of the tuning capacitors. That allows to place two parallel capacitors instead of only a single one for better value adjustment.*

3.1 Start parameters

For the start of the antenna tuning procedure some start parameters needs to be defined. These values might be taken to start an antenna design, using the NXP NFC Antenna Tool, which can be downloaded from the NXP NFC Antenna Design Hub (refer to [11]).

3.1.1 Target impedance

The target impedance defines the current consumption and the field strength. The lower the target impedance, the higher the driver current ITVDD gets, and the more output power the PN5190 can drive.

The ITVDD limit of $ITVDD_{max}$ = 350 mA defines the minimum target impedance of $Z \approx 13 \ldots 14\Omega$.

An impedance of less than 20 Ω typically drives more than 200 mA. The lowest possible target impedance is chosen to get the maximum output power, especially since the DPC 2.0 can control and limit the output power per setting.

However, the control range of the DPC 2.0 is limited from TVDD = 1.5 V to 5.7V. Sometimes, at close distances to a small antenna, the maximum allowed power transfer (field strength) is exceeded even with the lowest TVDD settings. In this case, the target impedance must be increased.

If no other input is known, the recommended target impedance is $Z \approx 15 \ldots 17\Omega$.

3.1.2 Q factor

The Q- factor defines the bandwidth available to transfer data. This definition includes the complete transfer channel, including the PICC or phone. The limits are normally specified via the wave shape requirements.

The final Q factor of the overall antenna setup depends on many frame conditions such as environment or PICC loading. The conditions are not fully known and they can change during the operation or test. So, it makes no sense to calculate and adjust the antenna based on a too precise value. The final Q must be tuned with the pulse shape measurements, if the antenna must be fully optimized.

Reasonable values vary from 10 up to 30, and a typical starting value can be a number between 20 and 25.

If no other input is known, Q = 22 is used.

The higher the Q factor, the better the power transfer, but the lower the stability gets.

Note: *While ISO allows data rates of up to 848 kbit/s, NFC allows data rates of up to 424 kbit/s. EMVCo systems are limited to 106 kbit/s. So, typically the Q of EMVCo reader systems can be higher than the Q of ISO or NFC reader systems.*

3.1.3 EMC filter cut-off frequency

The cut-off frequency of the EMC filter must be:

- Above 13.56 MHz to pass enough energy.
- Below 27.12 MHz to block the second harmonic.

The cut-off frequency defines the "symmetry" of the antenna. For "asymmetric" antenna tunings (as used for CLRC663), the cut-off frequency is $f_{EMCasymmteric} \approx 16 \ldots 22MHz.$

For the PN5190 a "symmetric" antenna design is recommended, which requires a lower cut-off frequency $f_{EMCPN5190} \approx 14.3 \ldots 14.6MHz.$

3.1.4 EMC filter inductor

The inductor L0 is a key component of the EMC filter in the overall antenna design. L0 defines the output power, the wave shapes, the loading behavior, and the radiation of unwanted harmonics.

Losses:

The losses of L0 must be as low as possible.

Note: *The losses are specified or measured under NFC operating conditions (at 13.56 MHz and the required power/current level). The specification of inductors uses lower frequencies and lower power conditions.*

Power rating:

For NFC use case with high current and under normal conditions, L0 can heat up easily, especially if L0 has high losses.

Nonlinearity:

Some high Q inductors use ferrite cores that can go into saturation. As a consequence, a nonlinear behavior can occur, and limit the output power and/or disturb the wave shapes.

A lower inductance value leads to lower losses. Since the PN5190 does not need to comply with the correlation requirement (as known from PN5180), the inductance value can be low. If no other input is known, use L0 = 160 nH.

Note: *Foresee a footprint size of 0805 so that both 0805 and 0603 components can be assembled. That gives the maximum flexibility for the final choice of L0.*

3.2 Comparison to PN5180 antenna design

The antenna design for the PN5190 is the same as other NXP NFC reader ICs such as the PN5180. The PN5190 provides new features to consider for optimized performance.

3.2.1 Power

The DPC 2.0 of the PN5190 directly measures the driver current, so no correlation requirement (as known from the PN5180 or PN7462) needs to be considered. That allows to use lower inductance values for L0, which decreases the losses.

The better EMC filter inductor in combination with the improved PN5190 TX driver design (lower losses + higher TVDD) and the increased driver current limit (from 250 mA to 350 mA) increases the output power quite a lot. So in many cases it makes sense to increase the antenna impedance to reduce the power as such.

At the same time, the control range has increased compared to PN5180: The PN5190 allows the full power control over the VDDPA from 5.7 V down to 1.5 V, if needed.

3.2.2 Waveshaping

The DPC 2.0 provides an easy-to-use TX shaping feature. TX shaping compensates the ringing or damping effects under different loading conditions. This feature is similar to the PN5180 TX shaping feature, but easier to adjust. PN5190 TX shaping feature allows flexible shaping for the falling and the rising edge of the ASK modulation pulses, which can compensate any setup issues.

Some EMVCo tests only pass with the help of such a feature when specific antenna forms are used.

3.2.3 Receiver performance

The PN5190 provides a complete new RX concept, compared to the known NFC reader ICs like e.g. the PN5180. With this concept the overall sensitivity, but even more important, the robustness against noise signals has been improved. The adjustment of RX settings has become less complex.

However, the external RX circuit stays as simple as it has been.

3.3 Layout recommendations for BGA

To ensure performance and comply with CE, FCC, or MIC regulations, the basic analog design must be kept. The following sections provide recommendations and show which parts of the design are most critical in terms of layout.

The RF circuit, the antenna circuit, and the power supply are the main parts to consider.

3.3.1 PN5190 BGA RF circuit recommendations

Layout recommendations for the PN5190:

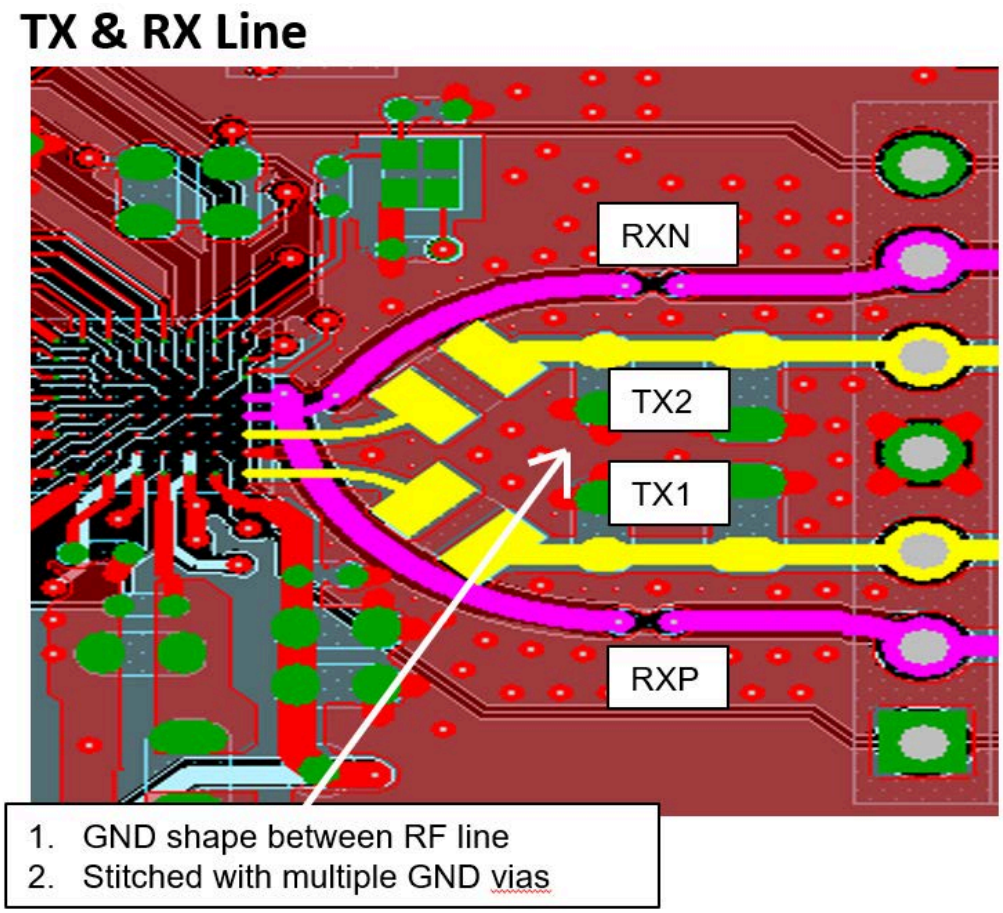
1. Place components as close as possible to the IC.
2. Place two inductors L0 close to each other, either perpendicular or at a 45-degree angle.
3. Place the capacitor of the RX line close to PN5190.
4. To keep a short TX line, place the inductor L0 very close to PN5190.

Guidelines for the routing:

1. Route TX line in Top Layer (due to huge current).
2. Route RX line in Top Layer (if possible), or route in Layer 3 (internal signal Layer 1) depending on the matching network and antenna placement.
3. Do not use any via for TX Line.
4. Use blind via for the RX line.
5. Route with any angle routing. No 90 degree/45 degree or odd angle bends are required.
6. RX and TX lines must be routed with GND separation (avoid cross-talking).
7. Route TX lines symmetrical to each other, and route RX lines symmetrical to each other.

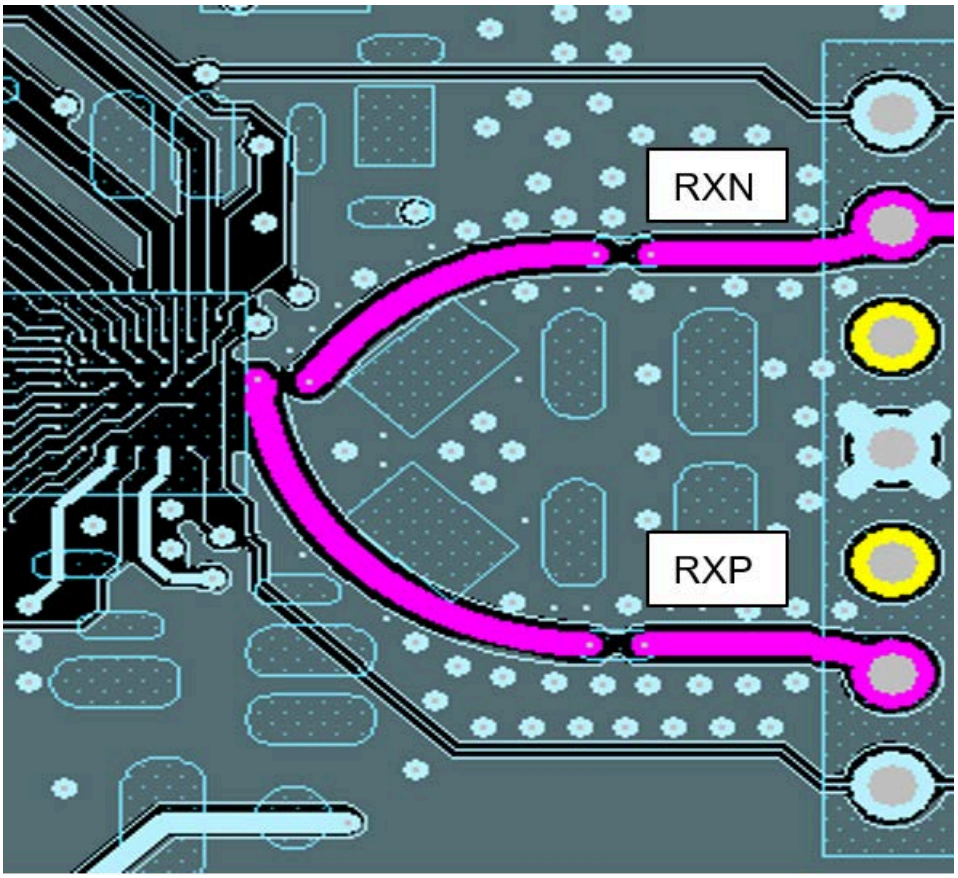
The GND layer is an important part of the layout (see Figure 13).

1. Provide a solid GND plane on adjacent Layer (L2_GND).
2. Fill all layers with GND shape.
3. Stitch with multiple GND via around RF line.
4. No test points are allowed.
5. No silk label on RF traces.



1. Screenshot with multiple layers

Figure 12. PN5190 Layout Reference example



1. Part of the signal layer 1
2. Middle Layer = GND area and RX lines

Figure 13. PN5190 Layout Reference middle layer example

Consider a proper heat sink for the lossy components like EMC filter inductors, damping resistors, and for PN5190.

3.3.2 PN5190 BGA power supply circuit recommendation

With the RF and antenna design, the power supply is important for the functionality and performance. The layout must be carefully designed for the DC-DC converter.

The PN5190 is optimized to support the EMVCo operating volume with 3.3 V input supply. The TX output can drive up to ITVDD = 350 mA. Based on a power supply voltage VDDPA = TVDD = 5.7 V, the total power consumption for the total antenna circuit is up to $P_{tot} \approx 2$ W.

The following guidelines are optimized for the standard use case, using the DC-DC for the VUP supply.

In that combination, the overall mean input current consumption at a supply voltage of 3.3 V can be up to 800 mA or higher. The rush-in current can be even higher.

VBATPWR, VDDBOOST, BOOST_LX

1. Place the components as close as possible to each other.
2. Route VBATPWR, BOOSTLX, VDDBOOST as short as possible.
3. Provide Cu shape. If shape is not possible, route with wide trace (150 mils).
4. No vias are allowed.
5. BOOST_LX is a noisy source. Sensitive signals should be far away from this net.

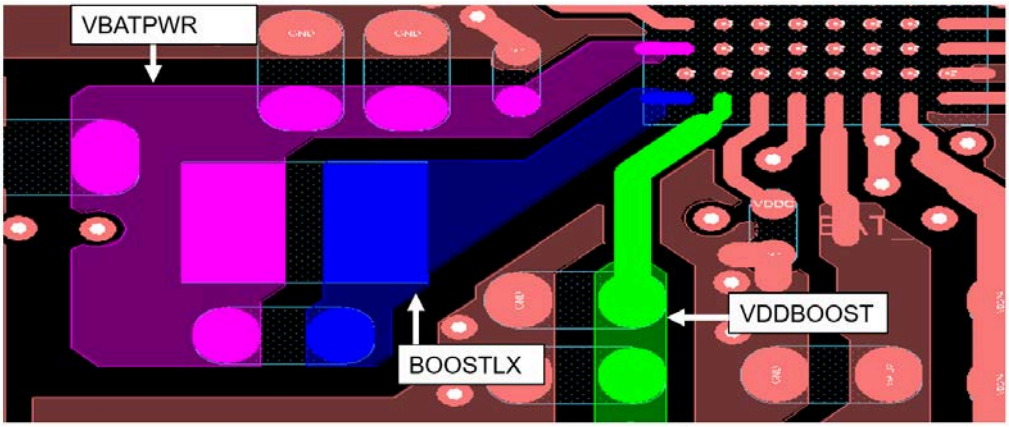


Figure 14. Layout example for VBATPWR, VDDBOOST, and BOOST_LX

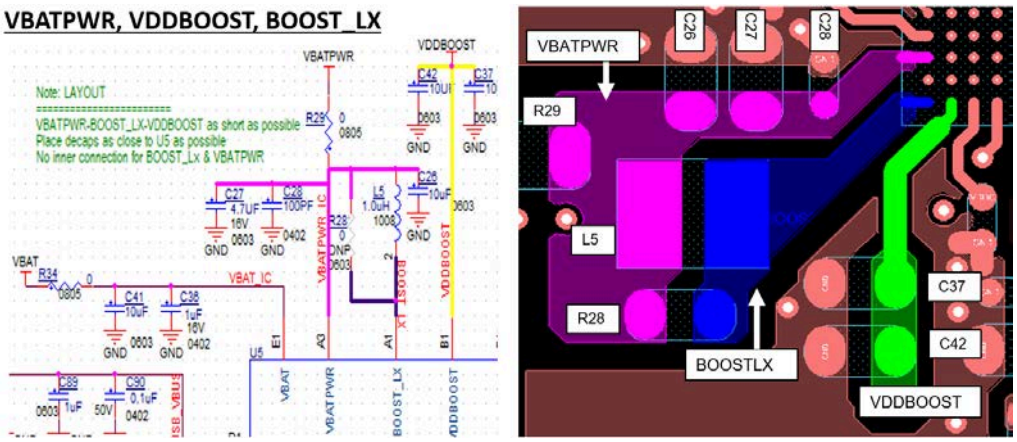


Figure 15. Layout example 2 for VBATPWR, VDDBOOST, and BOOST_LX

VDDNV:

- Place 0.22 µF capacitor as close as possible to VDDNV pad.
- Route with 10 mil width. No vias are allowed.

VDDC:

- Place 0.22 µF capacitor as close as possible to VDDC pad.
- Route with 10 mil width. No vias are allowed.

VDDPA:

- 100 pF + 4.7 µF capacitor must be as close as possible to VDDPA pads.
- Provide shape or a thicker trace width (30 mil or more).
- Avoid via.

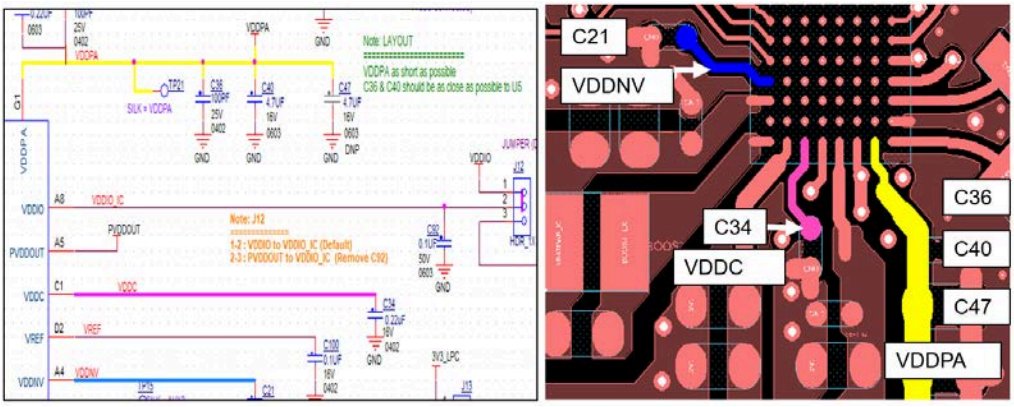
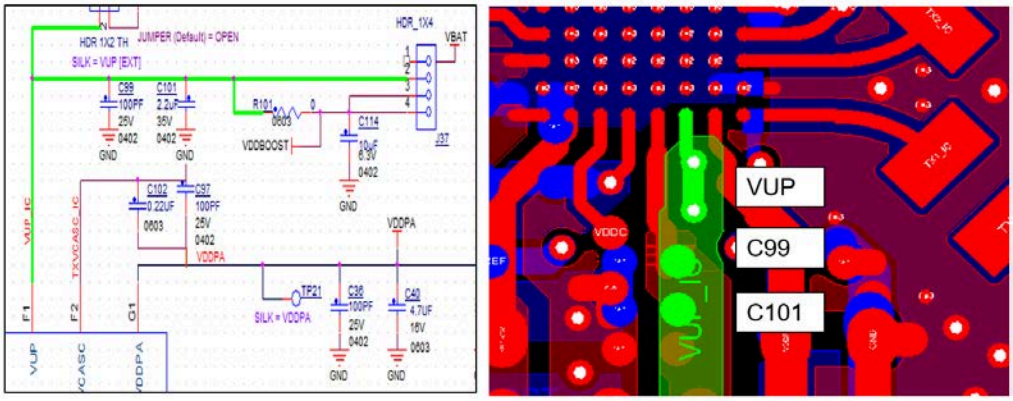


Figure 16. Layout example for VDDNV, VDDC, and VDDPA

VUP:

- Place the component as close as possible to VUP pad.
- Place the low-value capacitor close to the pin.
- Place the components on the same side of the chip.
- Provide Cu shape.



1. As there is no space on top side, here the related capacitors are placed on the bottom side.

Figure 17. Layout example for VUP

VREF:

1. Place 0.1 µF capacitor as close as possible to VREF pad.
2. Route with 20 mil trace width.

VMID:

1. Place the capacitor as close as possible to the pin.
2. Route with wide trace.

TXVCM:

1. Place the capacitor as close as possible to pin
2. Route with wide trace.

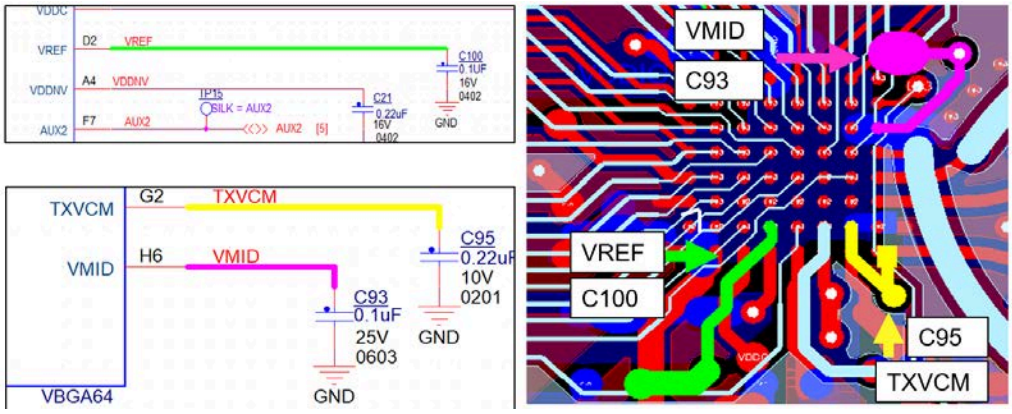


Figure 18. Layout example for VREF, VMID, and TXVCM

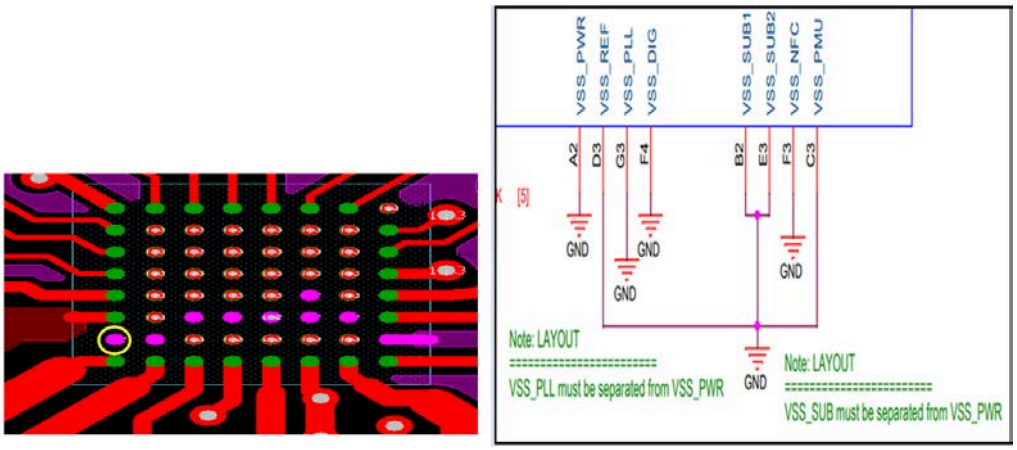
Table 1. Power supply design considerations

Keep the parasitic capacitance and inductance value lower than or equal to these values.

Net name	Parasitic capacitance	Parasitic inductance (BGA pin to first node)	Max VCC	Max ICC	Routing details
VDDBOOST	5.5 pF	0.41 nH	6 V	750 mA	Cu Shape
BOOST_LX	3.5 pF	0.19 nH	6 V	1900 mA	Cu Shape / thicker track width
VBATPWR	7.7 pF	0.56 nH	5.5 V	800 mA	Cu Shape
VDDC	1.5 pF	0.88 nH	1.14 V	30 mA	10 mil width
VDDNV	1.0 pF	0.98 nH	2.2 V	150 mA	10 mil width
VDDPA	1.8 pF	0.26 nH	6 V	750 mA	Cu Shape
VUP	8.1 pF	0.68 nH	6 V	750 mA	Cu Shape
VREF	—	—	0.9 V	1 mA	Thicker track width
VMID	—	—	1.8 V	20 mA	Thicker track width
TXVCM	—	—	3 V	20 mA	Thicker track width

3.3.3 PN5190 BGA GND design recommendation

VSSPWR:



1. Drop a separate via for VSS_PWR to GND and do not share with any other pin

Figure 19. Layout example for the VSS_PWR

VSS_SUB:

- Separate VSS SUB from VSS_PWR.
- Drop a via and connect to GND plane.
- If it is not possible to connect to GND plane directly, route to VSS-PMU pin or to VSS-REF pin, and drop a via (Figure 20).

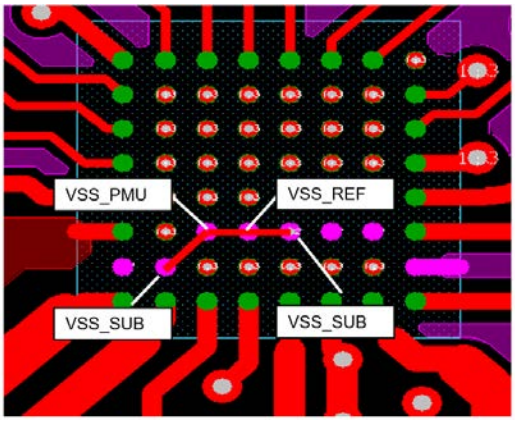


Figure 20. Layout example for VSS_SUB, VSS_PMU, and VSS_REF

VSS_PLL:

- Connect VSS_PLL to GND plane.
- Do not share VSS_PLL with any GND pin of the BGA.

VSS_DIG:

- Connect VSS_DIG to GND plane.
- Do not share VSS_DIG with any GND pin of the BGA.

VSS_NFC:

- Connect VSS_NFC to GND plane.
- Do not share VSS_NFC with any GND pin of the BGA.

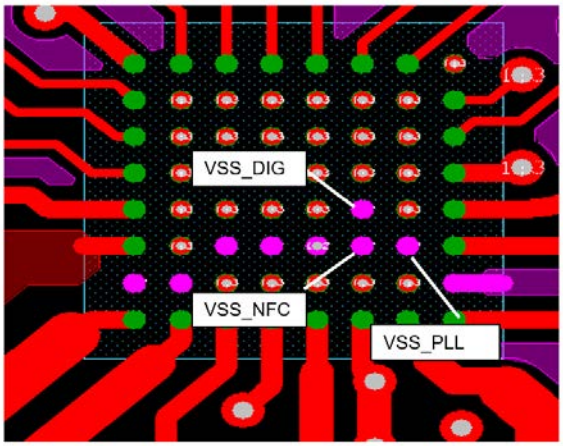


Figure 21. Layout example for the VSS_PLL, VSS_DIG, and VSS_NFC

Table 2. GND design considerations

VSS routing guidance

Net Name	Max ICC	Routing details	Comments
VSS_PWR	1900 mA	Connect directly to GND plane	
VSS_SUB	10 mA	Connect directly to GND plane	Can be shared with VSS_REF and VSS_PMU
VSS_REF	1 mA	Connect directly to GND plane	Can be shared with VSS_SUB and VSS_PMU
VSS_PMU	100 mA	Connect directly to GND plane	Can be shared with VSS_SUB and VSS_REF
VSS_PLL	20 mA	Connect directly to GND plane	
VSS_DIG	30 mA	Connect directly to GND plane	
VSS_NFC	35 mA	Connect directly to GND plane	
VSS_PA	400 mA	Connect directly to GND plane	

3.3.4 PN5190 BGA clock design recommendation

Clock:

- Place Xtal and the associated components as close as possible to the PN5190.
- Keep traces as close as possible to each other, and keep the length equal.
- Keep the load capacitance close to the crystal.
- Isolate the crystal away from all other signals
- Avoid vias.
- Provide proper GND isolation to avoid noise.

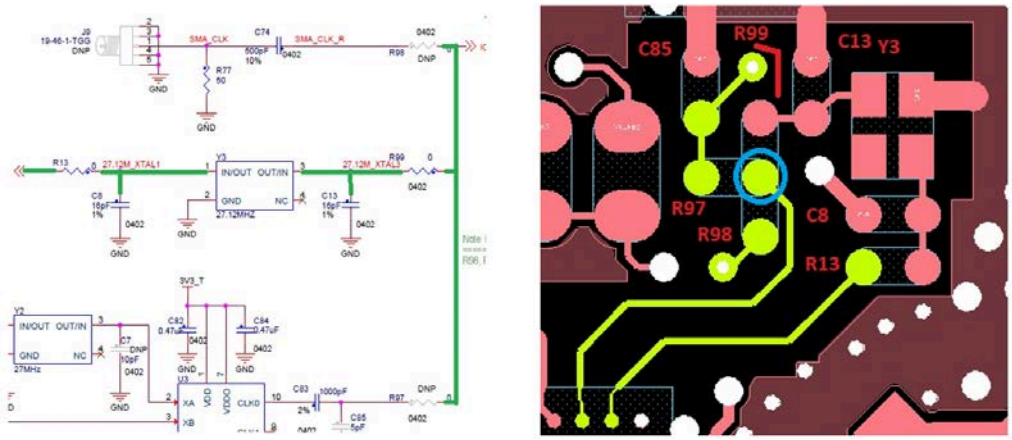


Figure 22. Layout example for the Clock

3.3.5 PN5190 supply capacitors

The choice of capacitance and the placement of the block capacitors influence the performance of the PN5190.

The PNEV5190BP (refer to [20]) and module board can be used as reference. Stick to the given values of capacitors. Larger capacitance values can cause higher rush-in current and/or analog misbehavior. Smaller capacitance values can cause extra noise and decrease the analog performance.

VDBOOST and VUP:

VDDBOOST uses a 22µF capacitor to GND (22 µF 25V 20 % X5R 0805: Murata GRM21BR61E226ME44) and is connected to VUP, which uses a 4.7µF capacitor (4.7 µF 10V 10% X5R 0402: TDK C1005X5R1A475K050BC).

VBATPWR:

VBATPWR uses a 4.7µF capacitor (4.7 µF 10V 10 % X5R 0402: TDK C1005X5R1A475K050BC).

VBAT:

VBAT uses a 4.7µF capacitor (4.7 µF 10V 10% X5R 0402: TDK C1005X5R1A475K050BC).

Note: *Be aware of capacitance bias characteristics, as illustrated in Figure 23 copied from Murata specification [21].*

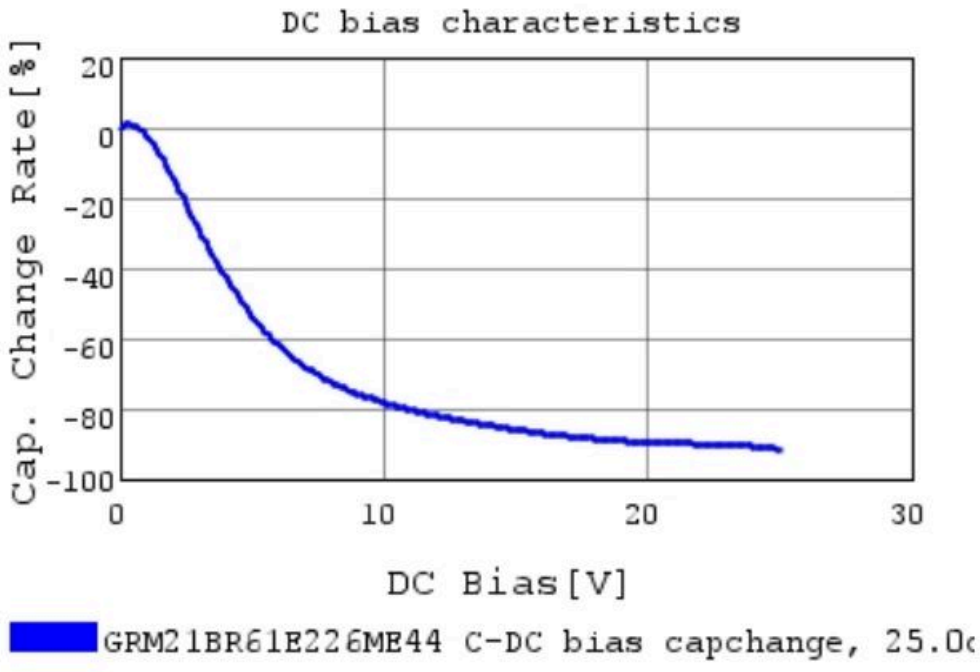


Figure 23. Murata: Capacitance Bias characteristics of X5R

Note: *The routing of VBAT and VBATPWR is important to avoid wrong DC-DC synchronization. Even though VBAT and VBATPWR are supplied from the same source, a separate routing including separate block capacitors to GND is required. The wrong routing of VBAT and VBATPWR can cause an extra RX noise level on specific VDDPA settings.*

3.4 Layout recommendation for VFLGA40

To ensure performance and comply with CE, FCC, or MIC regulations, the basic analog design must be kept. The following sections provide recommendations and show which parts of the design are most critical in terms of layout.

The RF circuit, the antenna circuit, and the power supply are the main parts to consider.

3.4.1 PN5190 VFLGA40 RF circuit recommendations

Layout recommendations for the PN5190 in VFLGA40:

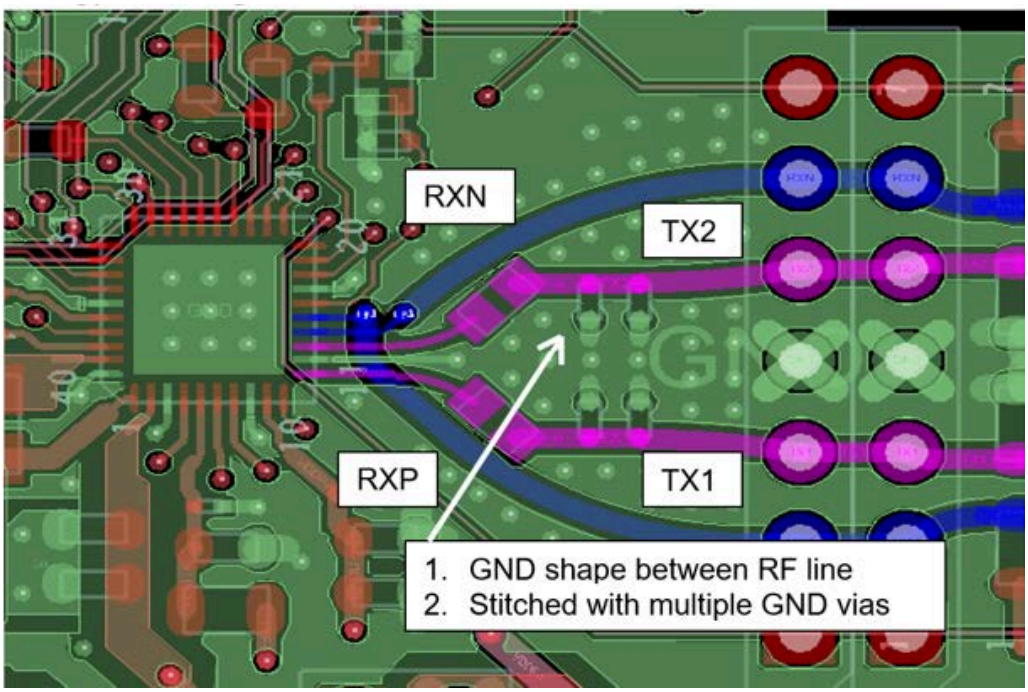
1. Place components as close as possible to the IC.
2. Place two inductors L0 close to each other, either perpendicularly or at a 45-degree angle.
3. Place the capacitor of the RX line close to PN5190.
4. For a shorter TX line, place the inductor L0 very close to PN5190.

Guidelines for the routing:

1. Route TX line in Top Layer (due to huge current).
2. Depending on the matching network and antenna placement, route RX line in Top Layer (if possible) or in Layer 3 (internal signal Layer 1).
3. Do not use any via for TX Line.
4. Use blind Via for the RX line.
5. Route with any angle routing. No 90 degree/45 degree or odd angle bends are required.
6. RX and TX lines must be routed with GND separation (avoid cross-talking).
7. Route TX lines symmetrical to each other. And route RX lines symmetrical to each other.

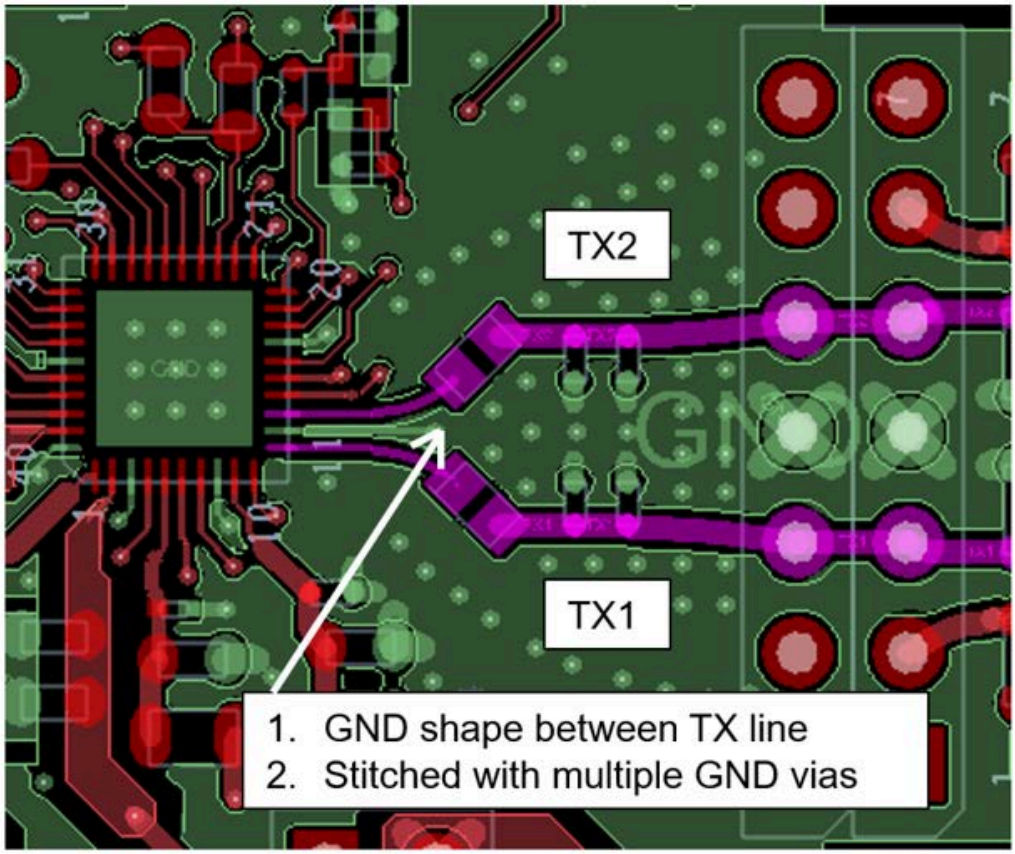
The GND layer is an important part of the layout (see Figure 12).

1. Provide solid GND plane on adjacent layer (L2_GND).
2. Fill all layers with GND shape.
3. Stitch with multiple GND via around RF line.
4. No Test point is allowed.
5. No silk label on RF traces.



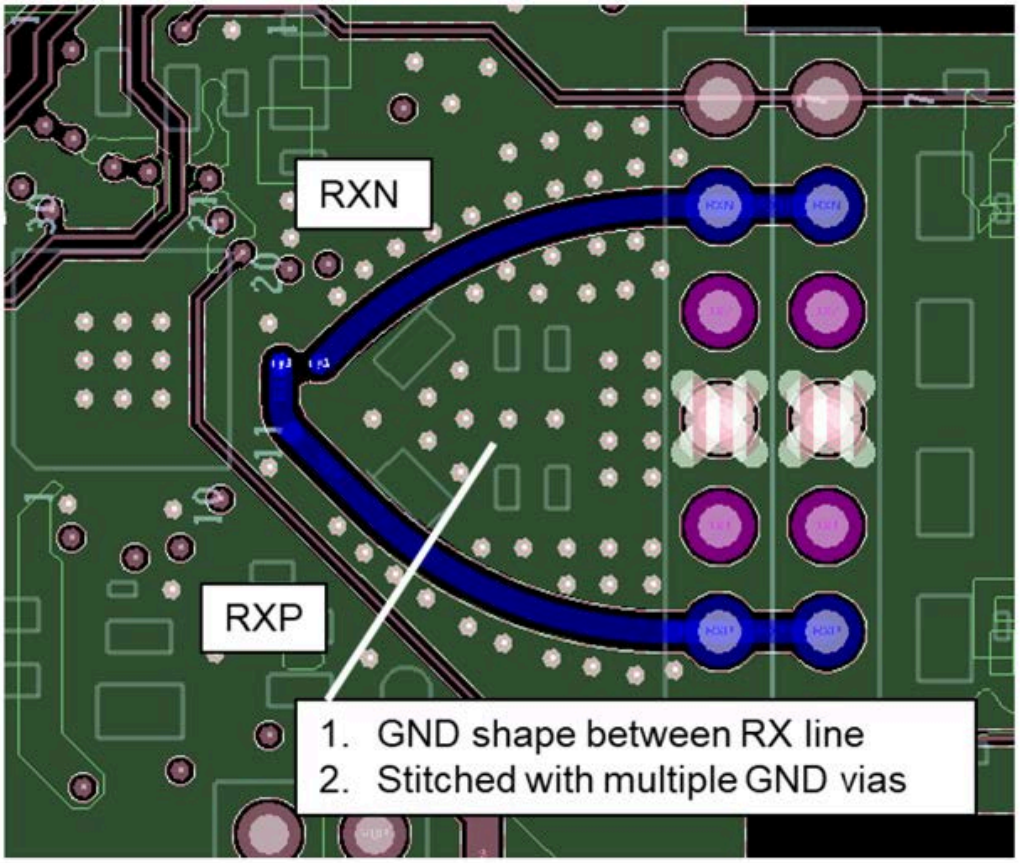
1. Screenshot with multiple layers

Figure 24. PN5190 VFLGA40 layout reference example



1. Screenshot with multiple layers

Figure 25. PN5190 VFLGA40 TX layout reference example



1. Screenshot with multiple layers

Figure 26. PN5190 VFLGA40 RX layout reference example

Consider a proper heat sink for the lossy components like EMC filter inductors, damping resistors, and for the PN5190.

3.4.2 PN5190 VFLGA40 power supply circuit recommendation

With the RF and antenna design, the power supply is important for the functionality and performance. The layout must be carefully designed for the DC-DC converter.

The PN5190 is optimized to support the EMVCo operating volume with a 3.3 V input supply. The TX output can drive up to ITVDD = 350 mA. Based on a power supply voltage VDDPA = TVDD = 5.7 V, the total power consumption for the total antenna circuit is up to $P_{tot} \approx 2$ W.

The following guidelines are optimized for the standard use case where DC-DC is used for the VUP supply.

In that combination, the overall mean input current consumption at a supply voltage of 3.3 V can be up to 800 mA or higher. The rush-in current can be higher.

VBATPWR, VDDBOOST, BOOST_LX

1. Place components as close as possible to each other.
2. Route VBATPWR, BOOSTLX, VDDBOOST as short as possible.
3. Provide Cu shape. If shape is not possible, route with a wide trace (150mils).
4. No vias are allowed.
5. BOOST_LX is a noisy source. Keep sensitive signals far from this net.

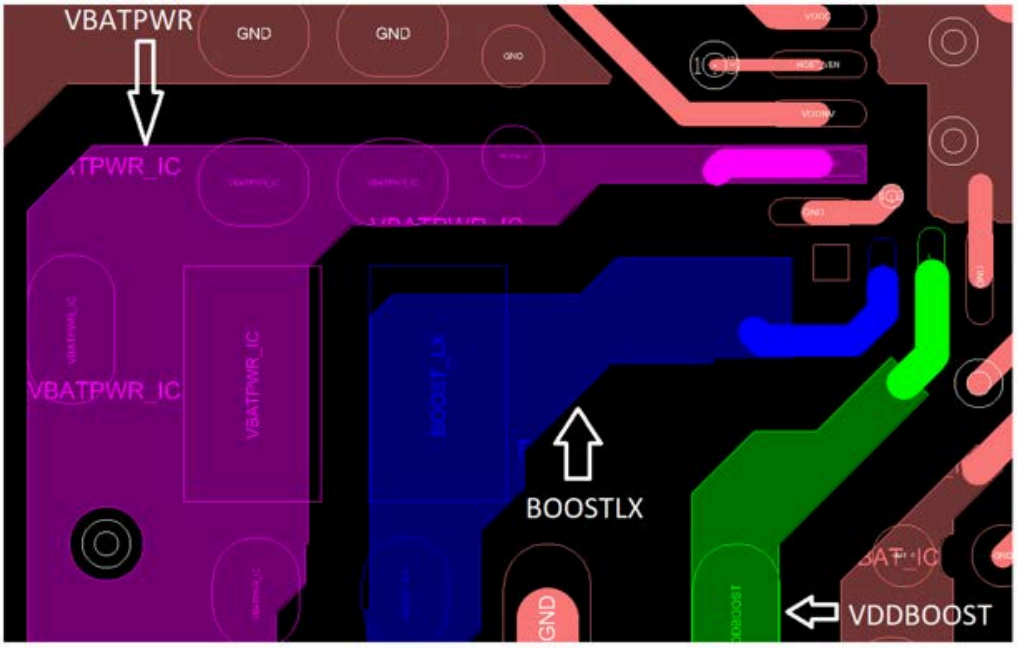


Figure 27. PN5190 VFLGA40 layout example for VBATPWR, VDDBOOST, and BOOST_LX

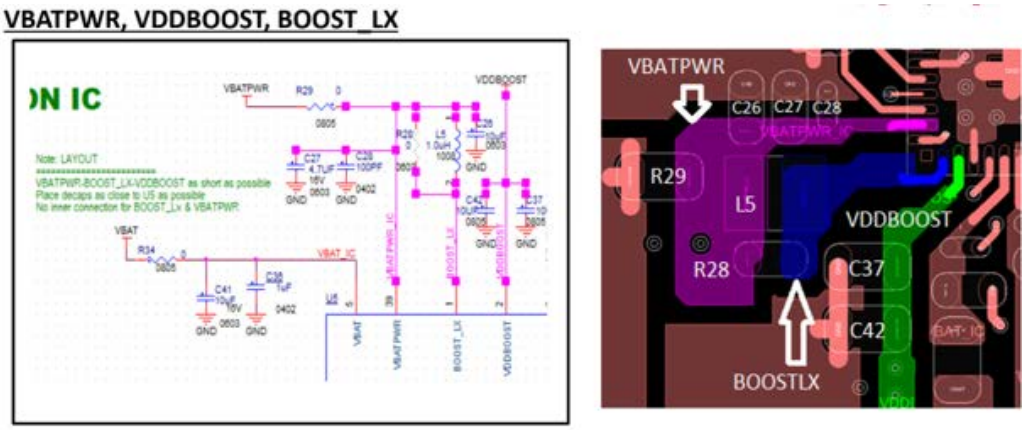


Figure 28. PN5190 VFLGA40 layout example 2 for VBATWPR, VDDBOOST, and BOOST_LX

VDDNV:

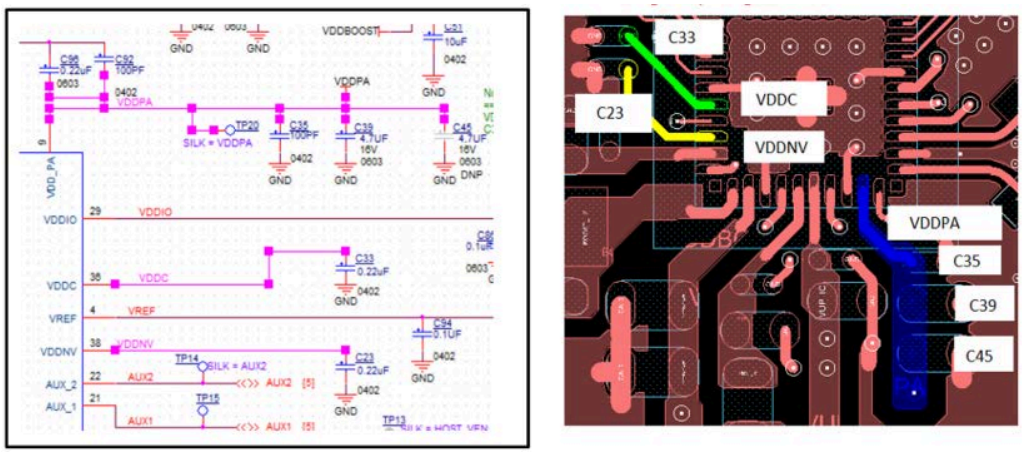
- Place a 0.22 µF capacitor as close as possible to VDDNV pad.
- Route with 10 mil width. No vias are allowed.

VDDC:

- Place a 0.22 µF capacitor as close as possible to VDDC pad.
- Route with 10 mil width. No vias are allowed.

VDDPA:

- Place 100 pF and 4.7 µF capacitors as close as possible to VDDPA pads.
- Provide shape or thicker trace width (30 mil or more).
- Try to avoid via.

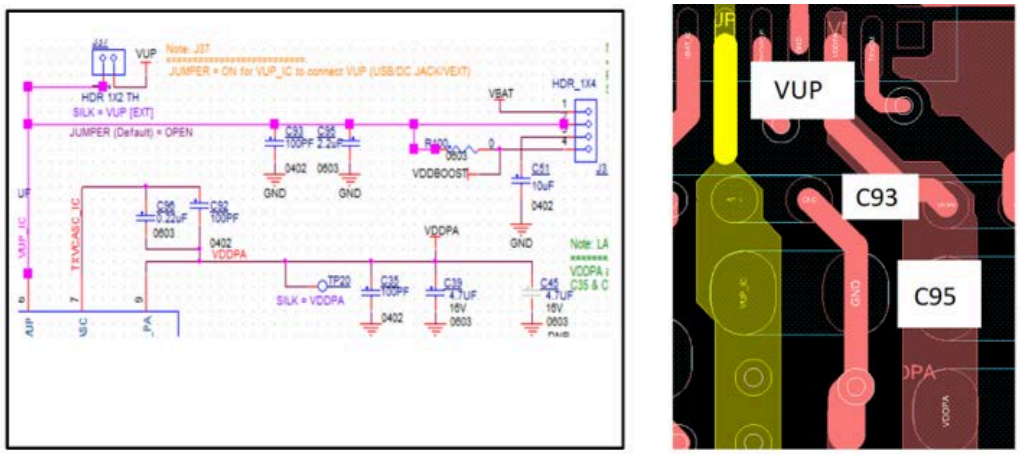


1. Screenshot with multiple layers

Figure 29. PN5190 VFLGA40 layout example for VDDNV, VDDC, and VDDPA

VUP:

- Place the component as close as possible to VUP pad.
- Place the low-value capacitor close to the pin.
- Place the components on the same side of the chip (if possible).
- Provide Cu shape.



1. Screenshot with multiple layers

Figure 30. PN5190 VFLGA40 layout example for VUP

VREF:

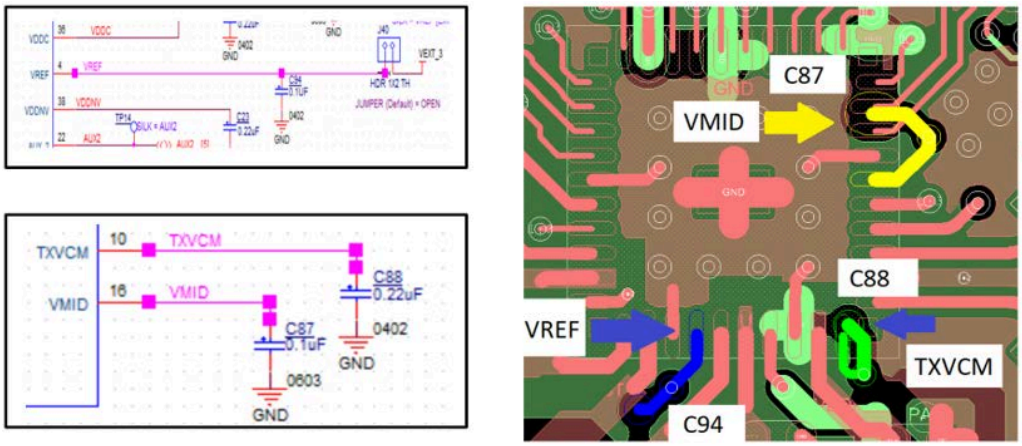
1. Place a 0.1 µF capacitor as close as possible to VREF pad.
2. Route with 20 mil trace width.

VMID:

1. Place the capacitor as close as possible to the pin.
2. Route with wide trace.

TXVCM:

1. Place the capacitor as close as possible to the pin.
2. Route with wide trace.



1. Screenshot with multiple layers

Figure 31. PN5190 VFLGA40 layout example for VREF, VMID, and TXVCM

Table 3. PN5190 VFLGA40 power supply design considerations

Keep the parasitic capacitance and inductance value lower than or equal to these values.

Net name	Parasitic capacitance	Parasitic inductance (BGA pin to first node)	Max VCC	Max ICC	Routing details
VDDBOOST	3.6pF	0.21nH	6V	750mA	Cu Shape
BOOST_LX	5.0pF	0.30nH	6V	1900mA	Cu Shape/thicker track width
VBATPWR	1.6pF	0.20nH	5.5V	800mA	Cu Shape
VDDC	0.6pF	0.71nH	1.14V	30mA	10 mil width
VDDNV	0.7pF	0.82nH	2.2V	150mA	10 mil width
VDDPA	0.6pF	0.54nH	6V	750mA	Cu Shape
VUP	0.6pF	0.54nH	6V	750mA	Cu Shape
VREF	0.4pF	0.45nH	0.9V	1mA	Thicker track width
VMID	0.6pF	0.55nH	1.8V	20mA	Thicker track width
TXVCM	0.4pF	0.55nH	3V	20mA	Thicker track width

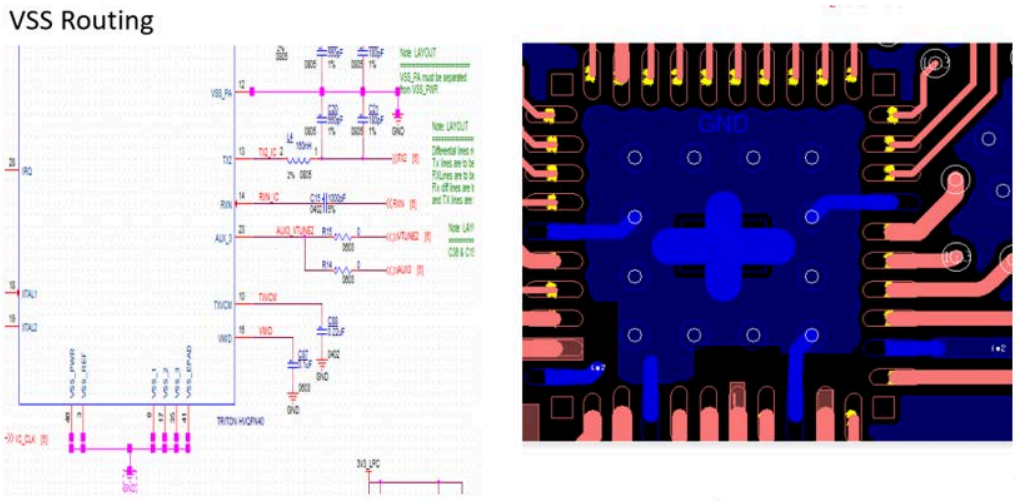
3.4.3 PN5190 VFLGA40 GND design recommendations

VSSPWR:

Table 4. PN5190 VFLGA40 VSS routing

VSS routing guidance

Net name	Max ICC	Routing details
VSSPWR	1900 mA	Drop separate via to GND
VSSREF	1 mA	Connect directly to GND plane
VSSPA	400 mA	Connect directly to GND plane
VSS_EPAD	—	Fill copper shape and place vias



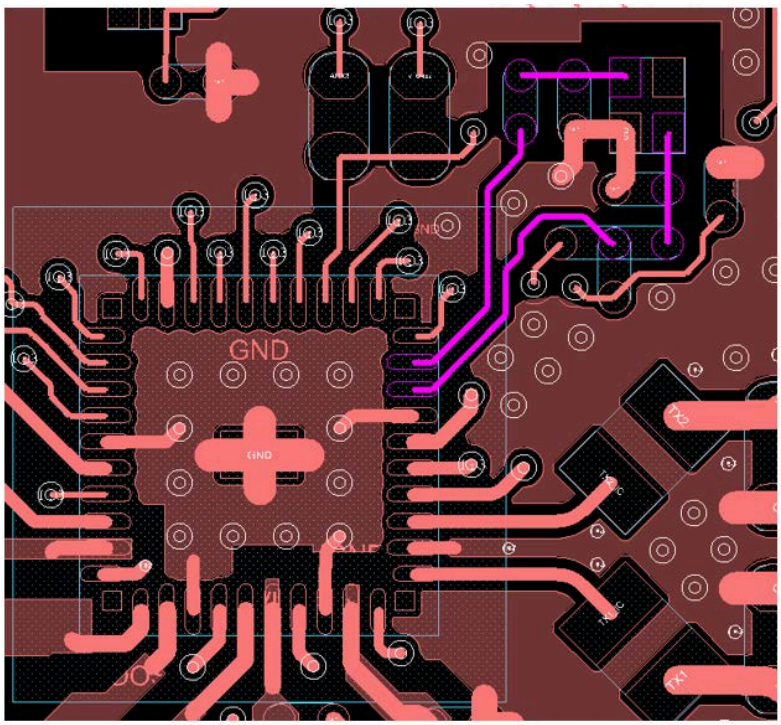
1. Screenshot with multiple layers

Figure 32. PN5190 VFLGA40 layout example for VSS

3.4.4 PN5190 VFLGA40 clock design recommendations

Clock:

- Place Xtal and the associated components as close as possible to the PN5190.
- Keep traces as close as possible to each other, and keep the length equal.
- Keep the load capacitance close to the crystal.
- Isolate the crystal away from all other signals.
- Avoid vias.
- To avoid noise, insulate GND.



1. Screenshot with multiple layers

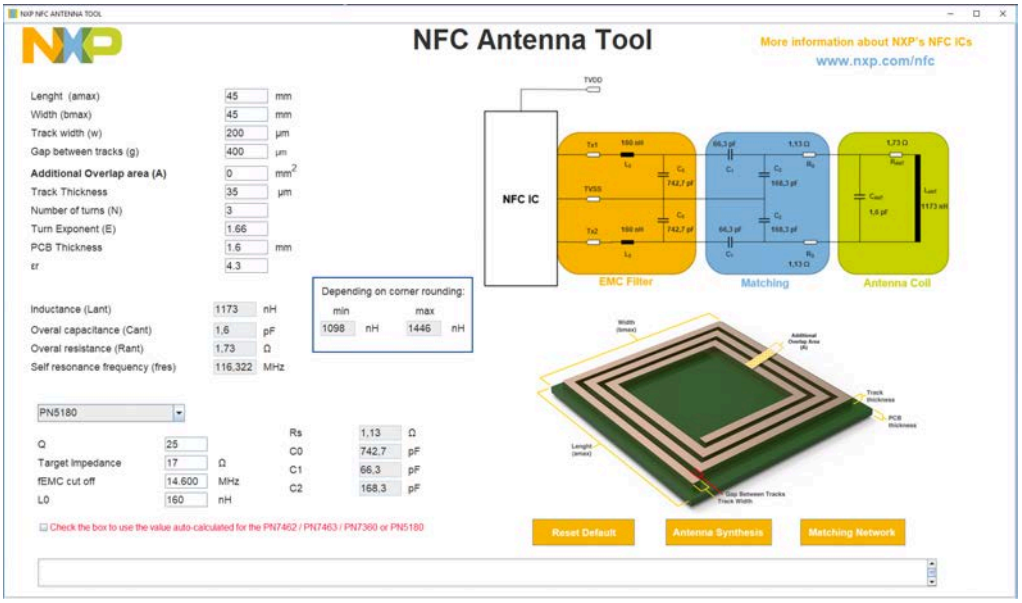
Figure 33. PN5190 VFLGA40 layout example for the clock

4 PN5190 antenna tuning

The following description focuses on the PCD antenna for the PN5190.

4.1 NFC antenna tool

If no other starting point is available, use the NXP NFC antenna design tool on the NFC Antenna Hub (see [11] and Figure 34).



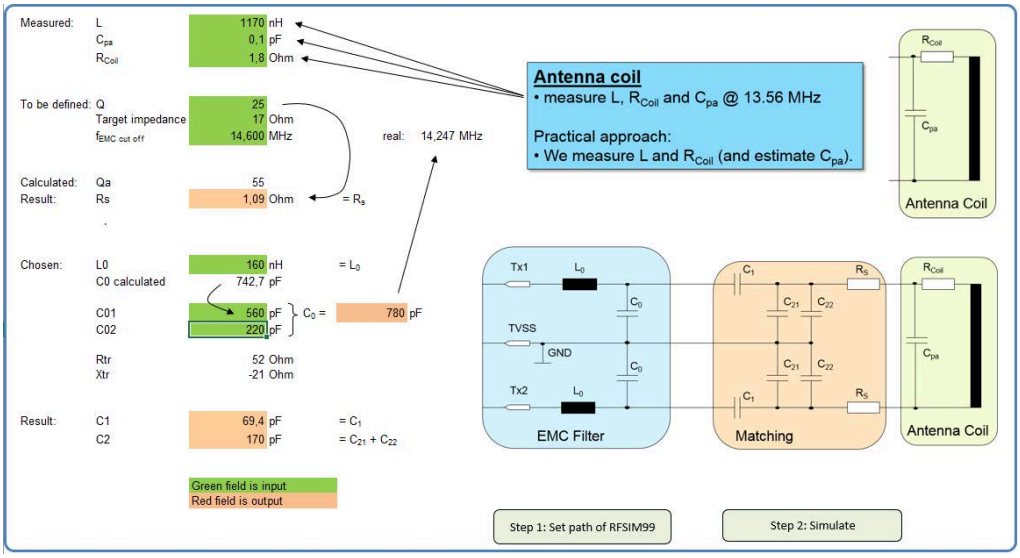
1. Choose the PN5180 as a starting point.

Figure 34. NFC Antenna Tool example

Use the PN5180 as NFC reader IC for the starting value. Change the target impedance to a lower value, for example 17 Ω. For EMC filter inductor, choose 160 nH.

4.2 Antenna tuning calculation Excel sheet

As for the PN5180 or any other NXP NFC reader ICs, use the Excel sheet as an alternative for the antenna calculation. The same example as for Section 4.1 is used in Figure 35.



1. This example is showing the same tuning values as the NFC Antenna Tool, see [18]

Figure 35. Antenna calculation excel sheet example

For a 45 mm x 45 mm antenna with three turns the antenna synthesis returns:

L = 1.17 µH

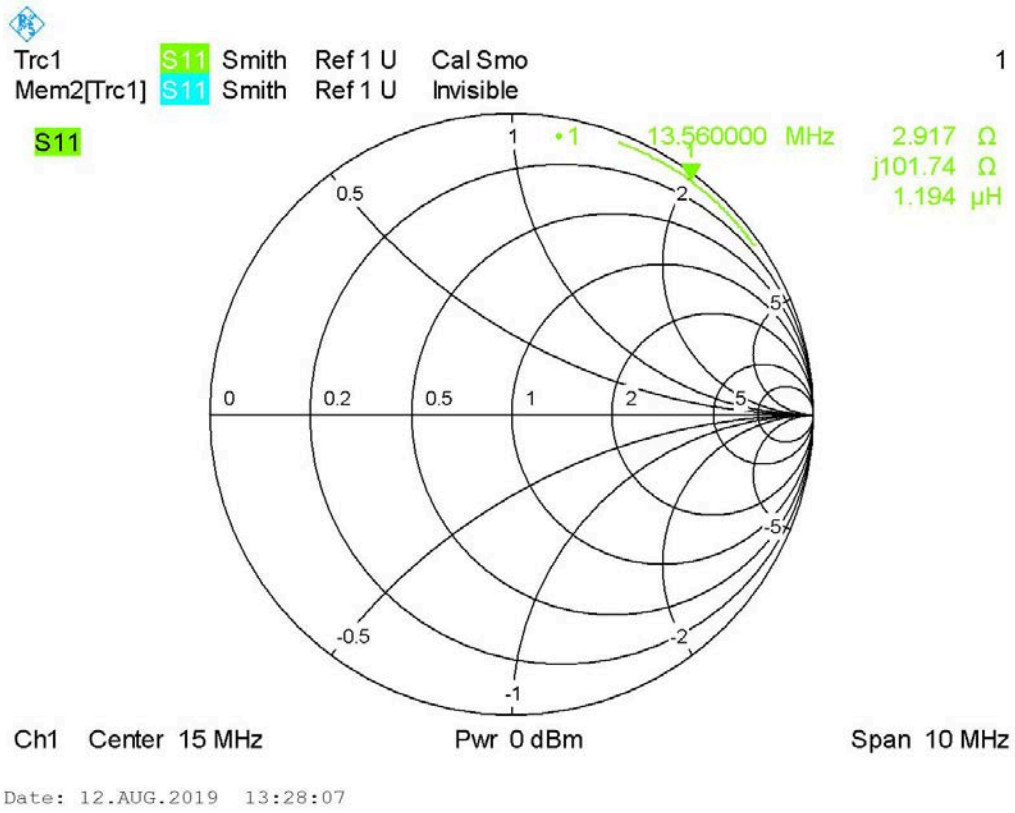
R_{Coil} = 1.7 Ω

For the antenna coil, use input values from a simple measurement rather than only from the antenna synthesis. The antenna coil measurement is required to derive accurate values for the inductance L, the resistance R_{Coil}, and the capacitance C_{pa}.

Use the VNA to measure the impedance $\underline{Z}$ of the antenna coil at 13.56 MHz and to calculate L and R.

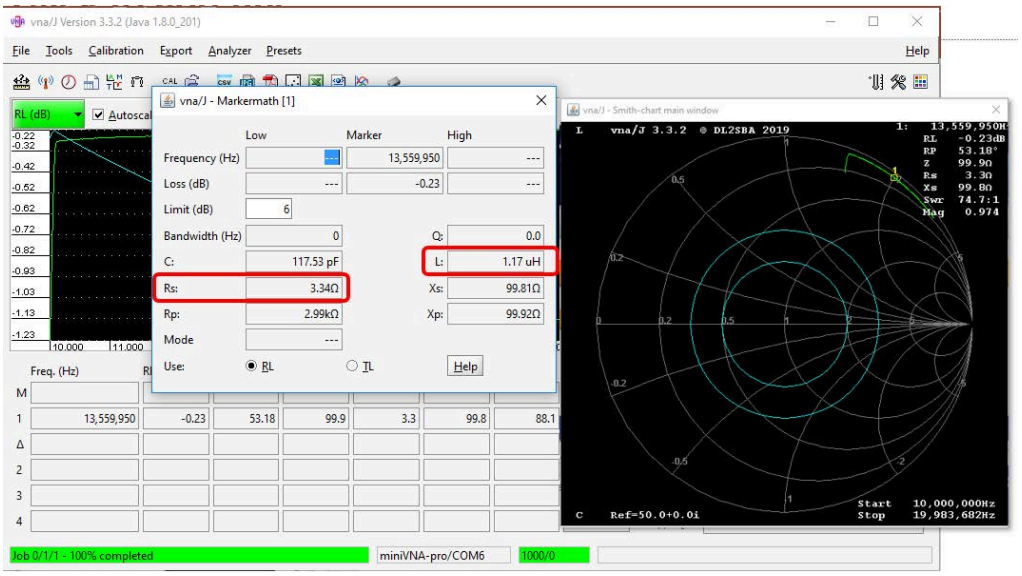
$$\underline{Z} = R + j\omega L_{Coil}$$

The VNA directly shows the L and R, as shown in Figure 36 and Figure 37.



1. Measured with Rohde & Schwarz ZVL (see [7])
2. L = 1.19 µH, R = 2.9 Ω

Figure 36. Antenna coil measurement example 1



1. Measured with minVNA Pro and VNA/J (see [8] and [10])

Figure 37. Antenna coil measurement example 2

In this example, the antenna coil is measured with:

L = 1.17 µH to 1.19 µH

R_{Coil} ≈ 2.9 Ω to 3.3 Ω

C_{pa} = not measured, can be estimated.

The inductance can be measured with accuracy. But the resistance cannot, because of the relation between R and jωL. And the capacitance is not measured at all with this simple measurement.

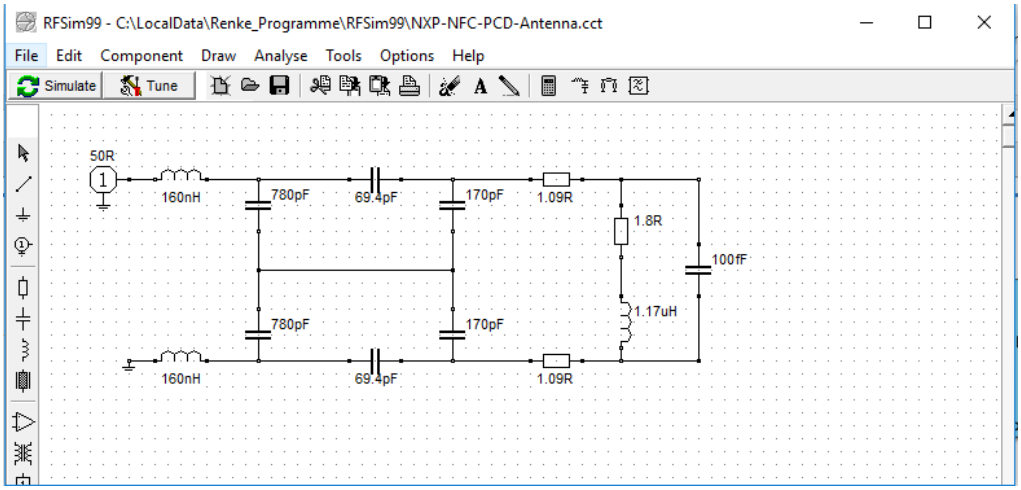
There are several ways to improve the accuracy and even further derive the capacitance, but these simple results are enough to start the tuning procedure. The tuning procedure is required, but there is no need to spend more effort in measuring more accurate antenna coil parameters.

Note: *You can adapt the Q in the Excel sheet calculation so the value of the calculated damping resistor R_Q is within an E-series of values. That is, 2.7 Ω or 3.3 Ω, but not 2.845 Ω. In this case, the following calculation is more accurate. That is, the result from the calculation and simulation is closer to the measured result.*

If the RFSIM99 is used, the next step is the simulation of the antenna circuit.

4.3 Antenna circuit simulation

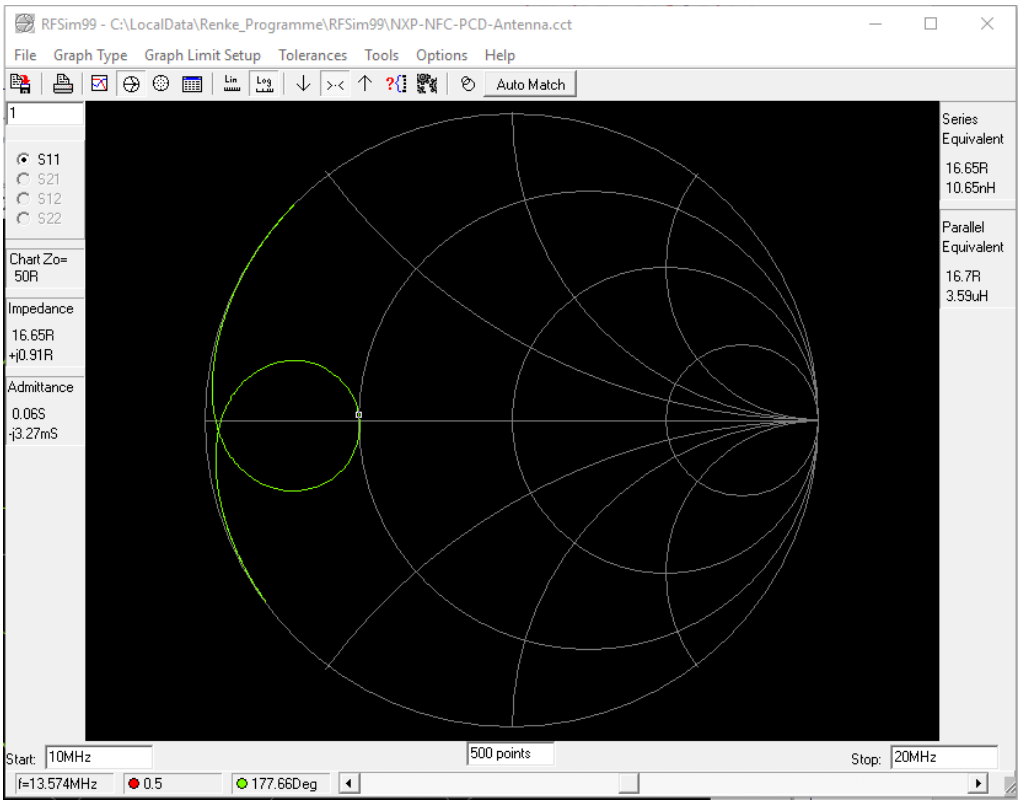
The Excel sheet calculation provides a macro function that writes the simplified netlist for the simulation tool RFSIM99 (see [9]). RFSIM99 starts automatically as shown in Figure 38.



1. This circuit uses ideal components!

Figure 38. Circuit derived from the calculation

The impedance plot (smith chart) in Figure 39 shows the related impedance from 10 MHz to 20 MHz. The marker at (or closest to) 13.56 MHz indicates the antenna impedance at the operating frequency.



1. This circuit uses ideal components!

Figure 39. RFSIM99 smith chart plot

Use the simulation to fine-tune the circuit with realistic components:

1. Fit the values into the given E-series. For example, Example: C2 = 180 pF instead of C2 = 197.2 pF in parallel to 18 pF.
2. The ideal inductor in the simulation indicates no losses: a first measurement reveals that the value is not realistic. Add 1 Ω to 3 Ω per inductor.

4.4 How to interpret the smith chart

The smith chart is a well-used tool to indicate S-Parameters. The S11 simulation and measurement fit perfectly into the antenna tuning procedure, but understanding the mechanisms of the NFC Antenna circuit tuning can be useful.

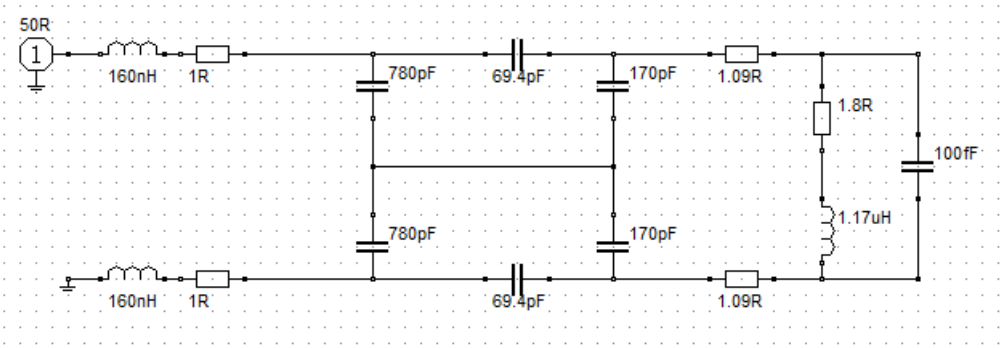
Note: *You can check the effect of the mechanisms with the RFSIM99.*

4.4.1 Smith chart: Inductor losses

The biggest effect in terms of losses (besides the damping resistors) comes from the EMC filter inductors. The simple circuit from the calculation uses ideal components, i.e. it does not take any inductor losses at all into account.

So the first step for the simulation is to add those losses. Instead of using a physical model of a real inductor, the Figure 40 shows the circuit including manually added losses.

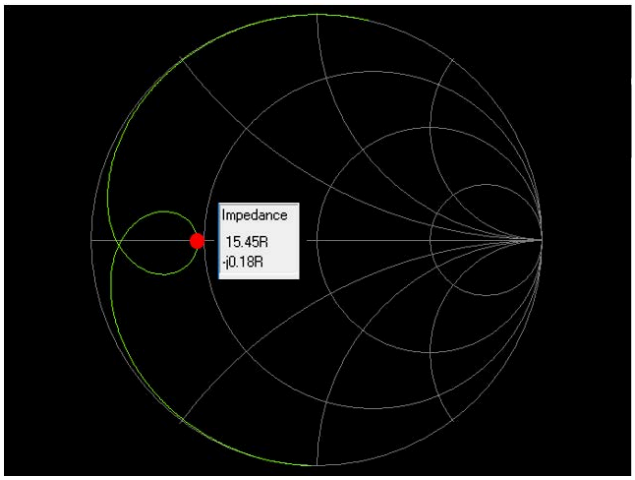
That example indicates losses of 1 Ω per inductor (at the operating frequency, which is quite realistic).



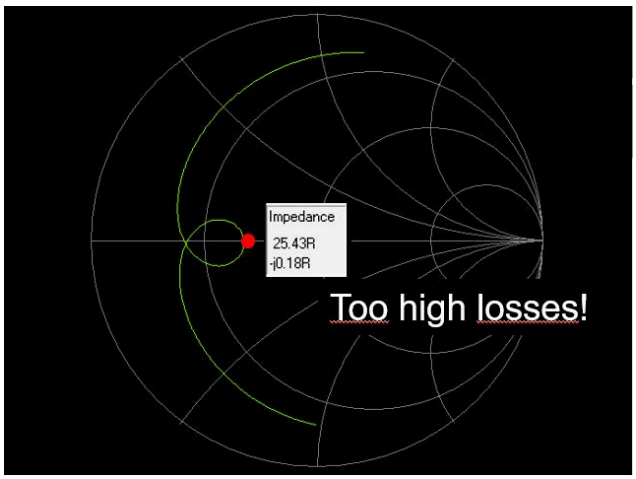
1. The L0 inductor (real component) contains losses, which are manually added.

Figure 40. Circuit derived from the Calculation including losses

The impact of those losses can be directly seen in the smith chart as shown in principle in Figure 41.



Ideal L0, no losses

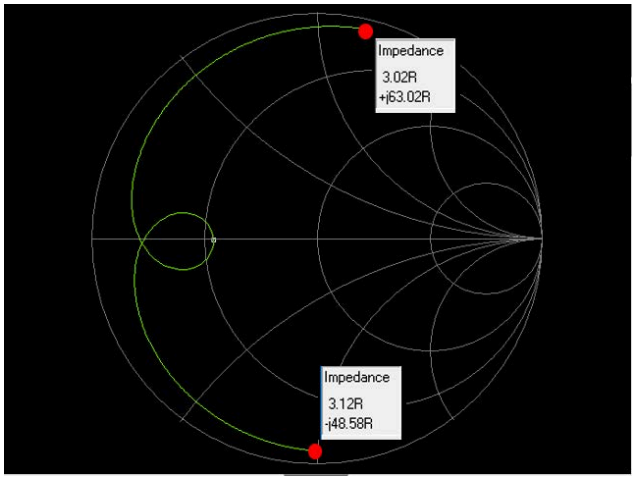


Bad L0 with 5 Ω losses at 13.56 MHz

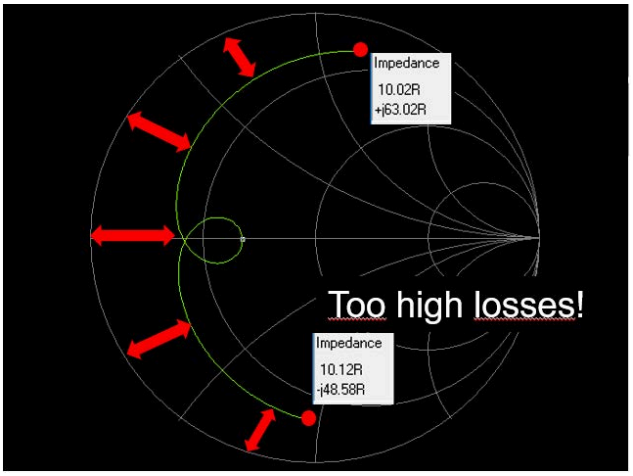
Figure 41. Impedance comparison with and without losses

Even further, the losses can be directly measured within this circuit, when moving the measurement marker to its ends, either to 10 MHz or to 20 MHz, as shown in Figure 42.

The marker directly shows the added losses of the two inductors, since all other components are either loss-free (capacitors) or do not count at these frequencies (damping resistor or antenna coil losses). So the real part of the S11 (ignore the reactive part) in Ω shows the losses of the series of the two L0.



Good L0 with R = 1.5 Ω

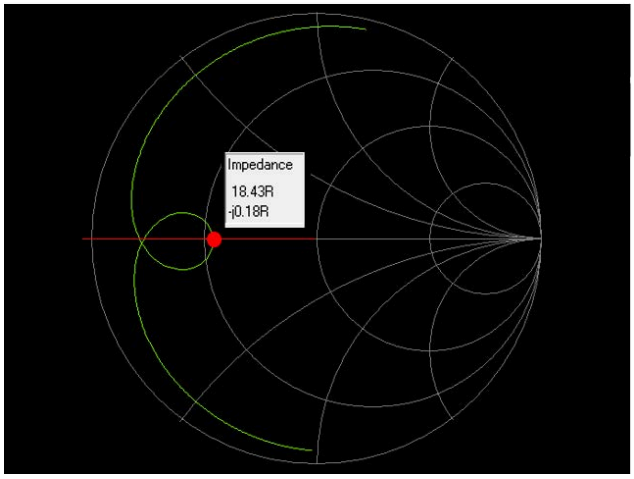


Bad L0 with R = 5 Ω

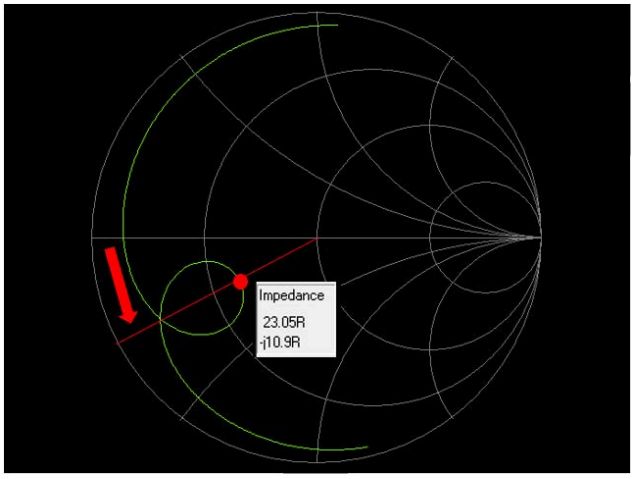
Figure 42. Measure the inductor loss

4.4.2 Smith chart: C0

The impact of the value of C0 (EMC filter capacitor) can also be read from the smith chart, as indicated in Figure 43 and Figure 44.

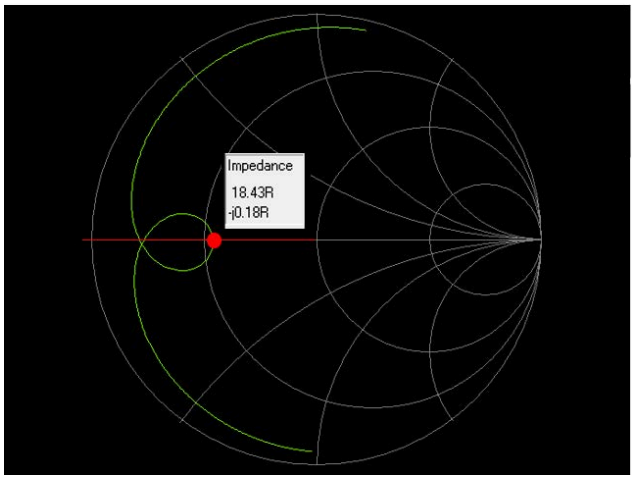


C0 ok, Cut off frequency ok

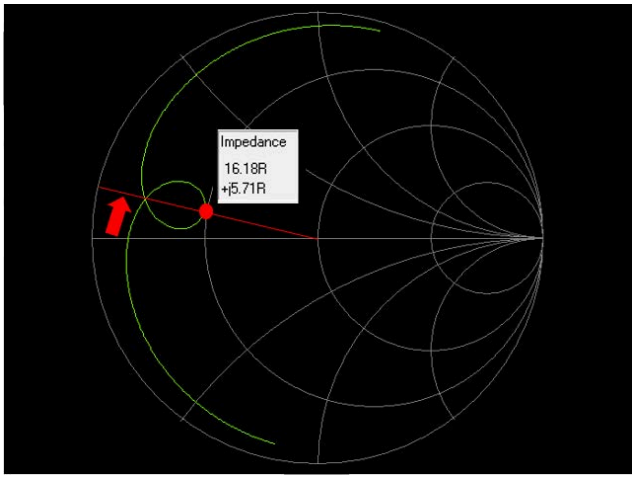


C0 too low, Cut off frequency too high

Figure 43. Smith chart: C0 too low



C0 ok, Cut off frequency ok

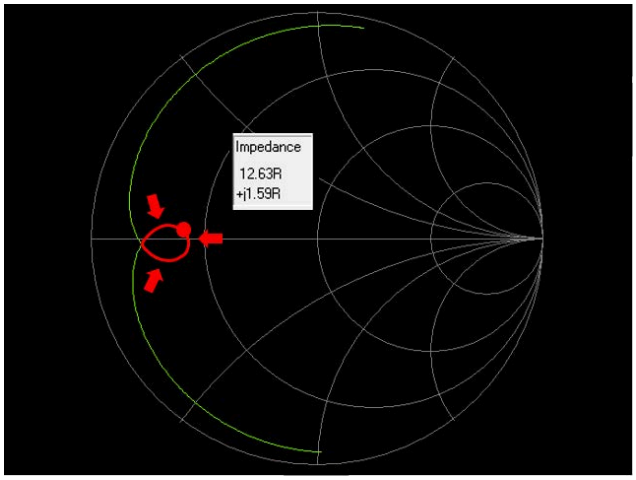


C0 too high, Cut off frequency too low

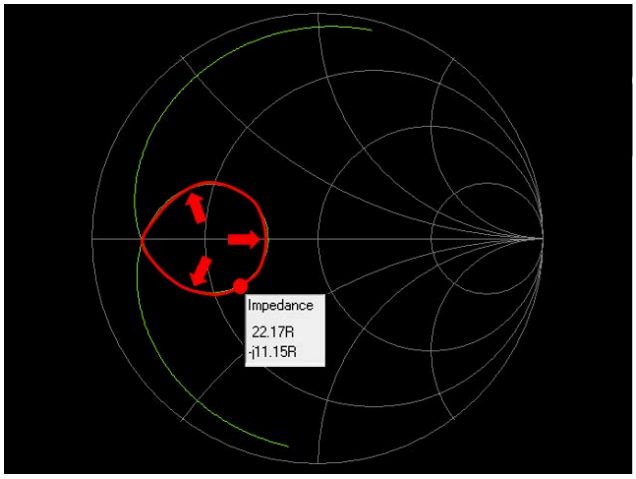
Figure 44. Smith chart: C0 too high

4.4.3 Smith chart: C1

The effect of C1 can also be estimated from the smith chart, as shown in Figure 45.



C1 too low, impedance too low

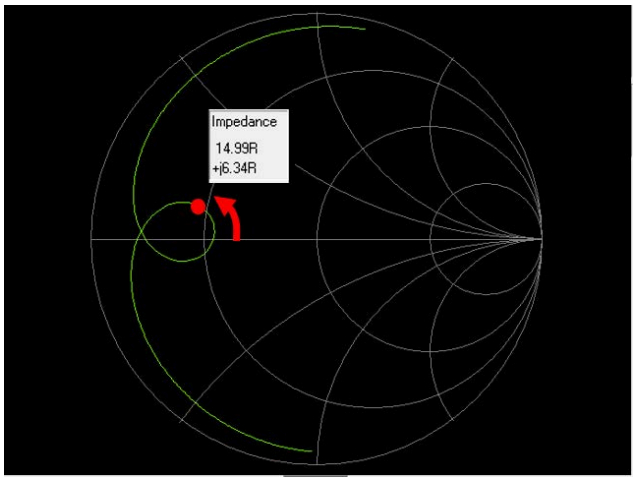


C1 too high, impedance too high

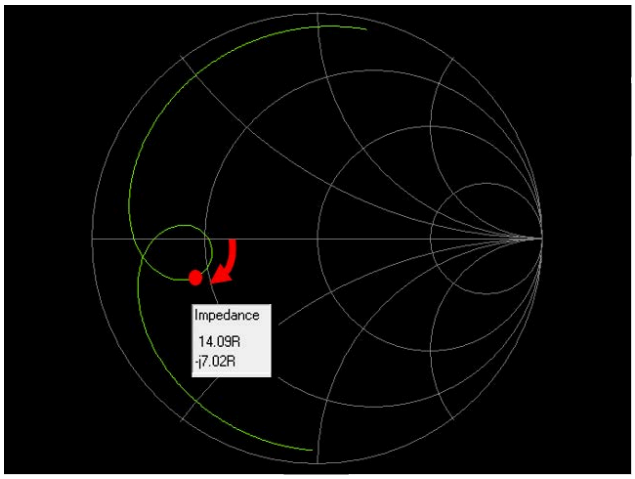
Figure 45. Smith chart: impact of C1

4.4.4 Smith chart: C2

Estimate the effect of C2 from the smith chart, as shown in Figure 46.



C2 too low, impedance too inductive



C2 too high, impedance too capacitive

Figure 46. Smith chart: impact of C2

4.5 Correction of the simulated circuit

Based on the measured inductance and resistance value of the antenna, the basic tuning circuit is derived (see Section 4.2 and Section 4.3). After adding the realistic losses of L0 (see Figure 40), now the capacitance values are modified into realistic values.

C0 = 780 pF are replaced with 560 pF || 220 pF

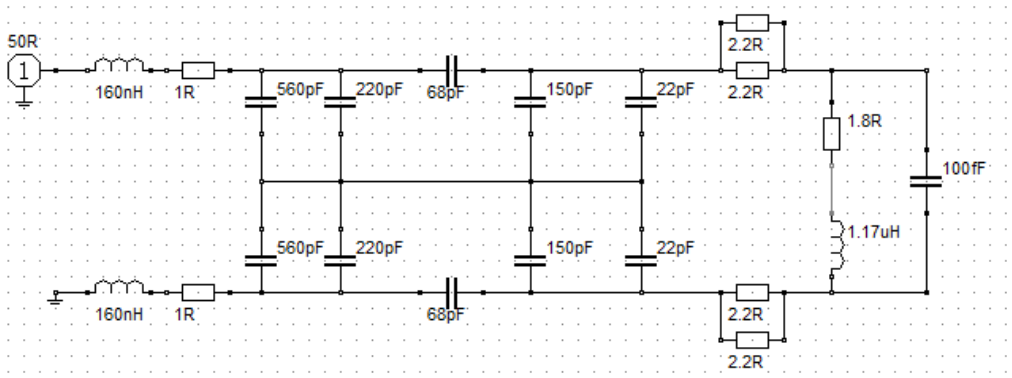
C1 = 69.4 pF is replaced with 68 pF

C2 = 170 pF is replaced with 150 pF || 22 pF

$R_{damping}$ = 1.09 Ω is replaced with 2.2 Ω || 2.2 Ω

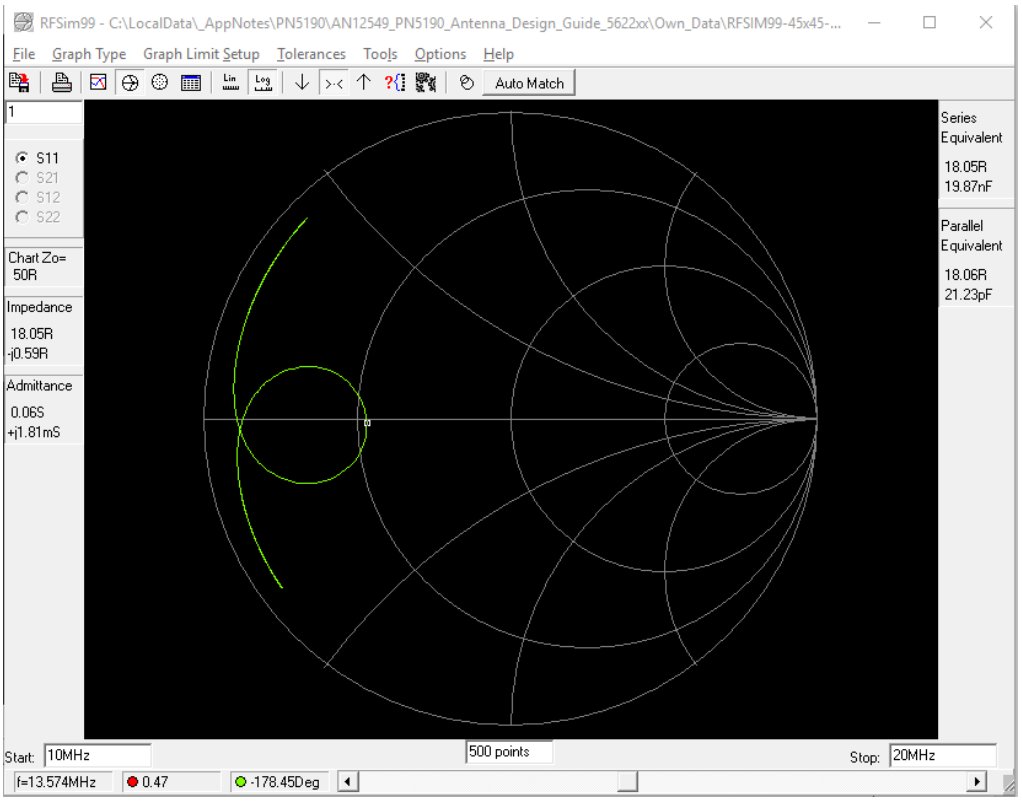
All values are tuned in such a way, that the smith chart plot shows a “symmetrical” plot with the correct target impedance at resonance.

The Figure 47 and Figure 48 show the result of that correction.



1.

Figure 47. Corrected simulation circuit



1. The simulated impedance is slightly higher than the target.

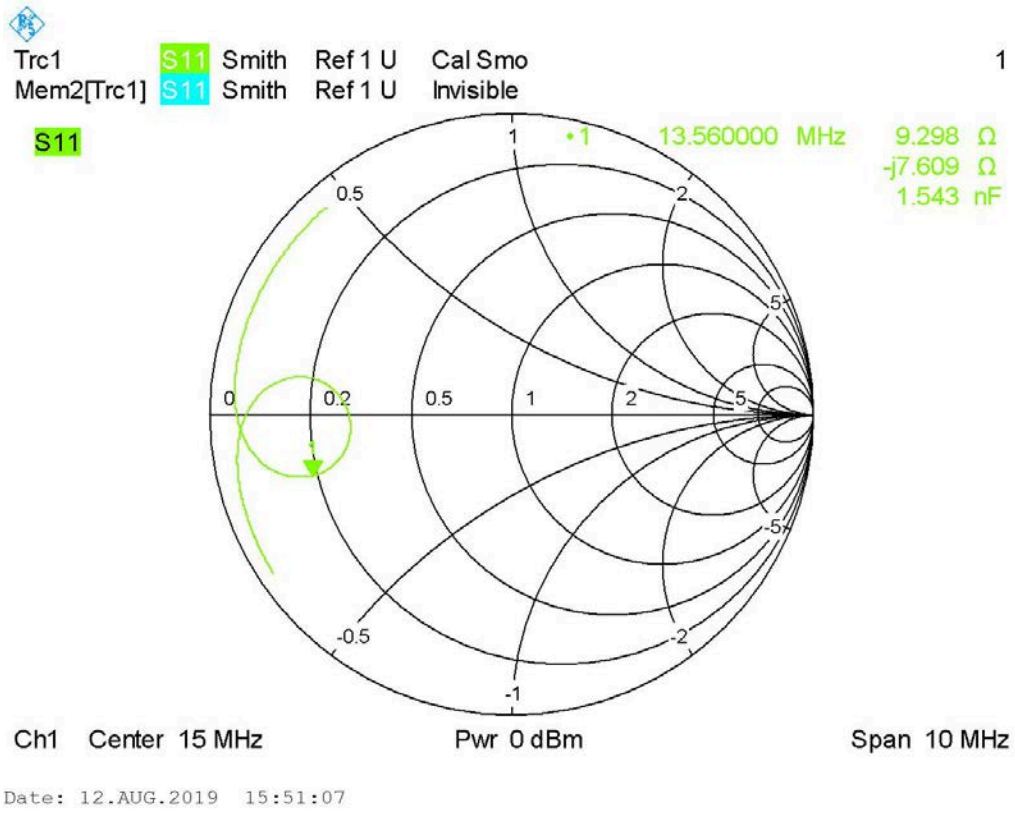
Figure 48. Smith chart plot of the corrected tuning circuit

4.6 Measure the real circuit

Use the measured values for the tuning. If the measured values are correct and close to the simulated values, the measured impedance plot must be the same as the simulated one.

However, the measurement of the antenna coil introduced some uncertainties especially on the losses, which the simulation did not consider. The layout has some influence too as it introduces some additional parallel capacitance and some inductance due to the length of traces.

Figure 49 shows an example of mismatch between the measured and the simulated circuits.



1. First-time assembly after simulation

Figure 49. Smith chart plot of the corrected circuit

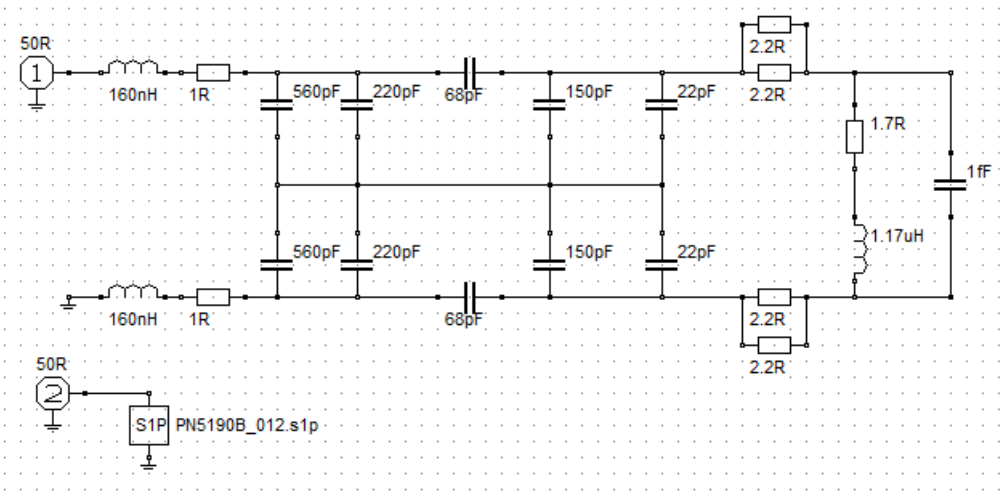
The measured smith chart indicates a high C2, and the impedance is a bit low.

The explanation for C2 value is that the antenna coil measurement did no take any capacitance into account. A few pF are missing in the simulation.

The low impedance value is related to the inaccurate R_{Coil} measurement. The antenna synthesis returned R_{Coil} = 1.7 Ω, while the VNA measurement showed R_{Coil} = 2.9 Ω to 3.3 Ω. Try different values in the simulation (preferably between 1.7 Ω and 3.3 Ω) to derive an S11 simulation plot that matches the measurement plot.

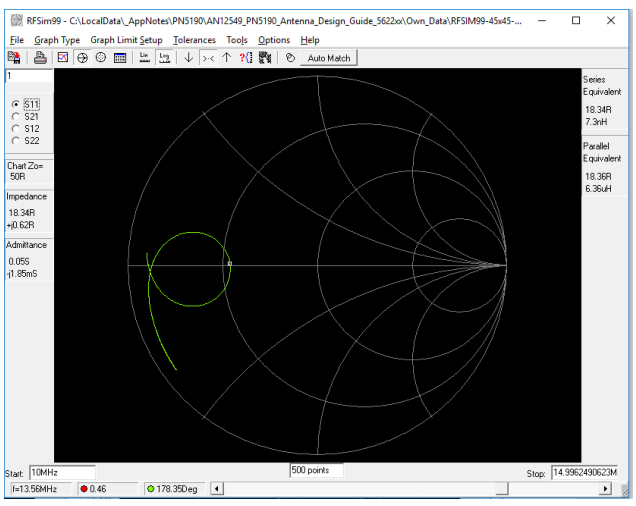
4.7 Adapt the simulation

To simplify the exercise, the measurement plot is saved in S1P-file, and then added into the simulation file (Figure 50).

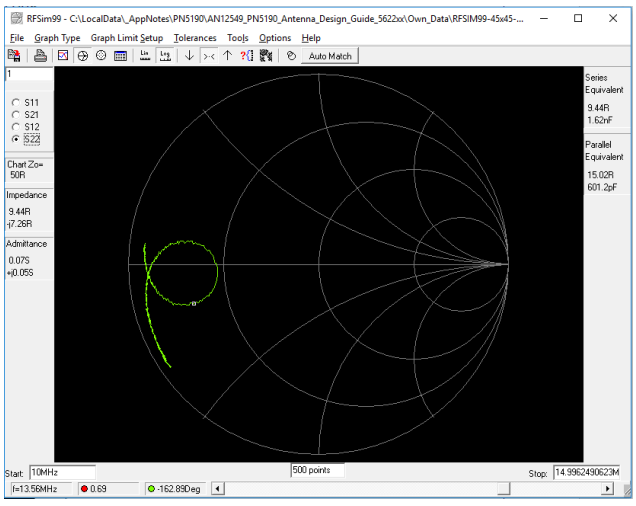


1.

Figure 50. First Assembly, simulated and measured



S11: simulation plot



S22: measured plot

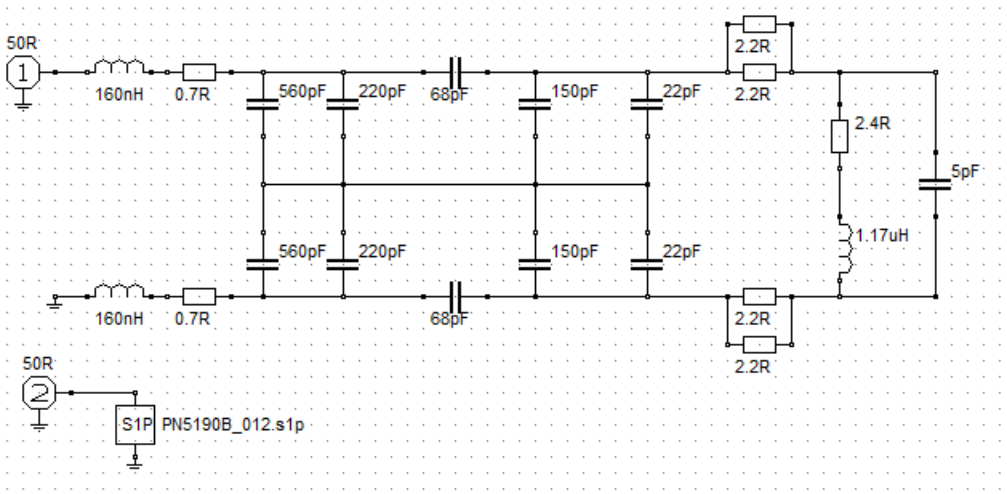
Figure 51. Comparison of simulation and measurement

Note: *The span is automatically limited by the simulation tool due to the high number of measurement points, and therefore ends at 15 MHz. 15 MHz still is enough for the tuning purpose, so this limitation does not matter.*

With the following changes, the simulation is adapted to match the reality:

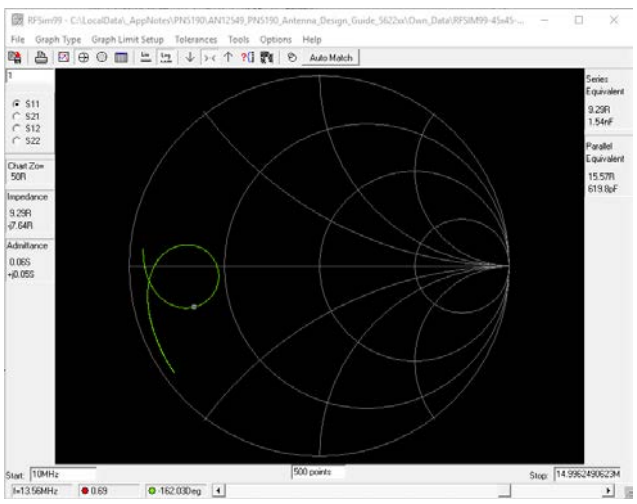
- Increase the C_{ant} to C_{ant} = 5 pF.
- Increase the R_{Coil} to R_{Coil} = 2.4 Ω.
- The estimated losses of the L0 inductors were too high. So, the resistance values, which indicate the L0 losses, are reduced to R_{L0} = 0.7 Ω.

With these three corrections, the simulation plot matches the measurement (Figure 52 and Figure 53).

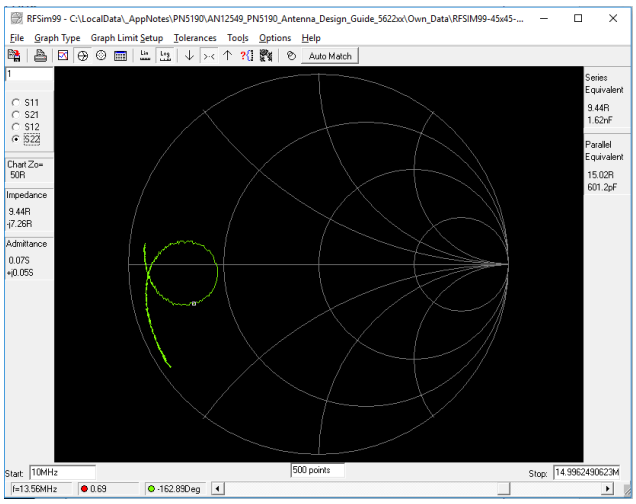


1. The antenna is not properly tuned yet!

Figure 52. Adapted simulation plot to match the measured plot



S11: simulated plot



S22: measured plot

Figure 53. Smith chart comparison after adaptation

After the adaptation, the simulation is accurate enough to represent the reality.

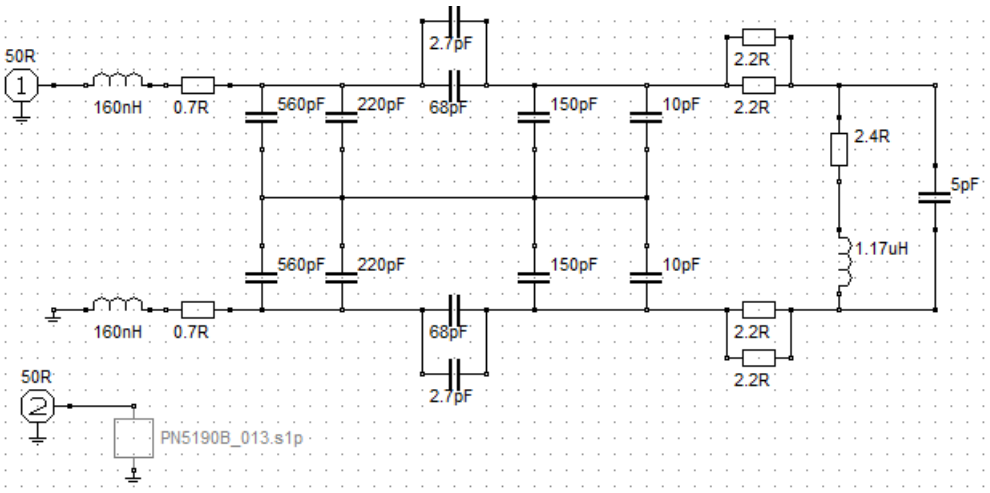
The last step is to retune the circuit to meet the initial target, which is to get a symmetrical plot with the parallel resonance at the target impedance.

4.8 Correct the simulation

When the values are adapted so the simulation matches the reality, the final step is the symmetrical tuning to meet the target impedance. The changes are:

- Reduce C2 to C2 = 10 pF
- Increase C1 to C1 = 68 pF || 2.7 pF

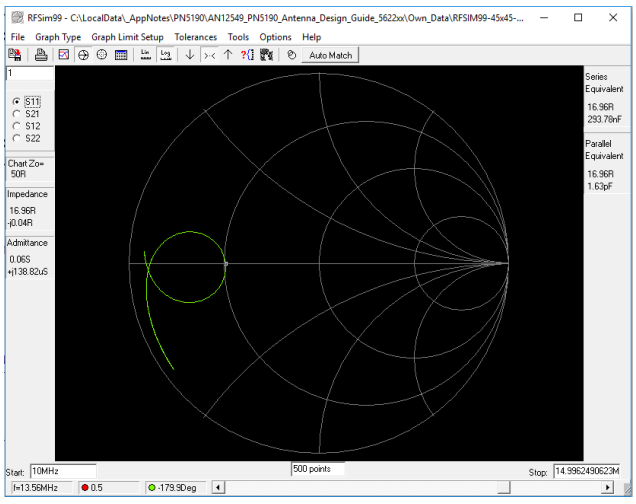
With these changes, the target impedance is correct, as the simulation result shows in Figure 54 and Figure 55.



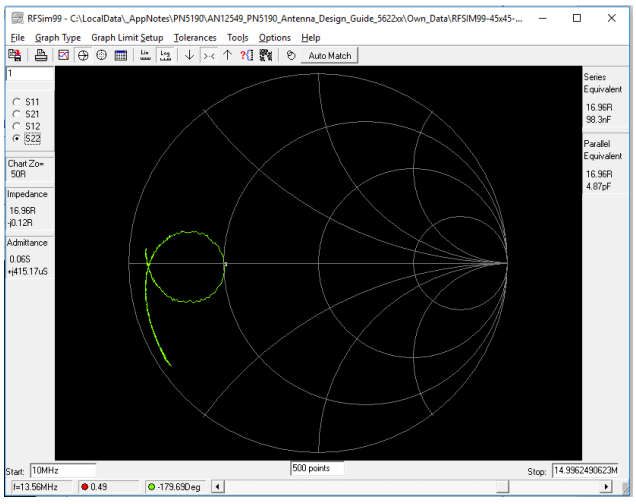
1.

Figure 54. Corrected simulation circuit to meet the target impedance

Using these values, the target impedance is 17 Ω.



S11: Corrected simulation plot

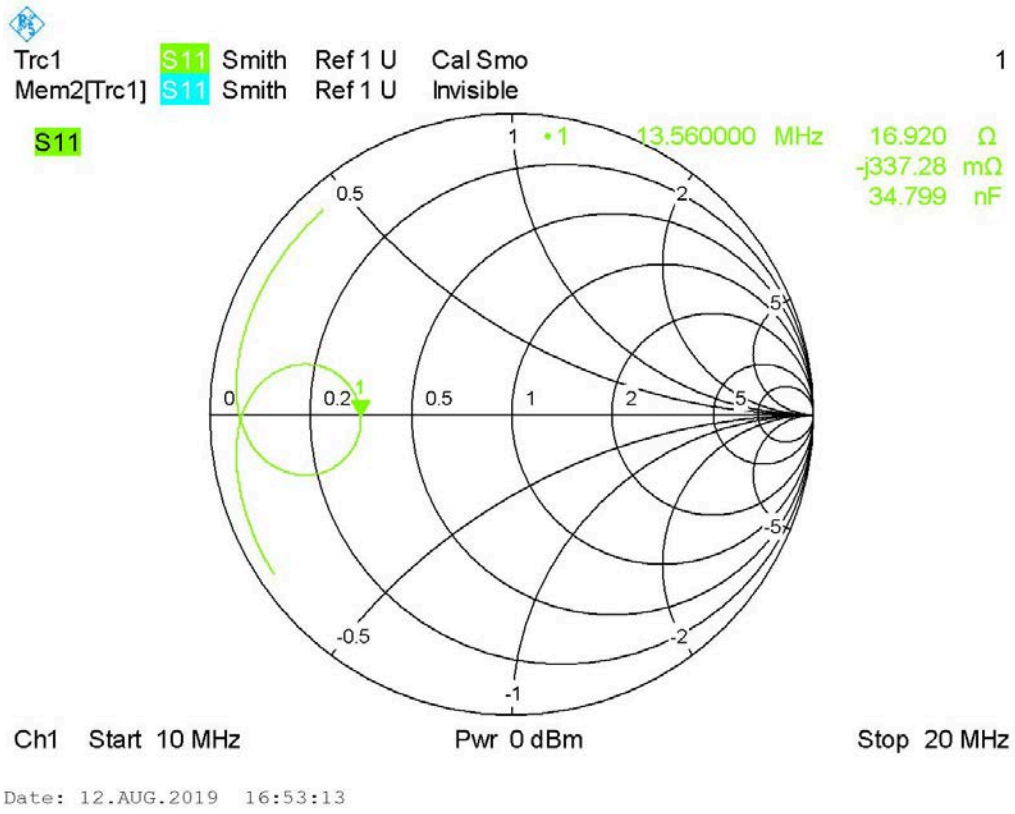


S22: Measured corrected plot

Figure 55. Corrected simulation plot to meet the target impedance

4.9 Finalize the tuning

The real measurement (already shown as S11-File in Figure 55) then shows the correct tuning, which is already finally tuned, as shown in Figure 56.



1. No further fine-tuning is required.

Figure 56. Final antenna tuning measurement

4.10 RX circuit

The RX circuit is the coupling of the EMC filter output to the RX inputs. The coupling creates a capacitor for DC decoupling, and a resistor (Figure 57).

The value must be:

Crx = 1 nF

Rrx = 560 Ω to 1500 Ω

The exact value of Rrx must be set after DPC has been calibrated. See Section 6.

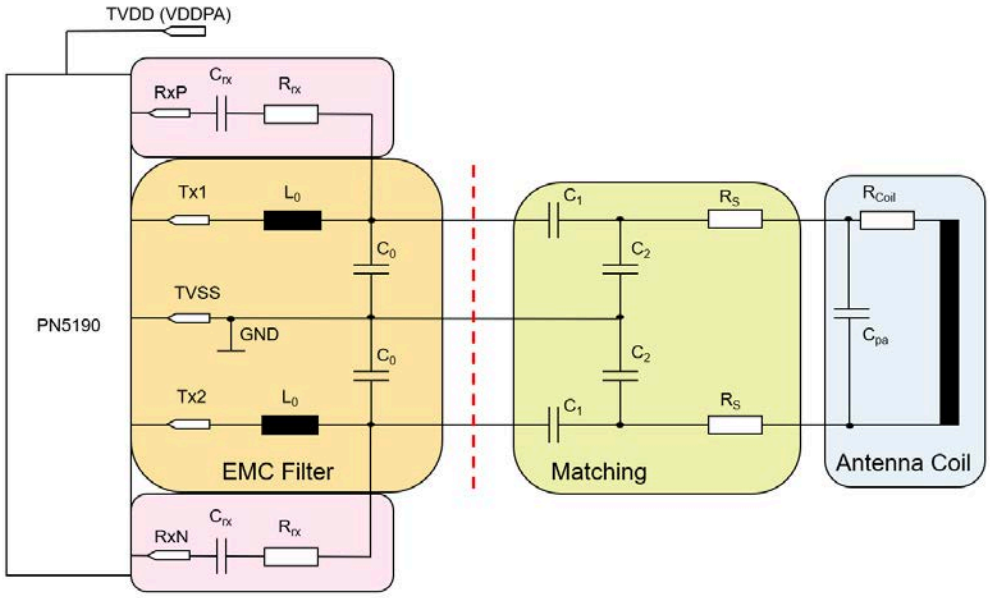


Figure 57. PN5190 complete antenna circuit (including RX)

5 PN5190 and Dynamic Power Control (DPC)

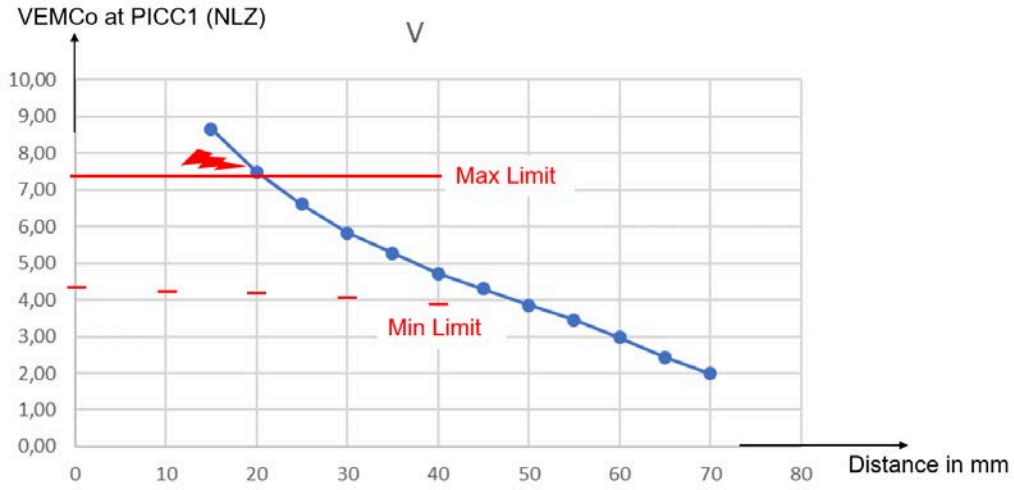
The PN5190 antenna tuning is optimized to provide a maximum power transfer for a large operating distance (related to the antenna size), i.e. it is optimized for the case of very low coupling. This provides the maximum possible power transfer operating distance.

5.1 Bad example with no DPC

However, as soon as the PICC comes closer to the PCD antenna, the loading and detuning causes an increase of the driver current ITVDD as well as an increase of the power transfer. That can easily result in too much RF field (power transfer) for the PICC as well as too much driver current (ITVDD). Examples measured with the EMVCo 3.0 TestPICC1 for the 45 mm x 45 mm antenna are shown in Figure 58 and Figure 59.

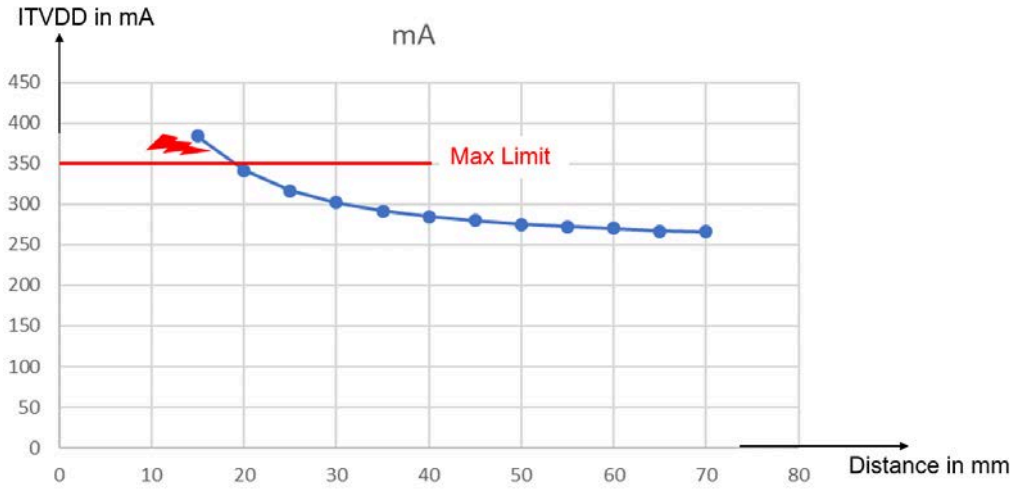
Below 20 mm the maximum power transfer is exceeded as well as the ITVDD limit of the PN5190. That might both destroy the PICC and the PCD, and at least violates the specifications.

Note: *The PN5190 has an overcurrent protection, which switches off the RF field in case of over temperature, as well as an over temperature protection, which resets the PN5190 in case of over temperature. However, in a good PCD design, these protections should never be triggered during normal operation.*



1. 45 mm x 45 mm antenna

Figure 58. EMVCo Power transfer example without DPC



1. 45 mm x 45 mm antenna

Figure 59. TX Driver current (ITVDD) example without DPC

5.2 First step of DPC: current limiter

To comply with the specification, the PN5190 DPC provides a current limiter function, which can be configured.

The first step of the configuration is the definition of a target current. The PN5190 DPC automatically:

- Controls the supply voltage of the TX driver (VDDPA) from 5.7 V down to 1.5 V in 43 100-mV steps.
- Keeps the driver current (ITVDD) constant at the target current value +/- a hysteresis.

Both the target current (DPC_TARGET_CURRENT) and the hysteresis (DPC_HYSTERESIS for loading and unloading) can be defined in EEPROM (see [1]).

5.2.1 DPC_TARGET_CURRENT

The target current (DPC_TARGET_CURRENT, 0x77 and 0x78) is the nominal current that drives the antenna. When the ITVDD exceeds the target current (including a hysteresis), the VDDPA is reduced automatically. The automated correction protects the PN5190, and maintains the field strength limits (of ISO, NFC or EMVCO).

For EMVCo POS design, measure the ITVDD with the TestPICC (for example TestPICC1) at 4 cm distance. Then write the values into the DPC_TARGET_CURRENT. The NFC Cockpit provides a simple interface to do that.

5.2.2 DPC_HYSTERESIS

The hysteresis (DPC_HYSTERESIS_LOADING, DPC_HYSTERESIS_UNLOADING) together with the target current (DPC_TARGET_CURRENT) define the current limit at which the DPC automatically decreases or increases the VDDPA.

The VDDPA is automatically reduced as soon as the current exceeds the DPC_TARGET_CURRENT + DPC_HYSTERESIS_LOADING. The VDDPA is automatically increased again as soon as the current is below DPC_TARGET_CURRENT – DPC_HYSTERESIS_UNLOADING.

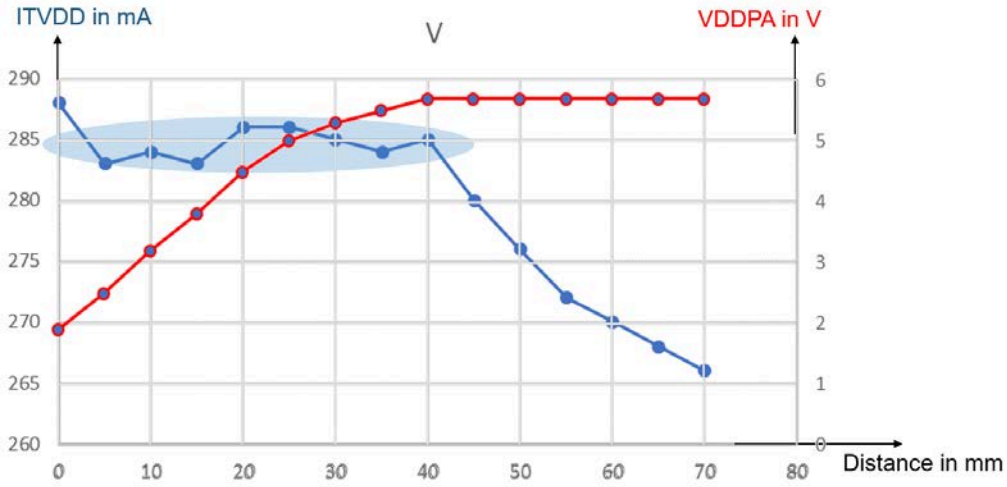
The hysteresis must not be less than 20 dec (loading) and 10 dec (unloading). The default values cannot be changed – other than for test purposes.

The Figure 60 shows an example with the current ITVDD and the related TX driver supply voltage VDDPA under loading conditions. The TestPICC1 is used to load the 45 mm x 45 mm antenna. The target current is set to 285 mA, and all the current reduction values in the LUT are reset to 0 (this is no default setting).

Below 40 mm of operating distance, the DPC current limiter reduces the VDDPA, which then keeps the current within the defined window of 285 mA +/- 20 mA. This protects the PN5190 and the overall power supply circuit.

Note: *With the RDON feature, the default control range of the VDDPA is [2.2 V – 5.7 V]. But if the loading is too strong, the current can increase above the limit, since the VDDPA cannot decrease further.*

Note: *If needed, use the TXLDOVDDPALOW (0x7D) to set the minimum VDDPA. With the RDON feature, use TXLDOVDDPALOW = 2.2 V. For all other cases, use the lowest setting of 1.5 V. Run the DPC calibration for the full VDDPA range from 1.5 V to 5.7 V. Next, adjust the lower limit of the VDDPA to any higher value (enabling or disabling the RDON feature), if needed, without changing the DPC calibration.*

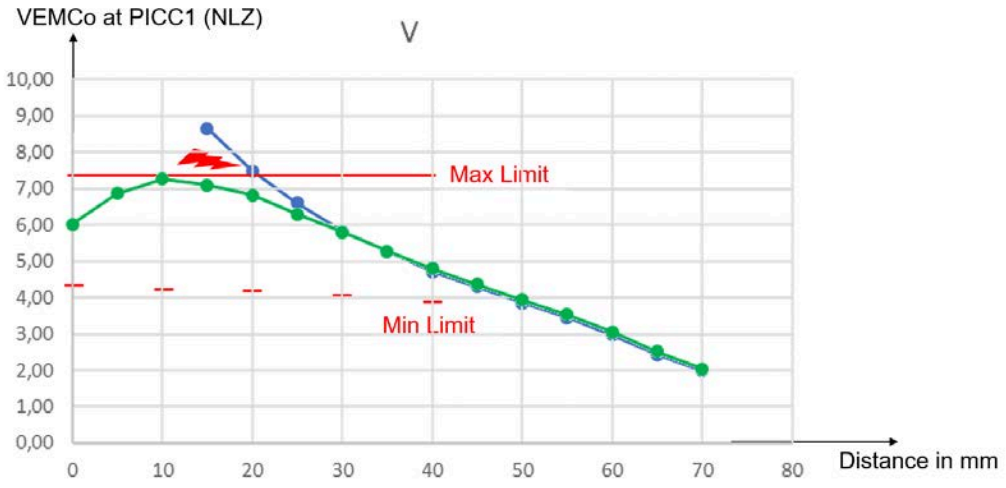


1. 45 mm x 45 mm antenna, target current = 285 mA

Figure 60. ITVDD and VDDPA with automatic current limiter

The Figure 61 shows the EMVCo power transfer measured with the EMVCo TestPICC1. The use case is the same with the current limiter shown in Figure 60. The figures show that the current limiter helps to meet the EMVCo power transfer limits. But at 1 cm distance, the maximum power limit is almost reached. A further current reduction (= power reduction) under these loading conditions (TestPICC in the range of around 1 cm) is needed.

To enhance the control of the power transfer, the current reduction feature is used (Section 5.3).



1. 45 mm x 45 mm antenna

Figure 61. EMVCo power transfer with automatic current limiter

5.3 Second step of DPC: current reduction

As shown in Figure 61, the current limiter does not suffice to meet the specification limits. In addition to the current limiter (“target current”), the PN5190 DPC uses a current reduction lookup table (DPC_LOOKUP_TABLE, see [1]). The lookup table is used for each of the 43 VDDPA steps (if TXLDOVDDPALOW = 1.5 V).

5.3.1 DPC_LOOKUP_TABLE

The DPC_LOOKUP_TABLE (DPC LUT) defines a 4-byte entry per VDDPA step, from 5.7 V down to 1.5 V (resulting in 43 entries).

BYTE 0 (LSByte): This byte defines the current reduction at this VDDPA(new). The value is an unsigned integer value: The final target current is the DPC_TARGET_CURRENT – current reduction value.

The DPC takes the current measurement and calculates a load:

Load = VDDPA(old) / ITVDD

Based on the load, the “new” VDDPA = VDDPA(new) is calculated. If no extra current reduction is defined, the VDDPA(new) is the applied VDDPA:

VDDPA(new) = Load · target current

In a second step, the required current reduction is applied, which results in the final VDDPA = VDDPA(target):

VDDPA(target) = Load · (target current – current reduction @ VDDPA(new))

Example:

Assumption 1: Unloaded ITVVD = 300 mA @ VDDPA = 5.7 V (due to the antenna tuning)

Assumption 2: Target current = 300 mA (set in DPC_TARGET_CURRENT)

Assumption 3: Current reduction @ 5.3 V = 20 mA (set in the related entry of DPC_LOOKUP_TABLE)

When the loading changes and the ITVDD exceeds the 320 mA, the DPC must switch the power level.

Load = 5.7 V / 320 mA = 17.8 Ω -> VDDPA(new) = 17.8 Ω · 300 mA = 5.3 V

VDDPA(target) = 17.8 Ω · (300 mA - 20 mA) = 5.0 V

The DPC switches down to 5.0 V.

Attention: To get a certain ITVDD at a certain VDDPA = VDDPA(target), the current reduction value of the corresponding VDDPA(new) must be set. The VDDPA(new) is the related VDDPA value **without** current reduction.

Example above: To achieve the ITVDD = 280 mA at VDDPA = 5.0 V, the current reduction of 20 mA must be set into the LUT entry at the VDDPA = 5.3 V.

The NFC Cockpit DPC calibration provides a calculation, which creates some major LUT entries, based on a few measurements.

Attention: The current reduction for a lower VDDPA can be even higher than the one of the next higher VDDPA, as long as the calculated load (load = VDDPA / ITVDD) is equal or higher than the one of the next higher VDDPA. Otherwise, the DPC starts oscillating.

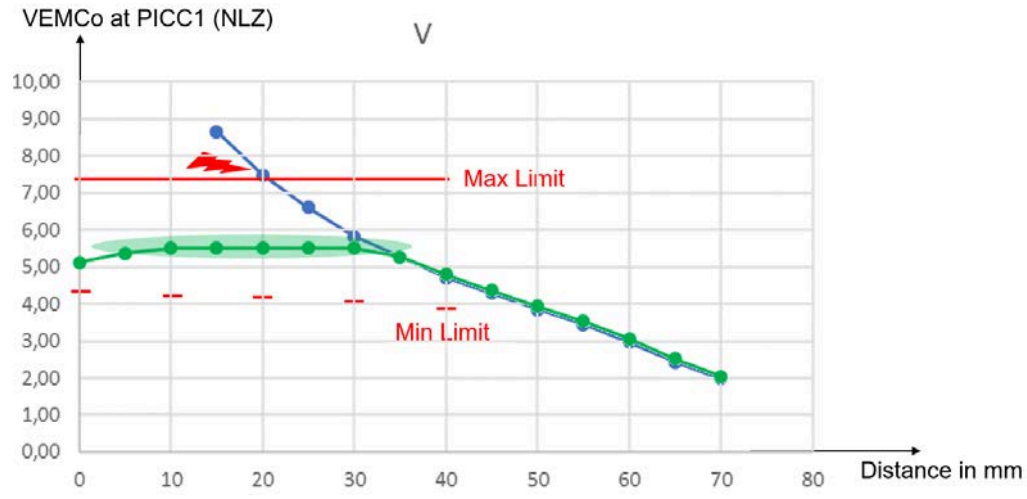
The BYTE 1, BYTE 2, and BYTE 3 are not relevant for the DPC calibration itself, so they have no impact of the power transfer. However, they are used to define a dynamic adjustment of TX Shaping parameters. The details of the TxShaping are explained in[19].

BYTE 1: This byte defines a relative change of the modulation index. It is a signed integer value, which is added to the RESIDUAL_AMPL_LEVEL of the applied protocol.

BYTE 2: This byte defines the relative change of the rise and fall time parameter (EDGE_STYLE) of the 100 % ASK (for example, type A 106). It is a signed integer, which is added to the EDGE_STYLE of the applied protocol (for 100 % ASK), if the FW-based TxShaping is used.

BYTE 3: This byte defines the relative change of the rise and fall time parameter (EDGE_STYLE) of the 10 % ASK (for example, type B 106). It is a signed integer, which is added to the EDGE_STYLE of the applied protocol (for 10 % ASK), if the FW-based TxShaping is used.

Use the current reduction per VDDPA step to optimize the power transfer. The Figure 62 shows the power transfer measurement with **manually** adjusted current: the power transfer is the target for the DPC calibration.



1. 45 mm x 45 mm antenna

Figure 62. EMVCo power transfer with manual current reduction (target)

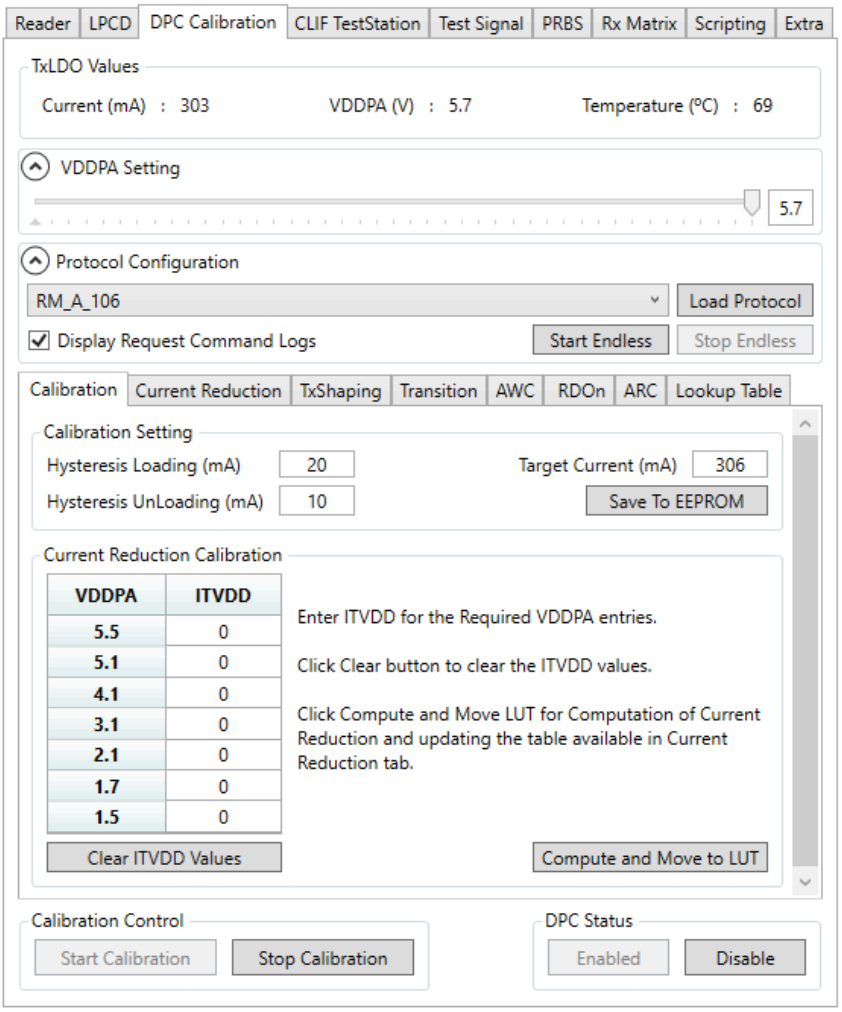
5.4 PN5190 DPC calibration

To operate the PN5190 with optimum performance, only a few settings must be defined. You can use the NFC Cockpit to adjust the settings.

5.4.1 Set target current

The target current is the first setting.

For EMVCo POS design, measure the ITVDD with the TestPICC (for example TestPICC1) at 4 cm distance. Use NFC Cockpit to write the values into the DPC_TARGET_CURRENT (Figure 63).



1. The DPC calibration loop reads continuously the ITVDD and the temperature, and indicates the VDDA.

Figure 63. NFC Cockpit: DPC Calibration entry of target current and hysteresis

Set the target current, but do not change the hysteresis value (other than for test purposes).

Set the target current so the PN5190 does not reduce the VDDPA without major loading.

For EMVCo: Use the TestPICC1 to check the power transfer at 4 cm distance, as it gives a reasonable amount of loading (depending on PCD antenna size). The current ITVDD increases by 15 mA to 20 mA from unloaded, as soon as the TestPICC1 is placed into position 400.

In combination with the given hysteresis, use the target current anywhere in between the unloaded current and the ITVDD with the TestPICC in 400.

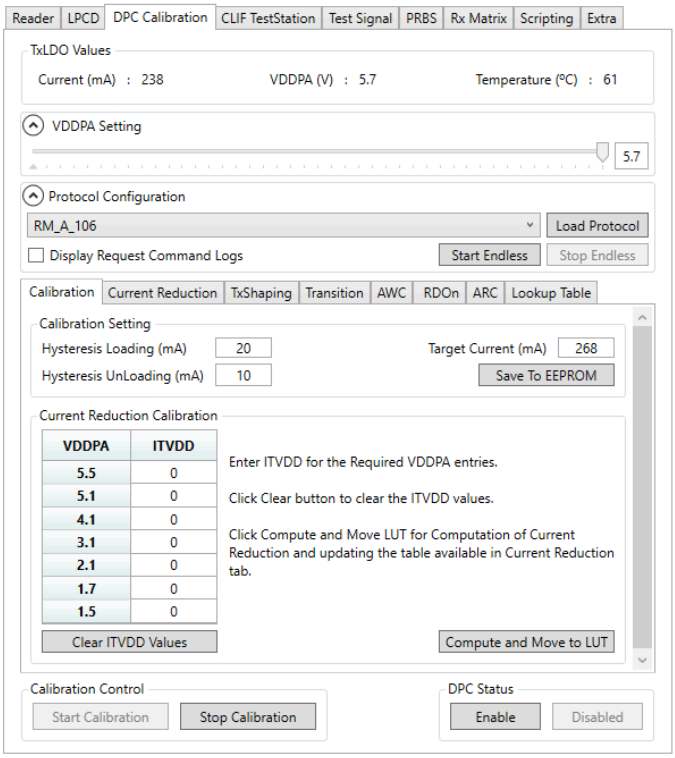
5.4.2 Set current reduction

Set the current reduction carefully to avoid a DPC oscillation. The NFC Cockpit provides a function to measure the current at seven VDDPA positions and then calculate the related current reduction values. The remaining empty current reduction LUT entries must be filled manually with interpolation. This method is sufficient to retrieve a working DPC calibration.

A more accurate alternative is to use the NFC Cockpit and measure each VDDPA separately and calculate all the related values.

The principle of measuring the required current reduction is the same in both methods:

1. Start DPC calibration and disable DPC.
2. Stop DPC calibration and reset PN5190 (soft reset).
3. Restart the DPC calibration and load protocol A106.



1. Unloaded conditions: ITVDD = 238 mA

Figure 64. DPC Calibration start with disabled DPC

Start the measurement of the required ITVDD at a certain VDDPA:

1. Adjust the required VDDPA using the VDDPA slider.
2. Apply the required loading, for example with the EMVCo TestPICC, for the given VDDPA at the distance the required power transfer is achieved.
3. Read the current ITVDD.

Note: *With disabled DPC, there is no current limiter. Take care that the resulting current ITVDD depends on the loading condition, and can exceed the PN5190 limits.*

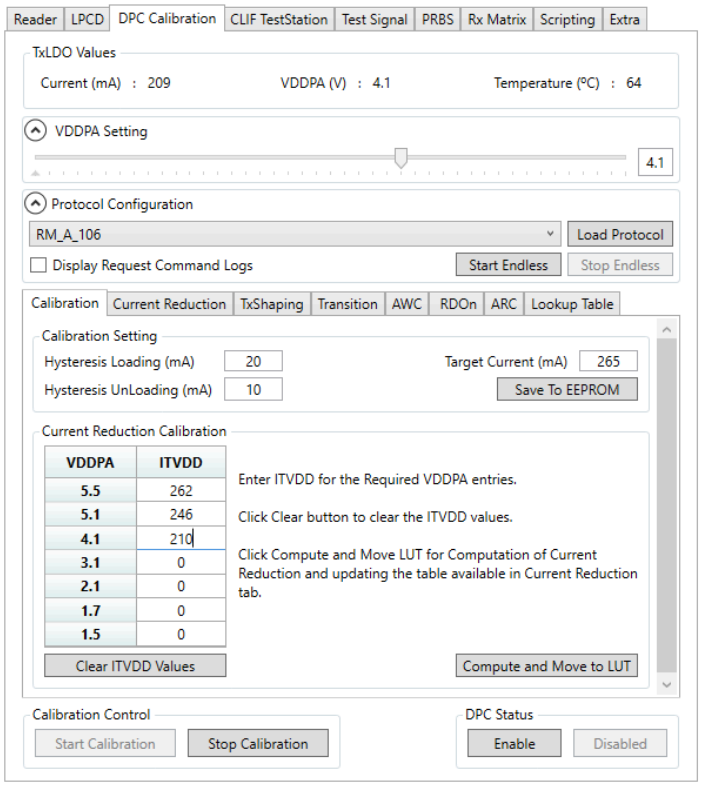
5.4.2.1 NFC Cockpit current reduction calibration fast method

The NFC Cockpit provides a simple support to calibrate the DPC. It calculates seven LUT entries out of a measurement procedure.

Enter the target condition (= target ITVVD) for seven different VDDPA levels.

Figure 65 shows the example of measurement at VDDPA 4.1 V: the applied load (TestPICC at a certain distance, which shows the targeted power transfer) causes an ITVDD of 208 mA to 210 mA.

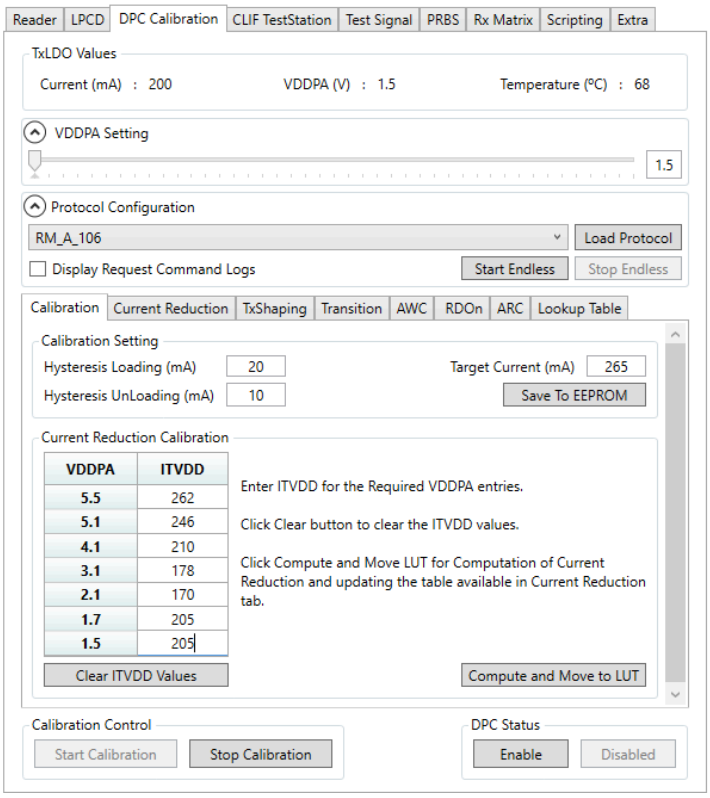
To achieve the same power transfer when enabling the DPC, set DPC LUT so the DPC loop targets the 210 mA at 4.1 V.



1. The load applied results in ITVDD = 210 mA @ VDDPA = 4.1 V

Figure 65. DPC Calibration with NFC Cockpit, calibrating

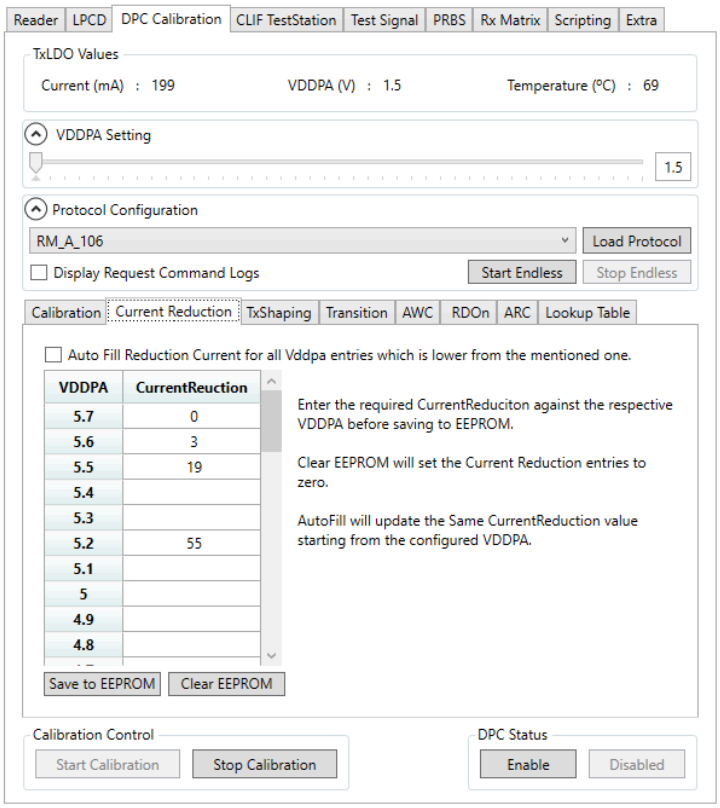
When all seven measurements are done, click the <Compute and Move to LUT>. The NFC Cockpit calculates the related LUT entries (Figure 66) .



1. All measurements done

Figure 66. DPC Calibration with NFC Cockpit, measurements done

The NFC cockpit switches to the second subtab. Seven entries are indicated in the LUT as shown in Figure 67. The empty LUT entries must now be filled manually, before the complete LUT can be saved in EEPROM.



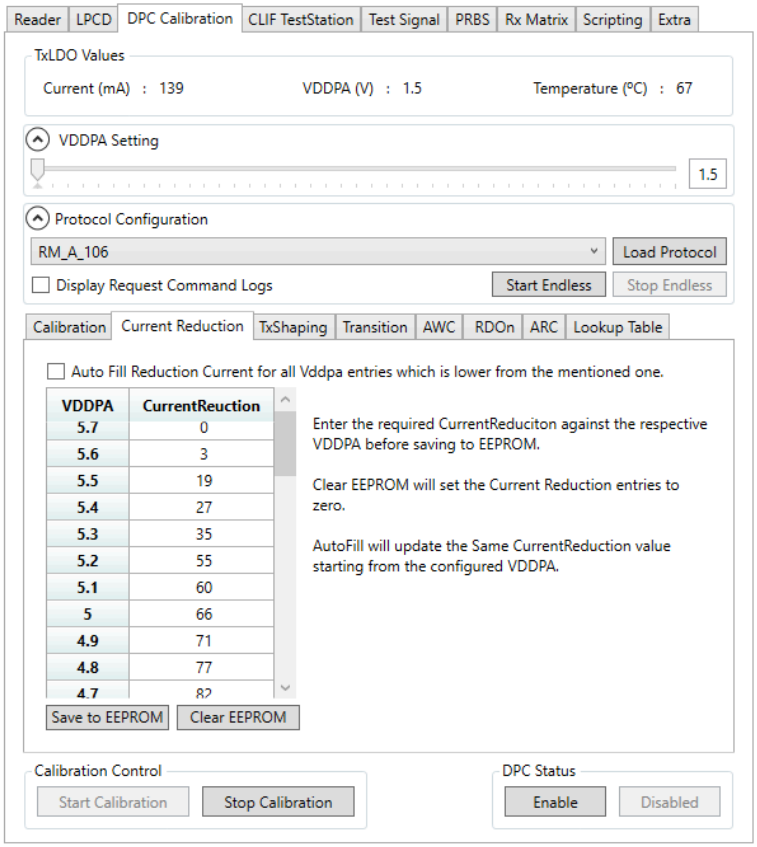
1. The empty entries must be filled manually (interpolation).

Figure 67. DPC Calibration with NFC Cockpit, LUT start

To fill the missing LUT entries, the in-between values can simply be interpolated (Figure 68).

To save the values into EEPROM when all LUT entries are filled, click the <Save to EEPROM> button.

The DPC is calibrated and must be enabled again.



1. The complete LUT must be saved to EEPROM

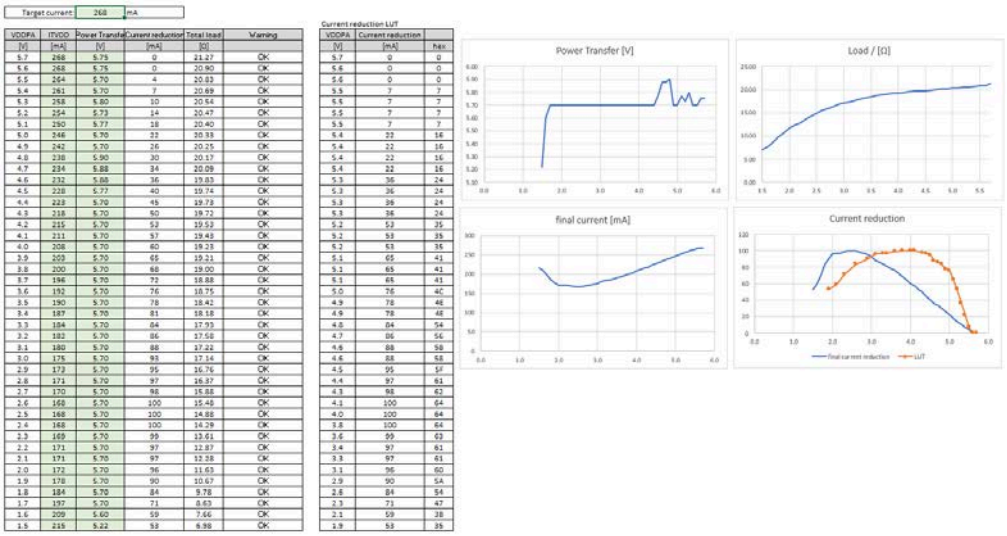
Figure 68. DPC Calibration with NFC Cockpit, all LUT entries filled

5.4.2.2 NFC Cockpit current reduction calibration accurate method

If needed, the LUT can be filled manually with an accurate measurement for each of the given VDDPA values.

NXP provides an excel sheet to perform the calculation and help to visualize the calibration results, as shown in Figure 69.

The way of calibrating is the same as described in Section 5.4.2.1, but instead of seven, all 43 VDDPA steps are measured.



1. 50 mm x 30 mm antenna

Figure 69. Example of DPC Calibration, using DPC_LUT excel sheet

In this example, the EMVCo TESTPICC (EMVCo 2.6) is used to load and define the DPC current values. The measurement starts with disabled DPC, VDDPA = 5.7 and the TestPICC placed in 70 mm above. This can be seen as “unloaded”: moving the TESTPICC further away does not influence the current value.

Moving the TestPICC in steps of 5 mm, the VDDPA and the ITVDD are measured (reading from NFC Cockpit) and the EMVCo power transfer is checked (Vdc at the TestPICC) at each step.

At 40 mm distance the current value can be read: ITVDD = 268 mA. The value is taken as the input for the DPC_TARGET_CURRENT.

The power transfer at this point is 5.75 V, measured at the TestPICC. This value is the target over the full calibration range.

When switching the VDDPA to 5.6 V, the ITVDD decreases and so does the power transfer. Correcting the operating distance shows that at a slightly lower distance and with the same current, the same power transfer can be achieved. The target current for VDDPA = 5.6 V is 268 mA.

When switching the VDDPA to 5.5 V, the ITVDD decreases and so does the power transfer. Correcting the operating distance shows that at a slightly lower distance, the current required to achieve the same power transfer is slightly less than before. The target current for VDDPA = 5.5 V is 264 mA.

To achieve the power transfer of ≈ 5.75 V, note down the current for each VDDPA when stepping down the VDDPA step by step.

At VDDPA = 5.3 V, the current of 255 mA that is required to achieve the power transfer of 5.75 V, cannot be taken, since with that combination of VDDPA and ITVDD, the load increases at lower VDDPA. This case leads

to an undefined DPC condition and must be avoided. The current must be increased until the load = VDDPA / ITVDD is lower than the previous one.

For the VDDPA = 5.3 V, the current is raised to 258 mA.

Make the measurement for all VDDPA steps. For each step, the conditions are:

1. the power transfer is at its target,
2. the load is lower than the load in the previous (higher) VDDPA step.

The example is shown in Table 5.

Table 5. Current reduction LUT example

If there is ambiguity, the higher current is taken.

VDDPA / [V]	ITVDD / [mA]	Load / [Ω]	LUT VDDPA	Current reduction
5.7	268	21.27	5.7	0
5.6	268	20.90	5.6	0
5.5	264	20.83	5.6	0
5.4	261	20.69	5.5	7
5.3	257	20.62	5.5	7 (instead of 11)
5.2	254	20.47	5.5	7 (instead of 14)
5.1	250	20.40	5.5	7 (instead of 18)
5.0	246	20.33	5.4	22
4.9	242	20.25	5.4	22 (instead of 26)
4.8	238	20.17	5.4	22 (instead of 30)
4.7	234	20.09	5.4	22 (instead of 34)
4.6	232	19.83	5.3	36
4.5	228	19.74	5.3	36 (instead of 40)
4.4	223	19.73	5.3	36 (instead of 45)
4.3	218	19.72	5.3	36 (instead of 50)
4.2	215	19.53	5.2	53
4.1	211	19.43	5.2	53 (instead of 57)
4.0	208	19.23	5.2	53 (instead of 60)
3.9	203	19.21	5.1	65
3.8	200	19.00	5.1	65 (instead of 68)
3.7	196	18.88	5.1	65 (instead of 72)
3.6	192	18.75	5.0	76
3.5	190	18.42	4.9	78
3.4	187	18.18	4.9	78 (instead of 81)
3.3	184	17.93	4.8	84
3.2	182	17.58	4.7	86
3.1	180	17.22	4.6	88
3.0	175	17.14	4.6	88 (instead of 93)

Table 5. Current reduction LUT example*...continued*

If there is ambiguity, the higher current is taken.

VDDPA / [V]	ITVDD / [mA]	Load / [Ω]	LUT VDDPA	Current reduction
2.9	173	16.76	4.5	95
2.8	171	16.37	4.4	97
2.7	170	15.88	4.3	98
2.6	168	15.48	4.1	100
2.5	168	14.88	4.0	100
2.4	168	14.29	3.8	100
2.3	169	13.61	3.6	99
2.2	171	12.87	3.4	97
2.1	171	12.28	3.3	97
2.0	172	11.63	3.1	96
1.9	178	10.67	2.9	90
1.8	184	9.78	2.6	84
1.7	197	8.63	2.3	71
1.6	209	7.66	2.1	59
1.5	215	6.98	1.9	53

In this example, the current increases again at lower VDDPA. That is possible, since the load always decreases at lower VDDPA.

With these inputs, the current reduction LUT entries can be calculated:

$$LUT\ \ VDDPA = VDDPA \big/ ITVDD \cdot TargetCurrent$$

$$Current\ \ reduction = target\ \ current - ITVDD$$

With

- LUT VDDPA: entry field for the corresponding current reduction
- VDDPA = VDDPA, as set during the calibration measurement
- ITVDD = current, as measured with TXLDO_VOUT_CURR register
- Target current = DPC_TARGET_CURRENT
- Current reduction = decimal value for the LUT

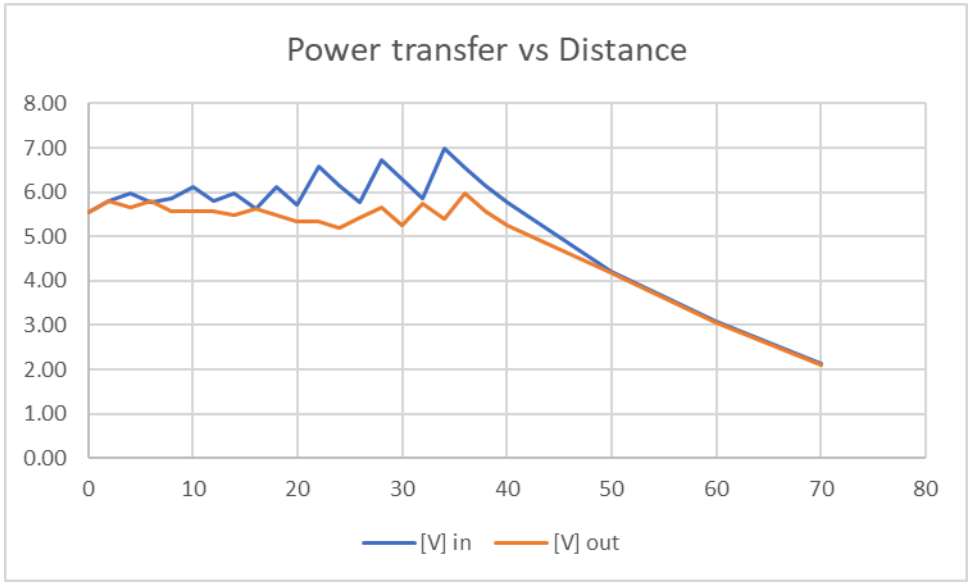
If different current reduction values are applied to the same VDDPA entry, the first value (which results in the highest ITVDD) must be chosen.

Note: *Empty LUT entries require a manual interpolation (VDDPA = 4.2 in the above example). Interpolate these entries with 99.*

With the values written into the DPC_LOOKUP_TABLE, the DPC is calibrated. Figure 70 shows the final measurement with the EMVCo 2.6 TestPICC moving into the field (blue curve) and moving back out of the field (orange curve).

With these settings, the overall power transfer with all three TestPICCs of EMVCo 3.0 can be met.

Note: *The calibration for EMVCo can be done with either of the TestPICCs. Even the older EMVCo 2.6 TestPICC can be used (as shown in this example). Consider the different voltage limits as the PICCs show different loading and different voltage levels.*



1. Distance in mm, power transfer in V, measured at the EMVCo 2.6 TestPICC
2. 50 mm x 30 mm antenna
3. Blue = moving in; orange = moving out

Figure 70. EMVCo 2.6 power transfer example with final DPC

6 PN5190 RX

The PN5190 receiver (RX) is different than the RX of PN5180 or CLRC663. PN5190 RX uses DSP with matched filters for a higher sensitivity and better robustness. The build Contactless Test Station (CTS) is used to optimize the settings and performance, and for debugging purposes.

The overall external circuitry of PN5190 RX is the same as PN5180 or CLRC663 (Figure 71).

For the optimum performance, only the values of Crx and Rrx must be defined.

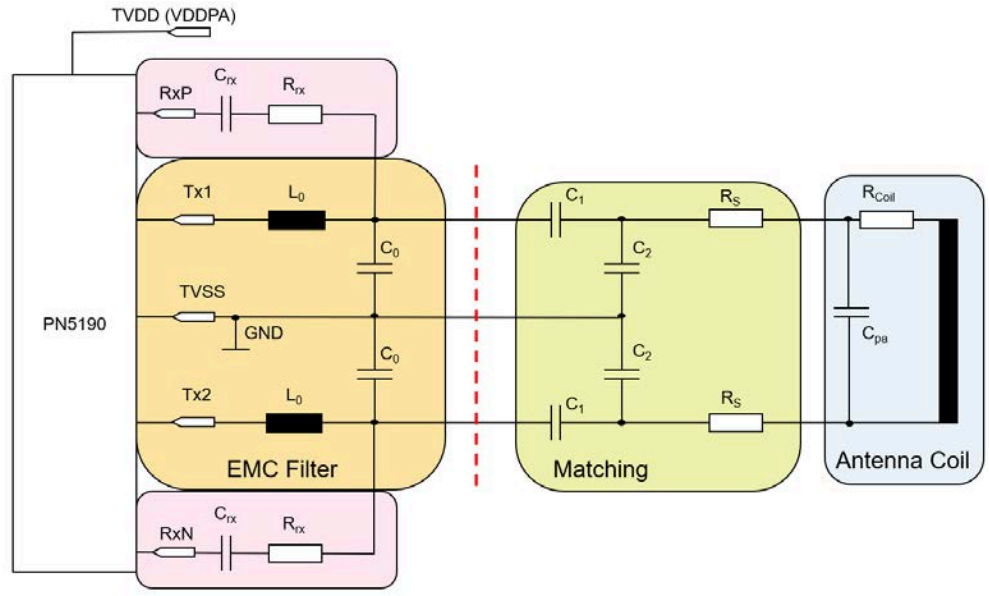


Figure 71. PN5190 antenna circuit including the RX path

C_{RX} = 1 nF

R_{RX} ≈ 560 … 1500 Ω (see below)

Note: *The RX layout must be symmetrical, as shown in Figure 12.*

6.1 Correct RX coupling

Use the NFC Cockpit to determine the value of R_{Rx}:

1. DPC: <Start Calibration>
2. <Load Protocol>
3. Use unloaded antenna (typical VDDPA = 5.7 V).
4. Read H_ATT_VALUE, RX_CONTROL_STATUS register (0x28), bit 3 to bit 8.

The target HF_ATT_VALUE must be 40 dec.

Increase R_{Rx}, if the HF_ATT_VALUE is too high.

Decrease R_{Rx}, if the HF_ATT_VALUE is too low.

7 References

[1] PN5190 NFC frontend, Product data sheet – https://www.nxp.com/docs/en/data-sheet/PN5190.pdf
[2] ISO/IEC 14443 standard, part 1 to part 4 – https://www.iso.org/home.html
[3] ISO/IEC 10373-6 – https://www.iso.org/home.html
[4] NFC Forum specifications – https://nfc-forum.org/
[5] BSI TR-03105 Conformity Tests for Official Electronic ID Documents, Part 2 (PICC) and Part 4 (PCD) – https://www.bsi.bund.de/DE/Home/home_node.html
[6] EMV Contactless Interface Specification, Version 3.0, February 2018 – https://www.emvco.com/
[7] Rohde & Schwarz – https://www.rohde-schwarz.com/nl/home_48230.html
[8] MiniVNA Pro – http://miniradiosolutions.com/
[9] Simulation tool RFSIM99 – http://www.electroschematics.com/835/rfsim99-download/
[10] VNA/J from Dietmar Krause, DL2SBA – https://vnaj.dl2sba.com/
[11] NFC Antenna Design Hub – https://www.nxp.com/products/rfid-nfc/nfc-hf/nfc-readers/nfc-antenna-design-hub:NFC-ANTENNA-DESIGN-TOOL
[12] WaveChecker, CTC Advanced – https://ctcadvanced.com/consulting/
[13] AWG Keysight 33511B – https://www.keysight.com/nl/en/home.html
[14] FIME Contactless SmartSpy – https://www.fime.com
[15] WavePlayer, CTC Advanced – https://ctcadvanced.com/consulting/
[16] NXP FireArmPositioner – https://www.nxp.com/downloads/en/nxp/software/SW6104.zip
[17] NFC Antenna Design Hub – NFC Antenna Design Hub
[18] PN5180 Antenna design tools – PN5180 Antenna design tools
[19] AN12551 PN5190 design-in recommendations – https://www.nxp.com/docs/en/application-note/AN12551.pdf
[20] PN5190 Evaluation board (PNEV5190BP) – https://www.nxp.com/products/rfid-nfc/nfc-hf/nfc-readers/development-board-for-pn5190:PNEV5190BP
[21] Murata capacitor specifications – https://www.murata.com/

8 Revision history

Table 6. Revision history

Document ID	Release date	Description
AN12549 v.1.3	14 March 2024	• Section 3.3.5 "PN5190 supply capacitors": added. • Section 4.6 "Measure the real circuit": updated the last paragraph. • Section 4.10 "RX circuit" corrected typos.
AN12549 v.1.2	25 October 2022	• Package name corrected from HVQFN to official naming VFLGA40
AN12549 v.1.1	23 April 2021	• Section 3.4 "Layout recommendation for VFLGA40" added
AN12549 v.1.0	20 January 2021	• Initial version

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Contents

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