AN12426

LA9310 Design Checklist

Rev. 0 — 05/2022

Application Note

Contents

1 About this document

This document provides recommendations for new designs based on the Layerscape Access LA9310 family of products. This device family uses an integrated programmable baseband processor primarily used to implement the low-PHY protocols of a 5G stack. It is typically used in a 2x2 ORAN Radio Unit, as a low-cost 5G repeater or as a controller of a high-performance repeater; as a network listening module; or for general-purpose DSP functionality. It receives analog I/Q signals from a radio frequency device; samples them with its analog to digital converter; performs digital signal processing with its vector signal processing engine; and then sends results over PCI Express to a host processor; while simultaneously performing the opposite path in the transmit direction using its digital to analog converter. The chain is supervised by an ARM Cortex-M4 processor.

The LA9310 device is built for ultra-low power consumption and its small 21 x 21 mm package can easily fit on an M.2 card. LA9310 features an ARM M4 core operating up to 307.2MHz, an innovative programmable signal processing accelerator operating up to 614 MHz, and integrated high-speed analog/digital data converters capable of sampling at up to 153.6 million samples per second. LA9310 includes on-chip RAM for packet buffering and operates without any external DRAM. The device can boot from the host processor via a x1 PCIe Gen3.

The Layerscape Access products are supported by proven NXP Codewarrior development applications and tools for customer developed solutions. NXP also fosters a variety of third party ecosystem partner for product ready software stacks and integration services.

This document can also be used to debug newly designed systems by highlighting those aspects of a design that merit special attention during initial system startup.

2 Before you begin

Ensure you are familiar with the following NXP collateral before proceeding:

- *LA9310 Data Sheet* (LA9310)
- *LA9310 Reference Manual* (LA9310RM) (LA9310RM)
- *LA9310 Chip Errata* (LA9310CE)

3 Simplifying the first phase of design

Before designing a system with the chip, it is recommended that the designer be familiar with the available documentation, software, models, and tools.

The following figure shows the major functional units of the LA9310 chip.

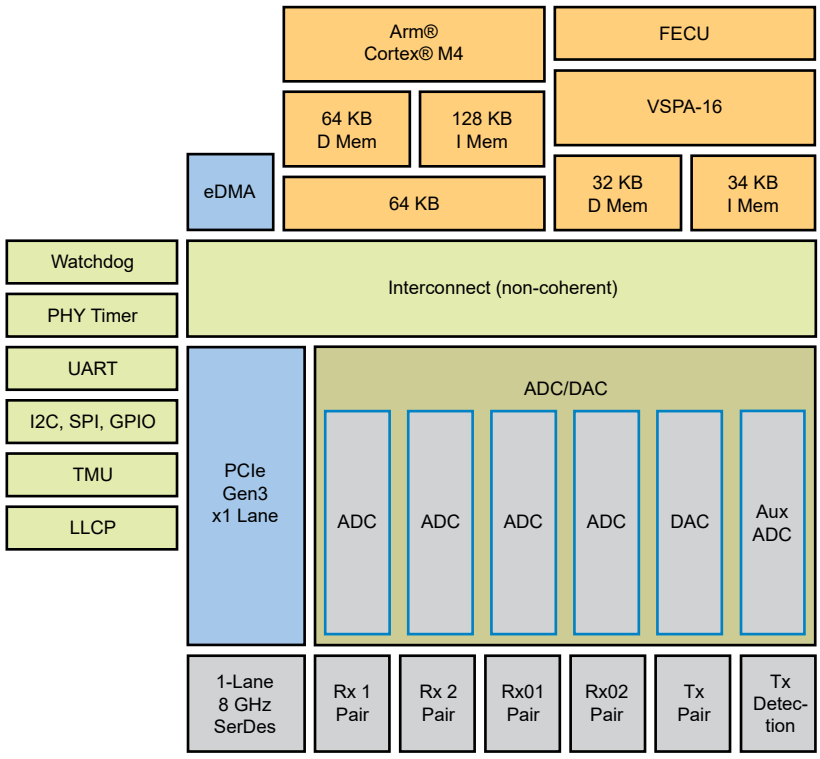


Figure 1. LA9310 block diagram

3.1 Recommended resources

This table lists helpful tools, training resources, and documentation, some of which may be available only under a non-disclosure agreement (NDA). Contact your local field applications engineer or sales representative to obtain a copy.

Table 1. Helpful tools and references

ID	Name	Location
	Related collateral	
LA9310CE	*LA9310 Chip Errata* **NOTE** This document describes the latest fixes and workarounds for the chip. It is strongly recommended that this document be thoroughly researched prior to starting a design with the chip.	Contact your NXP representative
LA9310	*LA9310 Data Sheet*	Contact your NXP representative
LA9310RM	*LA9310 Reference Manual*	Contact your NXP representative
AN4311	*SerDes Reference Clock Interfacing and HSSI Measurements Recommendations*	www.nxp.com

Table continues on the next page...

Table 1. Helpful tools and references (continued)

ID	Name	Location
Models		
IBIS	To ensure first path success, NXP strongly recommends using the IBIS models for board level simulations, especially for SerDes characteristics.	Contact your NXP representative
BSDL	Use the BSDL files in board verification.	
Flotherm	Use the Flotherm model for thermal simulation. Especially without forced cooling or constant airflow, a thermal simulation should not be skipped.	
Available training		
—	Our third-party partners are part of an extensive alliance network. More information can be found at www.nxp.com/alliances.	www.nxp.com/alliances

3.2 Product revisions

The following table provides a cross-reference to match the revision code in the processor version register to the revision level marked on the device.

Table 2. Revision level to part marking cross-reference

Part	Device Revision	Arm® Cortex®-M4 MPCore Processor Revision	Arm Core Main ID Register	System Version Register Value	Note
LA9310S7 S11AA	A0	r0p1	0x410FC241	0x81410010	Standard temp
LA9310X7 S11AA	A0	r0p1	0x410FC241	0x81410010	Extended temp

4 Power design recommendations

4.1 Power pin recommendations

The following table provides design recommendations related to termination of power and ground pins.

Table 3. Power and ground pin termination checklist

Signal name	Signal type	Used		Not used	Completed
V_{DD}	I	Core and platform supply voltage	0.9 V (± 30 mV)	Must remain powered	
GND	I	Ground			
SD_SV_{DD}	I	Main power supply for internal circuitry of SerDes and	0.9 V (± 90 mV)	Must remain powered	

Table continues on the next page...

Table 3. Power and ground pin termination checklist (continued)

Signal name	Signal type	Used		Not used	Completed
		pad power supply for SerDes receivers			
SD_X_{DD}	I	Pad power supply for SerDes transmitter	1.35 V (± 67 mV)	Must remain powered	
SD_GND	I	SerDes GND			
OV_{DD}	I	Power supply for RFCTL, PPS, LLCP, DSPI, I2C, DFT, JTAG and General Purpose peripherals	1.8 V (± 90 mV)	Must remain powered	
TH_V_{DD}	I	Thermal Monitor Unit supply	1.8 V (± 90 mV)	Must remain powered	
AV_{DD}_PLAT	I	PLL supply voltage (core PLL and platform)	1.8 V filtered (± 90 mV) Independent supplies derived from board 1.8 V	Must remain powered	
AV_{DD}_SD_PLL	I	PLL supply voltage (SerDes, filtered from XVDD)	1.35 V (± 67 mV)	Must remain powered	
AFE_OTV_{DD}	I	IQ_DAC High Voltage Supply	1.8 V filtered (± 90 mV)	Must remain powered	
AFE_OMV_{DD}	I	Aux ADC High Voltage Supply	1.8 V filtered (± 90 mV)	Must remain powered	
AFE_SV_{DD}	I	ADC Analog Supply	0.9 V filtered (± 30 mV)	Must remain powered	
AFE_CV_{DD}	I	AFE Clock Supply	0.9 V filtered (± 30 mV)	Must remain powered	

4.2 Maximum supply pin current consumption

The following table describes the maximum current for various supply pins of the SoC at 105 ºC.

Table 4. Maximum current consumption

Supply pin	Voltage (V)	Maximum current at 105 °C junction temperature	Unit
VDD	0.9	1190	mA
SD_SVDD	0.9	137	mA
OVDD	1.8	30	mA
AVDD_PLAT	1.8	7	mA
SD_XVDD	1.35	70	mA
AVDD_SD_PLL	1.35	23	mA
AFE_OTVDD	1.8	21	mA
AFE_OMVDD	1.8	2	mA
AFE_SVDD	0.9	54	mA
AFE_CVDD	0.9	54	mA
TH_VDD	1.8	12	mA
Notes: 1. Maximum current is provided for power supply design sizing.			

4.3 Power system-level recommendations

The following table provides system-level power design recommendations.

Table 5. Power design system-level checklist

Item	Completed
General	
Ensure to meet all of the requirements in the data sheet, including power sequencing, power down requirements, THERMAL and MAXIMUM power dissipation, I/O power dissipation, and power on ramp rate.	
Ensure the PLL filter circuit is applied to AV_{DD}_PLAT, and AV_{DD}_SD_PLL. See the "PLL power supply filtering" section of this table.	
General power supply decoupling	
Because of the large address and data buses and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the chip system, and the chip itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each VDD and OVDD, pins of the device. These decoupling capacitors should receive their power from separate VDD, OVDD and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part. These capacitors should have a value of 2.2 µF >=10 V . Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance, preferably 0201 sizes.	

Table continues on the next page...

Table 5. Power design system-level checklist (continued)

Item	Completed
As presented in Core and platform supply voltage filtering, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the VDD, VDDC and other planes (for example, VDD and OVDD) to enable quick recharging of the smaller chip capacitors.	
SerDes block power supply decoupling	
The SerDes block requires a clean, tightly regulated source of power (SD_SVDD and SD_XVDD) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below: 1. The board should have at least 1 x 2.2 µF 0201 SMT ceramic chip capacitor placed as close as possible to each supply ball of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible. 2. Between the device and any SerDes voltage regulator, there should be a lower bulk capacitor. For example, a 10 µF, low ESR SMT tantalum or ceramic capacitor. There should also be a higher bulk capacitor. For example, a 100 µF - 300 µF low ESR SMT tantalum or ceramic capacitor. **NOTE** Only SMT capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.	
Core and platform supply voltage filtering	
The V_{DD} supply is normally derived from a linear regulator or switching power supply that can regulate its output voltage very accurately despite changes in current demand from the chip within the regulator's relatively low bandwidth. Several bulk decoupling capacitors must be distributed around the PCB to supply transient current demand above the bandwidth of the voltage regulator. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure a quick response time. They should also be connected to the power and ground planes through two vias to minimize inductance. Customers should work directly with their power regulator vendor for best values and types of bulk capacitors. As a guideline for customers and their power regulator vendors, NXP recommends that these bulk capacitors be chosen to maintain the positive transient power surges to less than + 30 mV (negative transient undershoot should comply with specification of -30 mV) for current steps of up to 2A with a slew rate of 1.5 A/µs. These bulk decoupling capacitors will ideally supply a stable voltage for current transients into the megahertz range. Above that, see Decoupling recommendations for further decoupling recommendations.	
It is recommended that medium (ceramic) and large bulk (POS, aluminum) capacitors for V_{DD} should be placed in the corner sections of the chip. This will avoid blocking signal routing.	
For small decoupling capacitors, it is recommended to have the following mix of capacitors distributed across the entire BGA array: • V_{DD}. A quantity of even mix of 4.7 µF, 0.1 µF and 1.0 µF . See the "Core and platform supply voltage filtering" Note: All capacitors should be rated 6.3 V or higher and 0201 size	
PLL supply voltage (platform filtered from OV_{DD}) power supply filtering	

Table continues on the next page...

Table 5. Power design system-level checklist (continued)

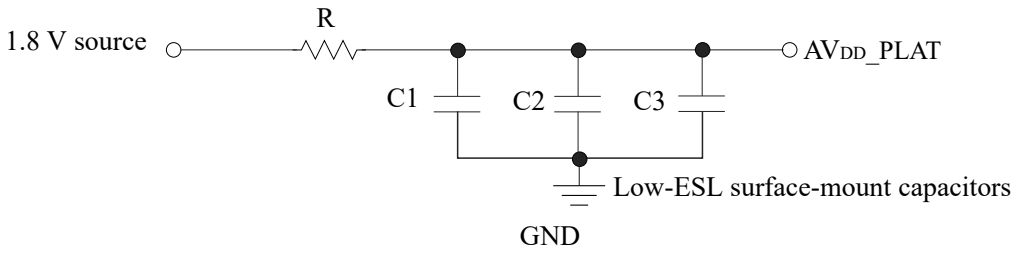
Item	Completed
All PLLs are provided with power through independent power supply pins AV_{DD}_PLAT voltage must be derived directly from a 1.8 V voltage source, through a low-frequency filter. For the AV_{DD}_PLAT filter, provide a circuit as illustrated in the following figure. Where: • R = 5 Ω ± 5% • C1 = 10 µF ± 10%, 0402, X5R, with ESL ≤ 0.5 nH • C2 = 1.0 µF ± 10%, 0402, X5R, with ESL ≤ 0.5 nH • C3 = 0.22 µF ± 10%, 0201, X5R, with ESL ≤ 0.5 nH  **Figure 2. Platform PLL AV_{DD} power supply filter circuit** Note the following: • Each AV_{DD} must have its own independent filter circuit. • If done properly, it is possible to route directly from the capacitors to the AV_{DD} pins, without the added inductance of vias. 1. Place the filter on the bottom side as close to the C5 pin as possible. 2. Use an area fill and not a single trace to connect the filter to the pin. For this filter, keep at least 3 routing lanes wide as far as possible. It will have to neck down near the pin where we may need to go to two or one routing lanes. • It is recommended that an area fill or power plane split be provided for a low-impedance profile, which keeps nearby crosstalk noise from inducing unwanted noise. • Place each circuit as close as possible to the specific AV_{DD} pin to minimize noise coupled from nearby circuits. • **Caution:** These filters are mandatory extension of the PLL circuitry and are compliant with the device specifications. Any deviation from the recommended filters is done at the user's risk.	
PLL supply voltage (SerDes, filtered)	
If SerDes is enabled, ensure the PLL filter circuit is applied to the AV_{DD}_SD_PLL pin. Otherwise, a filter is not required. Even if an entire SerDes module is not used, the power is still needed to the AVDD pins. However, instead of using a filter, it needs to be connected to the SD_XVDD rail through a 0 Ω resistor. See the "PLL power supply filtering" section of this table.	

Table continues on the next page...

Table 5. Power design system-level checklist (continued)

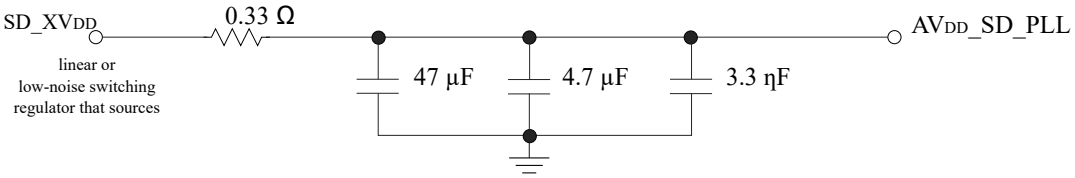
Item	Completed
Ensure the PLL filter circuits are placed as close to AV_{DD}_SD_PLL as possible. If specified, a small cap for the filter should be placed directly at the pin. If no small cap for the filter is specified, consider at least a standard decoupling cap, such as 0.1 µF.	
The AV_{DD}_SD_PLL signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, ensure the power supplied to the PLL is filtered using a circuit similar to the one shown in the following figure. The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, one for each side of the AV_{DD} pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced. Note the following: • Each AV_{DD} must have its own independent filter circuit. • The 3.3 ηF must be located at the AV_{DD} pin. • It is recommended that an area fill or power plane split be provided for a low-impedance profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • A 4.7 µF and a 47µF 0805 XR5 or 0603 XR7 or smaller, and 3.3 ηF 0402 or 3.3 ηF 0201 capacitor are recommended. The size and material type are important. A 0.33 Ω ± 1% resistor is recommended. • **Caution**: These filters are a necessary extension of the PLL circuitry and are compliant with the device specifications. Any deviation from the recommended filters is done at the user's risk.  **Figure 3. SerDes PLL AV_{DD}_SD_PLL power supply filter circuit**	
SerDes SD_SV_{DD} and SD_XV_{DD} power supply filtering	
For the linear or low-noise switching regulator, 10 mVp-p, 50 kHz to 500 MHz is the noise goal. All traces should be kept short, wide, and direct. Use small area fill, if possible. The goal is to lower the impedance of this net, therefore, lowering the noise. SD_SV_{DD}/SD_XV_{DD} may be supplied by a linear or low noise/ripple switching regulator. Example solution for SD_SV_{DD} and SD_XV_{DD} filtering, sourced from a linear or low noise switching regulator, are illustrated below.	

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Table 5. Power design system-level checklist (continued)

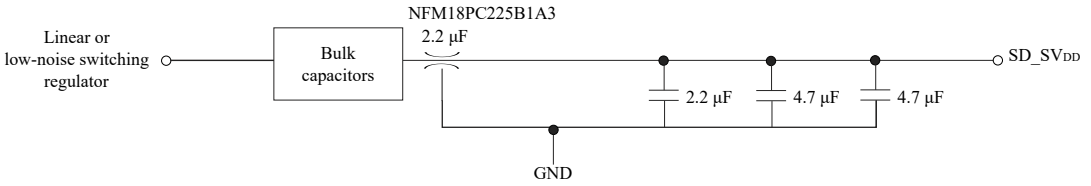
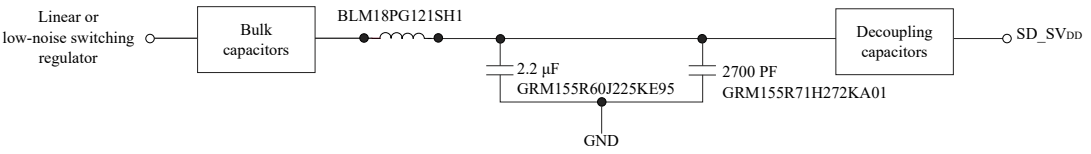
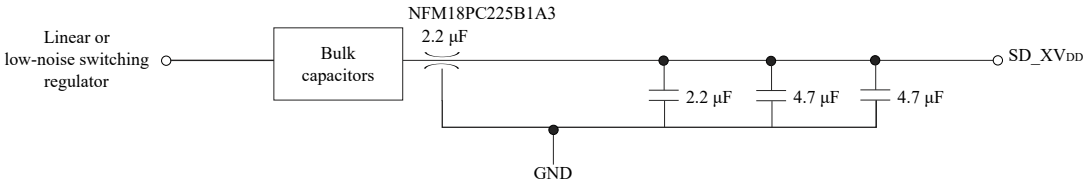
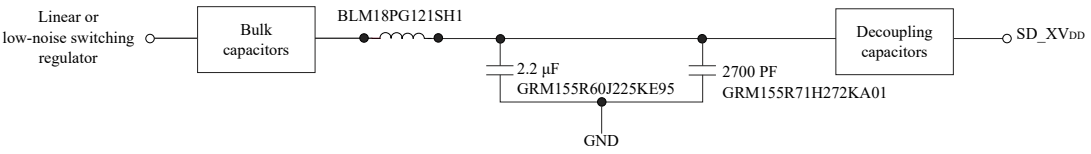
Item	Completed
 **Figure 4. SD_SV_{DD} power supply filter circuit**	
 **Figure 5. Alternate SD_SV_{DD} power supply filter circuit**	
 **Figure 6. SD_XV_{DD} power supply filter circuit**	
 **Figure 7. Alternate SD_XV_{DD} power supply filter circuit**	
Note the following: • See Section 3.5, "Power-on ramp rate," in the data sheet for maximum SD_SV_{DD} and SD_X_{DD} power-up ramp rate. • It is recommended that an area fill or power plane split be provided for a low-impedance profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • Each supply must have their own independent filter circuit. The SD_SV_{DD} must not be filtered off the VDD power supply as that may have substantial noise from the cores. • Place each circuit as close as possible to the specific set of pins being supplied to minimize noise coupled from nearby circuits. • Located at each pin should have a decoupling capacitor, as mentioned in the "General power supply decoupling" section.	

Table continues on the next page...

Table 5. Power design system-level checklist (continued)

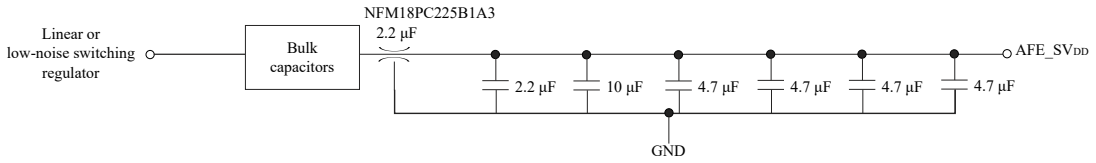
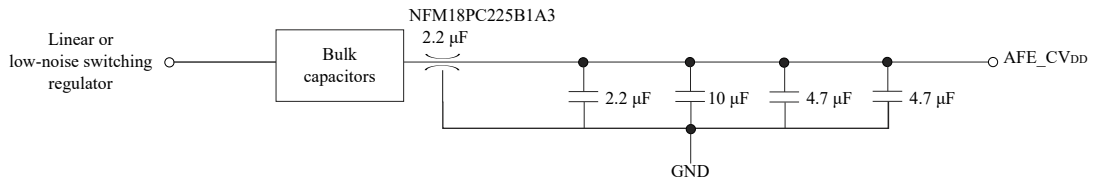
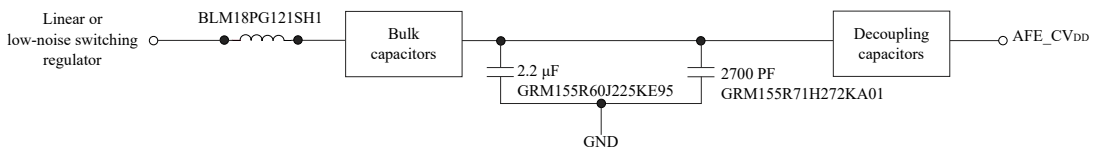
Item	Completed
AFE_SV_{DD} power supply filtering	
AFE_SV_{DD} may be supplied by a linear or low noise switching regulator. The following two figures, illustrate the example solutions for the AFE_SV_{DD} filtering, where AFE_SV_{DD} is sourced from a linear or low noise switching regulator. Any of the following solution can be used as per the requirements.  **Figure 8. AFE_SV_{DD} power supply filter circuit** Note the following: • For maximum AFE_SV_{DD} power-up ramp rate, See LA9310 data sheet. • Besides a linear regulator, a low-noise, dedicated switching regulator can also be used. The noise goal is 10 mVp-p, 50 kHz - 500 MHz. • **Caution**: These filters are a necessary extension of the PLL circuitry and are compliant with the device specifications. Any deviation from the recommended filters is done at the user's risk.	
AFE_CV_{DD} power supply filtering	
AFE_CV_{DD} may be supplied by a linear or low noise switching regulator. The following two figures, illustrate the example solutions for the AFE_CV_{DD} filtering, where AFE_CV_{DD} is sourced from a linear or low noise switching regulator. Any of the following solution can be used as per the requirements.  **Figure 9. Primary AFE_CV_{DD} power supply filter circuit**  **Figure 10. Alternate AFE_CV_{DD} power supply filter circuit**	

Table continues on the next page...

Table 5. Power design system-level checklist (continued)

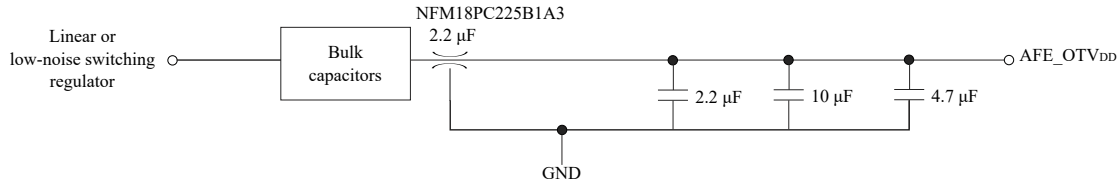
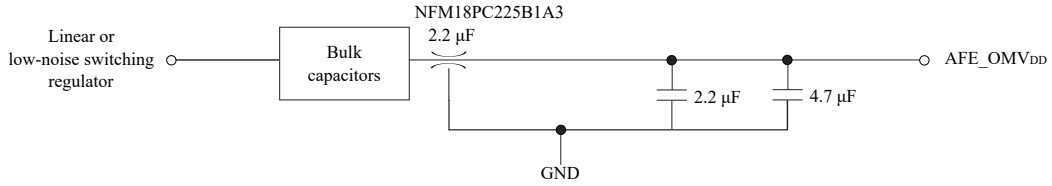
Item	Completed
Note the following: • For maximum AFE_CV_{DD} power-up ramp rate, see LA9310 Data sheet. • Besides a linear regulator, a low-noise, dedicated switching regulator can also be used. The noise goal is 10 mVp-p, 50 kHz - 500 MHz. • **Caution**: These filters are a necessary extension of the PLL circuitry and are compliant with the device specifications. Any deviation from the recommended filters is done at the user's risk	
AFE_OTV_{DD} power supply filtering	
 **Figure 11. AFE_OTV_{DD} power supply filter circuit** Note the following: • For maximum AFE_OTV_{DD} power-up ramp rate, see LA9310 Data sheet. • Besides a linear regulator, a low-noise, dedicated switching regulator can also be used. The noise goal is 10 mVp-p, 50 kHz - 500 MHz.	
AFE_OMV_{DD} power supply filtering	
 **Figure 12. AFE_OMV_{DD} power supply filter circuit** Note the following: • For maximum AFE_OMV_{DD} power-up ramp rate, see LA9310 Data sheet. • Besides a linear regulator, a low-noise, dedicated switching regulator can also be used. The noise goal is 10 mVp-p, 50 kHz - 500 MHz.	
VREF_RX_P/VREF_RX_N signal filtering recommendation	
The VREF_RX_P/VREF_RX_N signals may be supplied by a linear or low noise switching regulator. This figure illustrates the example solutions for the VREF_RX_P / VREF_RX_N signal filtering.	

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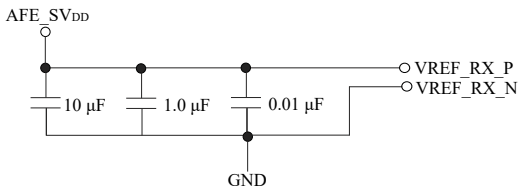
Table 5. Power design system-level checklist (continued)

Item	Completed
 **Figure 13. Primary VREF_RX_P/VREF_RX_N signal filter circuit** **Caution**: These filters are a necessary extension of the PLL circuitry and are compliant with the device specifications. Any deviation from the recommended filters is done at the user's risk	

5 Power-on reset recommendations

Various chip functions are initialized by sampling certain signals during the assertion of HRESET_B. These power-on reset (POR) inputs are pulled either high or low during this period. While these pins are generally output pins during normal operation, they are treated as inputs while HRESET_B is asserted. When HRESET_B de-asserts, the configuration pins are sampled and latched into registers, and the pins restore their normal output circuit characteristics.

The following table describes the power-on reset system-level recommendations.

Table 6. Power-on reset system-level checklist

Item	Completed
Ensure HRESET_B is asserted for a minimum of 32 SYSCLK cycles if used.	
Ensure PCI_CLK_P/N is running and stable before HRESET_B is de-asserted. Power-on configuration inputs must be set up 4 cycles before the negation of PORESET_B.	
Ensure PCI_CLK_P/N is running and stable before HRESET_B is de-asserted. Power-on configuration inputs must be held 2 cycles after the negation of HRESET_B.	
NOTE TRST_B should typically be driven asserted concurrently with HRESET_B, though it is recommended that customers control TRST_B separately from HRESET_B if boundary scan testing/operation is required. HRESET_B can be asserted without TRST_B in order to leave TAP configuration setting for a debug session after HRESET_B.	
In cases where a configuration pin has no default, use a 2.2 kΩ pull-up or pull-down resistor for appropriate configuration of the pin.	
Optional: An alternative to using pull-up and pull-down resistors to configure the POR pins is to use a PLD or similar device that drives the configuration signals to the chip when HRESET_B is asserted. The PLD must begin to drive these signals at least four SYSCLK cycles prior to the de-assertion of HRESET_B , hold their values for at least two SYSCLK cycles after the de-assertion of HRESET_B, and then release the pins to high impedance afterward for normal device operation.	

Table continues on the next page...

Table 6. Power-on reset system-level checklist (continued)

Item	Completed
NOTE See the applicable chip data sheet for details about reset initialization timing specifications.	
Configuration settings	
Ensure the Power-on reset configuration settings described in the chip reference manual are selected properly. **NOTE** See the applicable chip reference manual for a more detailed description of each configuration option.	

5.1 Power-on reset configuration pin termination recommendations

Reset configuration signals are sampled at the negation of HRESET_B. However, there is a setup and hold time for these signals relative to the rising edge of HRESET_B, as described in the chip's data sheet.

The following table provides design recommendations related to termination of power-on reset configuration pins. Refer to the timing diagram of the POR sequence in LA9310RM.

Table 7. Power-on reset configuration pin termination checklist

Configuration Pin Name	Functional Pin Name	Description	Used	Note	Completed
CFG_BOOT_SRC[1:0]	TXRX[1:0]	• 0b00: Reserved • 0b01: Reserved • 0b10: I2C EEPROM • 0b11: PCIe host memory	These configuration pins define the boot source.		
CFG_BOOT_HO	GPIO_09	• 0b0: Reserved • 0b1: Boot of Arm M4 core proceeds immediately upon reset state machine reaching SYSREADY	– normal boot with M4 executing BootROM and performing handshake		
CFG_RST_HNDSHK	PA_EN	HW/SW Handshake • 0b0: Reserved • 0b1: The Reset FSM pauses to allow software to perform necessary configuration.	– normal boot with M4 executing BootROM and performing handshake		
CFG_TEST_PORT_DIS	LNA1_EN	Reserved for internal use only.		2	

Table continues on the next page...

Table 7. Power-on reset configuration pin termination checklist (continued)

Configuration Pin Name	Functional Pin Name	Description	Used	Note	Completed
CFG_WRM_RSTB	PPS_OUT	Warm Reset (active low) (consumed by BootROM only) • 0b0: Reset has been asserted after a functional mode has been reached previously (and specifically after memories have been initialized). Power was not removed prior to the reset assertion. Memory initialization steps may be skipped. • 0b1: Cold reset. Memories must be initialized.			
CFG_SYSRDY_EVT	SPI_MOSI	SYSREADY Event (active low) (consumed by BootROM only) • 0b0: Boot Sequence determines SYSREADY state via EPU event which wakes M4 from WFE • 0b1: Boot Sequence determines SYSREADY state by polling Reset FSM state			
CFG_PCIE_GEN	LNA2_EN	• 0b0: PCIe interface will allow negotiation upto PCIe Gen2 (5 Gbit/s) frequencies. • 0b1: PCIe interface will allow negotiation upto PCIe Gen3 (8 Gbit/s) frequencies.	Maximum training rate of PCIe Controller 1	1	

Notes:

1. A 2.2 kΩ pull-down resistor is recommended to overpower the intrnal pull-up if it is needed.
2. This pin should be pulled up during reset.

6 Connection recommendations

The following are the connection recommendations:

- To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unless otherwise noted in this document, all unused active low inputs should be tied to VDD as required. All unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external VDD and GND pins of the device.
- Critical analog signal - IREF_TX
  - The pin IREF_TX is a very sensitive reference node that affects directly the DAC's dynamic performance if coupled to active signals such as TX_I_P/N , TX_Q_P/N or digital lines. It is recommended to place a 2.67K 0201 size PD 1% resistor (E96 series resistor) directly between the pad IREF_TX and the adjacent AFE_GND pad.

7 Interface recommendations

This section describes design recommendations for different interfaces of the chip.

7.1 Clocking pin signaling recommendations

The DCS_CLK_P/DCS_CLK_N input pair requires an input clock frequency of 122.88 MHz or 153.6 MHz. HCSL signaling is recommended for differential SYSCLK input.

Table 8. Clocking pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
DCS_CLK_P	I	DCS PLL and PLATFORM PLL Reference Clock + (122.88 MHz or 153.6 MHz).	Must always be connected.	
DCS_CLK_N	I	DCS PLL and PLATFORM PLL Reference Clock + (122.88 MHz or 153.6 MHz).	Must always be connected.	

7.2 System control pin signaling recommendations

The following table provides recommendations on termination of system control pins of the SoC.

Table 9. System control pin signaling checklist

Signal Name	IO type	Used	Not Used	Completed
HRESET_B	I	This pin is required to be asserted as per the applicable chip data sheet, in relation to minimum assertion time and during power up/power down. It is an input-only pin and must be asserted to sample power-on configuration pins.		

7.3 UART interface recommendations

One UART module is included in LA9310 that support one 16550-compatible two-pin UART instance.

Table 10. UART pin termination

Signal Name	I/O type	Used	Not Used	Completed
UART1_SIN /SPI_CS1_B	I	UART1	Pull low through a 2 kΩ -10 kΩ resistor to GND.	
UART1_SOUT/ SPI_CS2_B	O		Can be left unconnected.	

7.4 I2C pin termination recommendations

The following table provides recommendations on termination of I2C pins of the SoC.

Table 11. I2C pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
IIC1_SCL	IO	This pin is an open-drain signal. It is recommended that a weak pull-up resistor be placed on this pin to the respective power supply. For Pull-up resistor sizing, see Equation1 and Equation2 in I2C specification (UM10204), Rev 6.	Pull high through a 2 kΩ -10 kΩ resistor to OV_{DD}.	

Table continues on the next page...

Table 11. I2C pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
IIC1_SDA	IO	This pin is an open-drain signal. It is recommended that a weak pull-up resistor be placed on this pin to the respective power supply. For Pull-up resistor sizing, see Equation1 and Equation2 in I2C specification (UM10204), Rev 6.	Pull high through a 2 kΩ -10 kΩ resistor to OV_{DD}.	

7.5 DCS interface pin termination recommendations

The following table describes the design recommendations for termination of DCS interface pins of the SoC.

Table 12. DCS interface pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
RO0_I_P RO0_I_N	I	Analog Observation (I+/-) Vin 0, Used as needed	Should be terminated to GND	
RO0_Q_P RO0_Q_N	I	Analog Observation (Q+/-) Vin 0, Used as needed	Should be terminated to GND	
RO1_I_P RO1_I_N	I	Analog Observation (I+/-) Vin 1, Used as needed	Should be terminated to GND	
RO1_Q_P RO1_Q_N	I	Analog Observation (I+/-) Vin 1, Used as needed	Should be terminated to GND	
RX0_I_P RX0_I_N	I	Analog Receive (I+/-) Vin 0, Used as needed	Should be terminated to GND	
RX0_Q_P RX0_Q_N	I	Analog Receive (Q+/-) Vin 0, Used as needed	Should be terminated to GND	
RX1_I_P RX1_I_N	I	Analog Receive (I+/-) Vin 1, Analog Receive (I+) Vin 1	Should be terminated to GND	
RX1_Q_P RX1_Q_N	I	Analog Receive (Q+/-) Vin 1, Analog Receive (Q+) Vin 1	Should be terminated to GND	
VREF_RX_P VREF_RX_N	I	Analog Rx Voltage Ref +/-	Should be terminated to GND	
TX_DET	I	Analog Auxiliary input (Tx Power Detect)	Should be terminated to GND	
IREF_TX	I	Connect to 2.67 KΩ to GND		

Table continues on the next page...

Table 12. DCS interface pin termination checklist (continued)

Signal Name	I/O type	Used	Not Used	Completed
TX_I_P TX_I_N	O	Analog Transmit (I+/-) Iout, Used as needed	Can be left unconnected.	
TX_Q_P TX_Q_N	O	Analog Transmit (Q+/-) Iout, Used as needed	Can be left unconnected.	

7.5.1 ADC input and DAC output Signals

The data converter analog input and output signals should be routed as differential lines on the PCB and package substrate.

Attention should be paid to good symmetry and length matching. Sharp turns should be avoided but if that is not possible the turns should be rounded or beveled. To avoid coupling with other high speed signals or clocks proper separation or grounded shields should be used. Solid ground plane should be maintained underneath the traces. If filtering is included on the PCB between the data converter and the RX or TX device, symmetrical PCB layout should be used for the filter components.

These bulk decoupling capacitors will ideally supply a stable voltage for current transients into the megahertz range. Above that, see Decoupling recommendations for further decoupling recommendations. The external DAC load resistors can act as termination for the PCB trace and should be placed close to the device. The transmission line impedance should be designed based on the chosen DAC load resistor value.

7.6 LLCP interface pin termination recommendations

The following table describes the design recommendations for termination of light-weight LVDS communication protocol (LLCP) interface pins of the SoC.

Table 13. LLCP1 interface pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
LLCP_DIN_P LLCP_DIN_N	I	Place 100 Ω parallel termination on differential signals near LA9310	Connect to GND	
LLCP_STIN_P LLCP_STIN_N	I	Place 100 Ω parallel termination on differential signals near LA9310	Connect to GND	
LLCP_DOUT_P LLCP_DOUT_N	O	Place 100 Ω parallel termination on differential signals near RFIC	Can be left unconnected.	
LLCP_STOUT_P LLCP_STOUT_N	O	Place 100 Ω parallel termination on differential signals near RFIC	Can be left unconnected.	

7.7 SPI interface pin termination recommendations

The following tables describe the design recommendations for termination of SPI interface pins of the SoC.

Table 14. SPI interface pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
SPI_CS0_B	O	SPI Chip Select. Pull-up resistor 4.7 kΩ to OVDD recommended.	Can be left unconnected.	

Table continues on the next page...

Table 14. SPI interface pin termination checklist (continued)

Signal Name	I/O type	Used	Not Used	Completed
SPI_CS1_B /UART1_SIN	O	SPI Chip Select. Pull-up resistor 4.7 kΩ to OVDD recommended.	Can be left unconnected.	
SPI_CS2_B / UART1_SOUT	O	SPI Chip Select. Pull-up resistor 4.7 kΩ to OVDD recommended.	Can be left unconnected.	
SPI_CS3_B /GPIO_16	O	SPI Chip Select. Pull-up resistor 4.7 kΩ to OVDD recommended.	Can be left unconnected.	
SPI_CLK	O	SPI Clock	Can be left unconnected.	
SPI_MOSI / cfg_sysrdy_evt	O	SPI MOSI - Master Out / Slave In	Refer Table 7	
SPI1_MISO	I	SPI MISO - Master In / Slave Out	If this pin is not used, it should be pulled to its inactive state	

7.8 RFCTL pin termination recommendations

The following tables describe the design recommendations for termination of RFCTL interface pins of the chip.

Table 15. RFCTL interface pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
LNA1_EN /GPIO_11 / cfg_test_port_dis	O	Used as PHY Timer Triggers.	Refer Table 7	
LNA2_EN /GPIO_10 / cfg_pcie_gen	O	Used as PHY Timer Triggers.	Refer Table 7	
LNA3_EN /GPIO_09 / cfg_boot_ho	O	Used as PHY Timer Triggers.	Refer Table 7	
PA_EN /GPIO_12 / cfg_rst_hndshk	O	Used as PHY Timer Triggers.	Refer Table 7	
TXRX0 /GPIO_07 / cfg_boot_src0	O	Used as PHY Timer Triggers	Refer Table 7	
TXRX1 /GPIO_08 / cfg_boot_src1	O	Used as PHY Timer Triggers	Refer Table 7	

7.9 PHY Timer pin termination recommendations

The following tables describe the design recommendations for termination of PHY Timer interface pins of the chip.

Table 16. PHY Timer interface pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
PPS_IN /GPIO_04	I/O	Pulse Per Second In	When programmed as output type, no termination is required.	
PPS_OUT /GPIO_03 / cfg_wrm_rstb	I/O	Pulse Per Second Out	Refer Table 7	

7.10 GPIO pin termination recommendations

General purpose input/output (GPIO) pins are multiplexed with other functionalities and determined by RCW at the power on reset time.

Table 17. GPIO pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
GPIO_01/ IIC1_SDA	I/O	Used as needed	When programmed as output type, no termination is required.	
GPIO_02/ IIC1_SCL	I/O	Used as needed	When programmed as output type, no termination is required.	
GPIO_03/ PPS_OUT / cfg_wrm_rstb		Used as needed	Refer Table 7	
GPIO_04/ PPS_IN	I/O	Used as needed	When programmed as output type, no termination is required.	
GPIO_05	I/O	Used as needed	When programmed as output type, no termination is required.	
GPIO_06	I/O	Used as needed	When programmed as output type, no termination is required.	
GPIO_07/ TXRX0 / cfg_boot_src0	I/O	Used as needed	Refer Table 7	
GPIO_08/ TXRX1 / cfg_boot_src1	I/O	Used as needed	Refer Table 7	
GPIO_09/ LNA3_EN / cfg_boot_ho	I/O	Used as needed	Refer Table 7	
GPIO_10/ LNA2_EN / cfg_pcie_gen	I/O	Used as needed	Refer Table 7	
GPIO_11/ LNA1_EN / cfg_test_port_dis	I/O	Used as needed	Refer Table 7	

Table continues on the next page...

Table 17. GPIO pin termination checklist (continued)

Signal Name	I/O type	Used	Not Used	Completed
GPIO_12/ PA_EN / cfg_rst_hndshk	I/O	Used as needed	Refer Table 7	
GPIO_16/ SPI_CS3_B	I/O	Used as needed	When programmed as output type, no termination is required.	
GPIO_17	I/O	Used as needed	When programmed as output type, no termination is required.	
GPIO_18	I/O	Used as needed	When programmed as output type, no termination is required.	
GPIO_19 /ASLEEP	I/O	Used as needed	When programmed as output type, no termination is required.	

7.11 Programmable interrupt controller pin termination recommendations

The following table describes the design recommendations for programmable interrupt controller pin termination.

Table 18. Programmable interrupt controller pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
IRQ[0:4]/GPIO_4[3:7]	I	External Interrupt. Each of the IRQ[0:4] pins can be independently configured as either IRQ or GPIO	Pull high through 2 kΩ -10 kΩ resistors to OV_{DD} or program as GPIO output and leave open.	

7.12 Watchdog pin termination recommendations

The following table describes the design recommendations for termination of Watchdog pins of the chip.

Table 19. WDOG pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
WDOG_TOUT/ GPIO_1[7]/ TBGEN1_GPO39	I/O	This pin is assigned to generate an interrupt to the External Host. For example, it can be connected to IRQ pin of LS1046A host device.	When programmed as output type, no termination is required	

7.13 Analog signals pin termination recommendations

The following table describes the design recommendations for termination of analog signal pins of the SoC.

Table 20. Analog signals pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
TD1_ANODE	I/O	These pins should be tied to ground if the diode is not utilized for temperature monitoring.		
TD1_CATHODE	I/O	These pins should be tied to ground if the diode is not utilized for temperature monitoring.		

7.14 SerDes pin signaling recommendations

If a SerDes interface is entirely or partially unused, the unused pins should be terminated as described in the "Not Used" column of the following table. Even if a SerDes interface is unused (partially or entirely), SD_SV_{DD}, SD_X_{DD} and AV_{DD}_SD_PLL must remain powered. If SerDes is entirely not used, AV_{DD}_SD_PLL may be connected to SD_X_{DD} through a 0 Ω resistor (instead of filter circuit).

Table 21. SerDes pin signaling checklist

Signal Name	IO type	Used	Not Used	Completed
SD_SV_{DD}	Power Supply	Filtered 0.9 V (Must be powered even if SerDes interface is not used)		
SD_X_{DD}	Power Supply	Filtered 1.35 V (Must be powered even if SerDes interface is not used)		
AV_{DD}_SD_PLL	PLL Power	Filtered from SD_X_{DD}	0 Ω resistor to SD_X_{DD}	
SD_IMP_CAL_RX	I	This pin requires a 200 Ω 1% pull-up to SD_SV_{DD}.	If the SerDes interface is entirely unused, the unused pin must be left unconnected.	
SD_IMP_CAL_TX	I	This pin requires a 698 Ω 1% pull-up to SD_X_{DD}.	If the SerDes interface is entirely unused, the unused pin must be left unconnected.	
SD1_RX_P	I	Ensure these pins are terminated correctly.	If the SerDes lane is routed to a backplane slot or a PCIe connector, the SerDes pins can be left unterminated even if the link partner card is not present. If SerDes lane is a no-connect, pull down their receiver pins to GND. Then, if the SerDes block is powered, refer to the RM's Unused Lanes section for directions on how to power them down. To power down a SerDes lane, configure the General Control 0 register.	
SD1_RX_N	I			
SD1_TX_P	O	Ensure these pins are terminated correctly.	If the SerDes interface is entirely or partly unused, the unused pins must be left unconnected.	
SD1_TX_N	O			

7.15 JTAG pin termination recommendations

The following table describes the design recommendations for JTAG interface pin termination.

Signal Name	I/O type	Used	Not Used	Completed
TCK	I	If COP is used, connect as needed and strap to OV_{DD} via a 10 kΩ pull up.	Pull high through 2 kΩ -10 kΩ resistors to OV_{DD}.	
TDI	I	This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.	Can be left unconnected.	
TDO	O	This output is actively driven during reset rather than being tri-stated during reset.	Can be left unconnected.	
TMS	I	This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.	Can be left unconnected.	
TRST_B	I	This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.	Tie TRST_B to HRESET_B through a 0 kΩ resistor.	

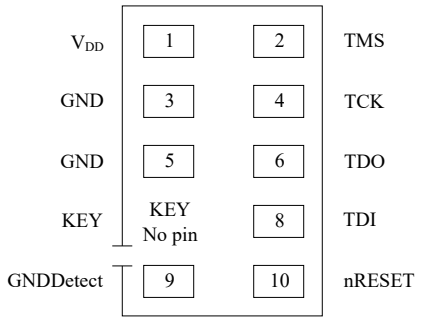
7.15.1 JTAG system-level recommendations

Table 22. JTAG system-level checklist

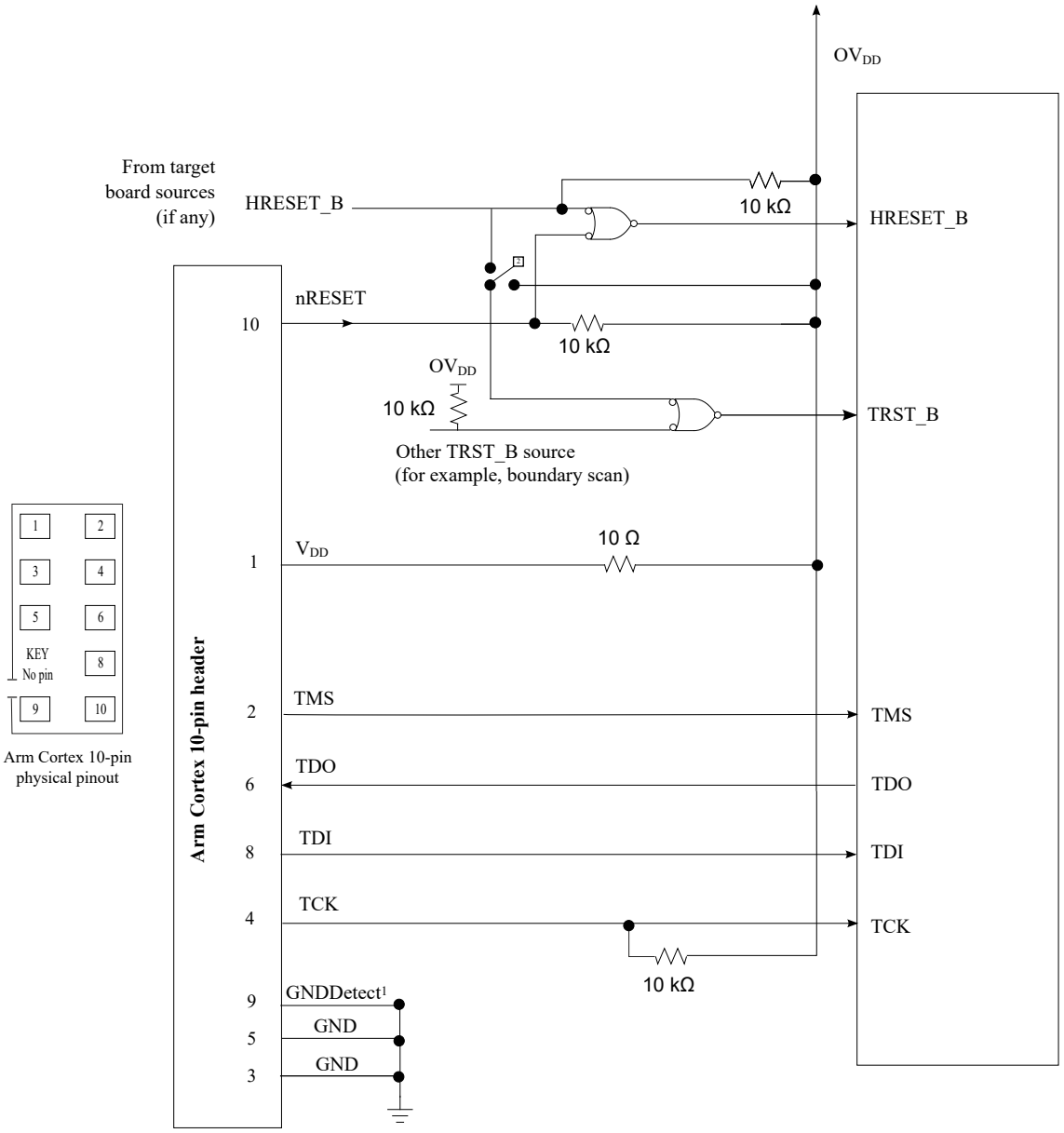
Item	Completed
10-pin header signal interface to JTAG port	
Configure the group of system control pins as shown in Figure 15. **NOTE** These pins must be maintained at a valid deasserted state under normal operating conditions, because most have asynchronous behavior and spurious assertion gives unpredictable results.	
The JTAG port of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The10- pin header connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The 10-pin header interface requires the ability to assert HRESET_B in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the nRESET signal must be merged into these signals with logic.	
Boundary-scan testing	
Ensure that TRST_B is asserted during power up flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. **NOTE** For boundary scan SCAN_MODE_B must be pulled up.	
Follow the arrangement shown in Figure 15 to allow the 10- pin header to assert HRESET_B while ensuring that the target can drive HRESET_B as well.	

Table continues on the next page...

Table 22. JTAG system-level checklist (continued)

Item	Completed
The10-pin interface has a standard header, shown in the following figure. The connector typically has pin 7 removed as a connector key. The signal placement recommended in this figure is common to all known emulators.  **Figure 14. Arm Cortex 10-pin header physical pinout** **NOTE** The 10-pin header adds many benefits such as breakpoints, watch points, register and memory examination/modification, and other standard debugger features. An inexpensive option is to leave the 10-pin header unpopulated until needed.	

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 15. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions, as most have asynchronous behavior and spurious assertion gives unpredictable results.



Note:
1. GNDDetect is an optional board feature. Check with 3rd-party tool vendor.
2. This switch is included as a precaution for BSDL testing. The switch can be open during BSDL testing to avoid accidently asserting the TRST line. If BSDL testing is not peformed, ensure this switch is closed.

Figure 15. JTAG interface connection

8 Revision history

This table summarizes changes to this document.

Table 23. Revision history

Revision	Date	Change
0	05/2022	Initial release

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