AN12333

FS84, FS85 product guidelines

Rev. 8 — 13 March 2024 | Application note

Document information

Information	Content
Keywords	FS84, FS85, power management, functional safety, EMC, ISO pulse, Non-ISO pulse, external components, SPI, I^2C, CRC, Hardware
Abstract	This application note provides guidelines for integrating the FS84/FS85 system basis chip (SBC) family of devices into automotive electronic systems.

1 Introduction

This application note provides guidelines for integrating the FS84/FS85 system basis chip (SBC) family of devices into automotive electronic systems.

2 MCU mapping

The FS84/FS85 family covers a wide range of MCU core voltages from NXP and other MCU suppliers. It functions as standalone power management integrated circuit (PMIC) or in combination with an additional PMIC from NXP or other suppliers.

Table 1 summarizes several MCUs and PMICs compatible with the FS84/FS85 family of parts. This summary does not identify all possible working combinations of the FS84/FS85 with MCUs and PMICs from NXP or other vendors. If you plan to use the FS84/FS85 with an MCU not listed in Table 1, contact your local NXP representative to verify compatibility.

Table 1. MCU mapping

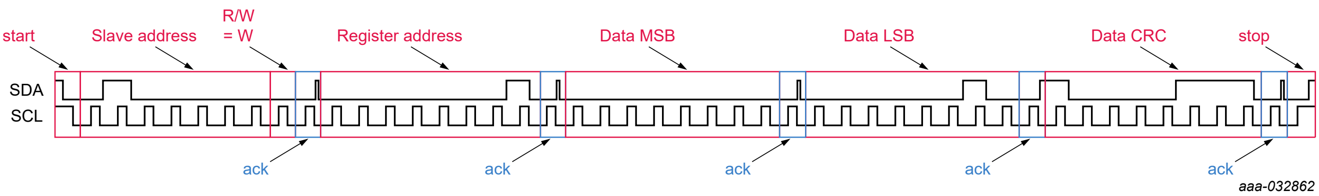
FS84, FS85	MCU	Additional PMIC	Application
FS8530	S32R4x[1]	PF8200 or PF5024 or non NXP	Imaging radar
FS8530	Renesas R-Car V3M	PF8200 or PF5024 or non NXP	Camera
FS8510	Aurix TC2x, TC3x	No	Domain Controller, BMS
FS8430	S32V234[1]	PF8200 or PF5024 or non NXP	Camera
FS8430	S32V3x[1]	PF8200 or PF5024 or non NXP	Camera
FS8430	Renesas R-Car V3M	Non NXP for the DDR	Camera, Lidar
FS8410	S32R274[1]	No	Radar
FS8410	MPC5748G	No	Gateway
FS8400	EYE Q4 + Aurix	PF8200 or PF5024 or non NXP	Camera

[1] NXP MCU

3 Communication with MCU

Refer to UM10204[14] for the complete I^2C bus specification.

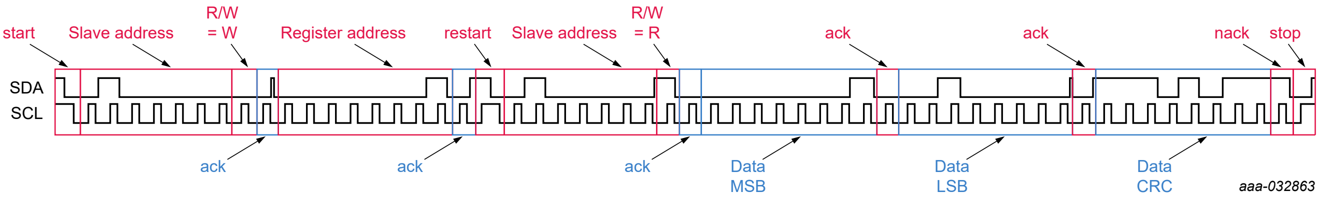
3.1 I^2C write frame



Red is master driving (MCU), blue is slave driving (FS84/FS85)

Figure 1. I^2C frame example with MAIN register M_MODE, address 0x01, write data 0x02

3.2 I²C read frame



Red is master driving (MCU), blue is slave driving (FS84/FS85)

Figure 2. I²C frame example with MAIN register M_MODE, address 0x01, read data

First perform an I²C write access to configure the register address to read, then perform an I²C read access to get data and CRC.

3.3 SPI write frame

For detailed SPI timings, refer to the SPI interface *Electrical characteristics* section of the product data sheet. The MCU is the master driving MOSI and FS84/FS85 is the slave driving MISO. The MISO data is latched at the SCLK rising edge and MOSI data is latched at the SCLK falling edge.

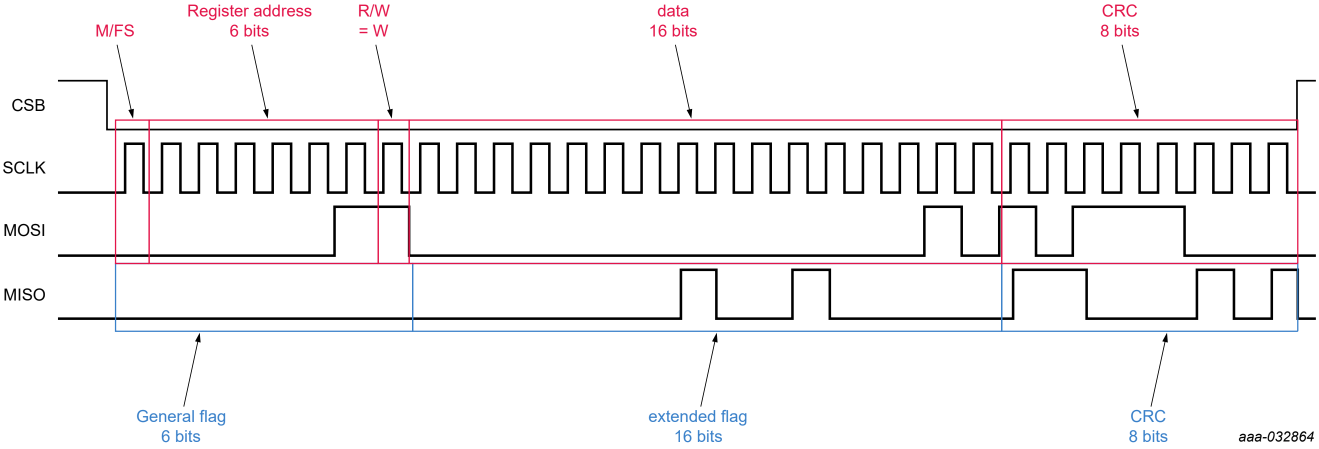


Figure 3. SPI frame with MAIN register M_MODE, address 0x01, write data 0x02

3.4 SPI read frame

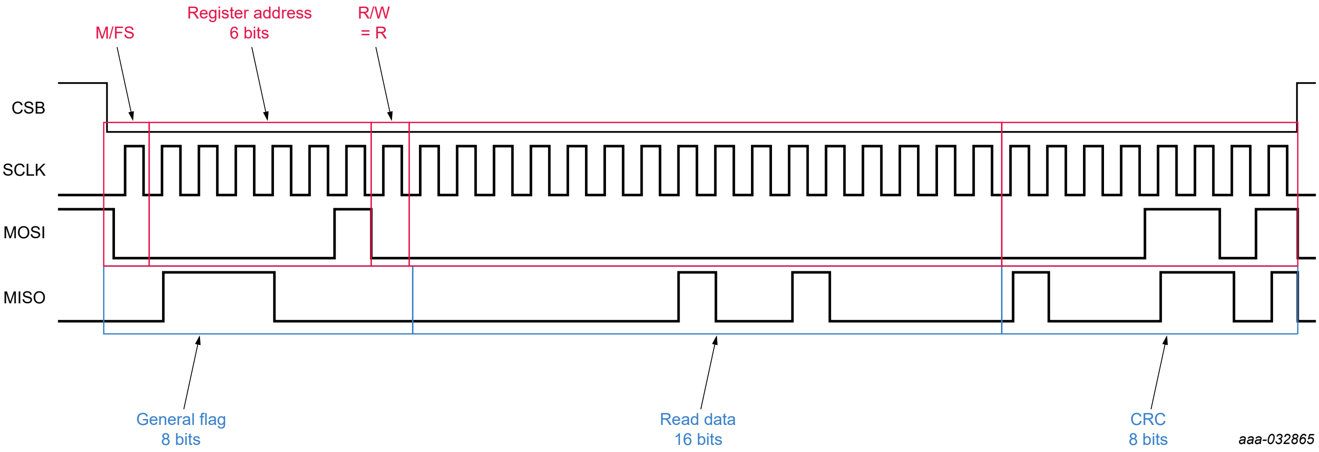


Figure 4. SPI frame with MAIN register M_MODE, address 0x01, read data

3.5 CRC implementation

I^{2}C and SPI communications are protected with an 8-bit CRC. This code example is a possible CRC implementation using a lookup table. Contact your local NXP representative for the complete FS85 demo driver.

```
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 terms found at https://www.nxp.com/LA_OPT_NXP_SW. Only the "internal use
 license" in Section 2.2 in the NXP SOFTWARE LICENSE AGREEMENT is granted for
 this software.static uint8_t FS8x_CalcCRC(const uint8_t* data, uint8_t dataLen)
{
    uint8_t crc;      /* Result. */
    uint8_t tableIdx; /* Index to the CRC table. */
    uint8_t dataIdx;  /* Index to the data array (memory). */

    FS_ASSERT(data != NULL);
    FS_ASSERT(dataLen > 0);
    /* Set CRC seed value. */
    crc = FS8x_COM_CRC_INIT;
    for (dataIdx = dataLen - 1; dataIdx > 0; dataIdx--)
    {
       tableIdx = crc ^ data[dataIdx];
        crc = FS8x_CRC_TABLE[tableIdx];
    }
    return crc;
}
```

4 Debug mode

One time programming (OTP) or OTP emulation is possible only during customer engineering development.

With OTP, the device starts with the configuration at every power up. With OTP emulation, the configuration is lost if the power supply is removed.

4.1 Debug mode entry

The Functional description *Debug mode* section of the product data sheet explains how the FS84/FS85 enters debug mode with the following sequence:

1. DBG pin = V_{DBG} and VSUP > V_{SUP_UVH}
2. WAKE1 or WAKE2 > $WAKE12_{VIH}$

V_{DBG} and VSUP come up at the same time as long as WAKE1 or WAKE2 come up last. There are 2 ways to achieve above sequence, either manually or automatically.

4.2 Manual debug mode entry

Manual debug mode entry is possible with the proposed circuitry in Figure 5.

The user generates the sequence 1-2-3 manually to enter debug mode

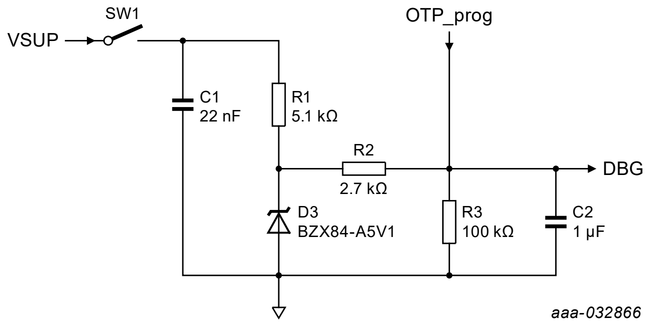


Figure 5. Manual debug mode entry circuitry

1. Close SW1
2. Apply VSUP
3. Apply WAKE1

The device starts and stops the state machines waiting for OTP or OTP emulation thru SPI or I^2C. OTP or OTP emulation can be done only with the FS85/84 Flex graphical user interface (FlexGUI)[12]. OTP requires that OTP_prog = 8 V upon FlexGUI request.

When OTP or OTP emulation is complete, open SW1 to enable the device to start with the power-up sequence in accordance with the OTP configuration.

4.3 Automatic debug mode entry

Automatic debug mode entry is possible with the proposed circuitry in Figure 6 attached to the WAKE1 (or WAKE2) pin. VSUP must be applied first, then WAKE input is applied.

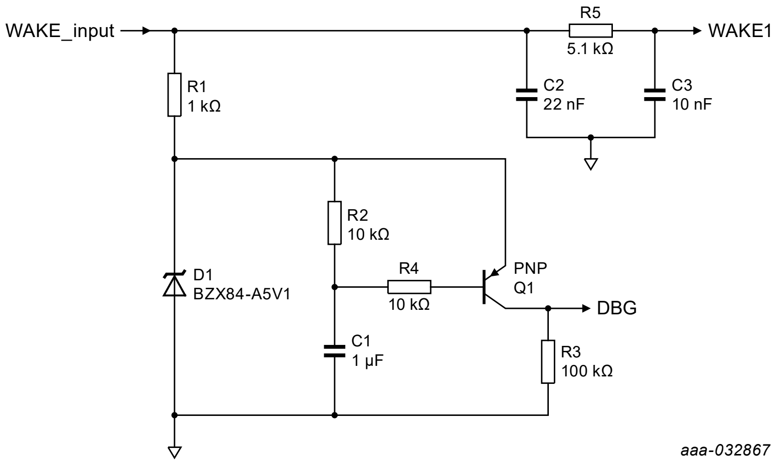


Figure 6. Automatic debug mode entry circuitry

This circuit is proposed for lab evaluation only. The pulse duration is affected by VSUP slew rate and does not work with very slow ramp up. NXP recommends applying VSUP voltage first, then WAKE_input voltage second. If VSUP is also supplying WAKE_input, a switch can be used to apply WAKE_input after VSUP. C1 needs time to discharge thru R2 + R1 between power down and power up cycle to generate a new pulse at DBG pin.

A pulse is automatically generated at the DBG pin to enter debug mode without OTP or OTP emulation but with the debug mode features listed in the Functional description *Debug mode* section of the product data sheet. These features include: watchdog window fully opened; deep fail-safe entry disabled; and 8 s timer monitoring of RSTB pin disabled.

When R1 is populated, the device will automatically start in debug mode. When R1 is not populated, the device will start in normal mode.

To correctly detect the debug mode entry, a recommended pulse with duration greater than 7 ms is required when WAKE1 > $WAKE12_{VIH}$ is generated to have VBOS started and LBIST executed before the end of the pulse. The total pulse duration is estimated as $T_{PULSE} = –RC × \ln(Q1\_V_{BE} / V_{D1})$ with R = R2 // R4, $Q1\_V_{BE}$ = 0.6 V and V_{D1} = 5.1 V.

In the circuitry of Figure 6, the RC value gives an estimated pulse duration of T_{PULSE} ~10.7 ms. The simulation in Figure 7 confirms a total T_{PULSE} ~10 ms, which is above the recommended 7 ms.

The external components values can be adjusted to optimize the pulse duration (longer or shorter) if needed.

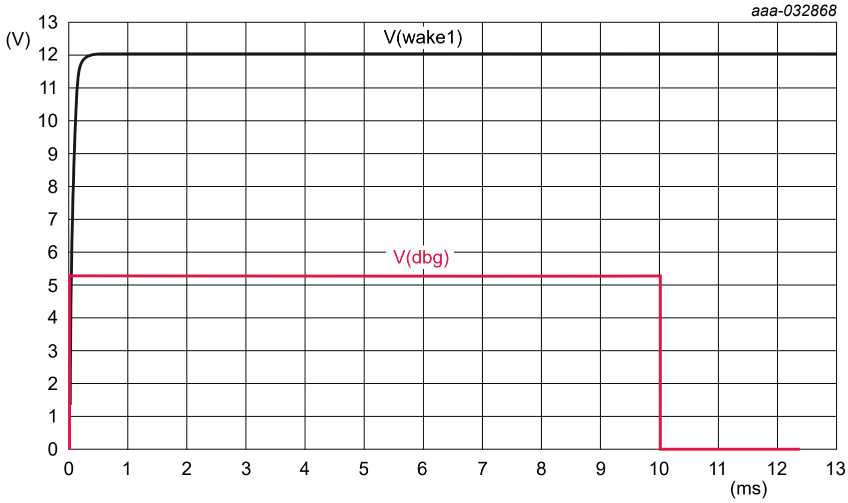


Figure 7. Automatic debug mode entry simulation

5 MCU programming

5.1 Production-level assembly line programming

After PCB assembly, the first time the MCU is powered up, the flash memory of the MCU is empty and needs to be programmed. To facilitate the programming, NXP recommends using the device debug mode applying the correct voltage at the DEBUG pin. Refer to the Functional description *Debug mode* section of the product data sheet. In debug mode, the watchdog timeout is disabled by default, preventing a periodic watchdog refresh.

When the programming is complete:

- If an MCU software reset is required, reset the MCU using a reset request with the RSTB_REQ bit in the FS_SAFE_IOs register in order to execute the new software and leave the debug mode with DBG_EXIT bit in FS_STATES register.
- If an MCU hardware reset is required, send the device to standby with the GOTOSTBY bit in the M_MODE register using WAKE1 or WAKE2 at high level in order to restart the MCU from a power on reset and execute the software.

5.2 In-vehicle programming

For in-vehicle programming, if debug mode cannot be used, the watchdog refresh may be disabled during the INIT_FS state of the fail-safe logic in order to allow programming without considering the watchdog refresh. The INIT_FS can be entered using the GOTO_INITFS bit in the FS_SAFE_IOs register.

NXP recommends disabling FCCU monitoring to avoid unexpected FCCU error detection during programming by setting the FCCU_CFG[1:0] bits at ‘00’ in the FS_I_SAFE_INPUTS register. The watchdog disable takes effect when the INIT_FS is closed and requires at least one good watchdog refresh within the 256 ms of the INIT_FS timeout. Refer to the Functional description *Watchdog* section of the product data sheet for a description of "good watchdog."

When the programming is complete:

- If an MCU software reset is required, reset the MCU using a reset request with the RSTB_REQ bit in the FS_SAFE_IOs register in order to execute the new software and leave the debug mode with DBG_EXIT bit in FS_STATES register.
- If an MCU hardware reset is required, send the device to standby with the GOTOSTBY bit in the M_MODE register using WAKE1 or WAKE2 at high level in order to restart the MCU from a power on reset and execute the software.

6 Application schematic

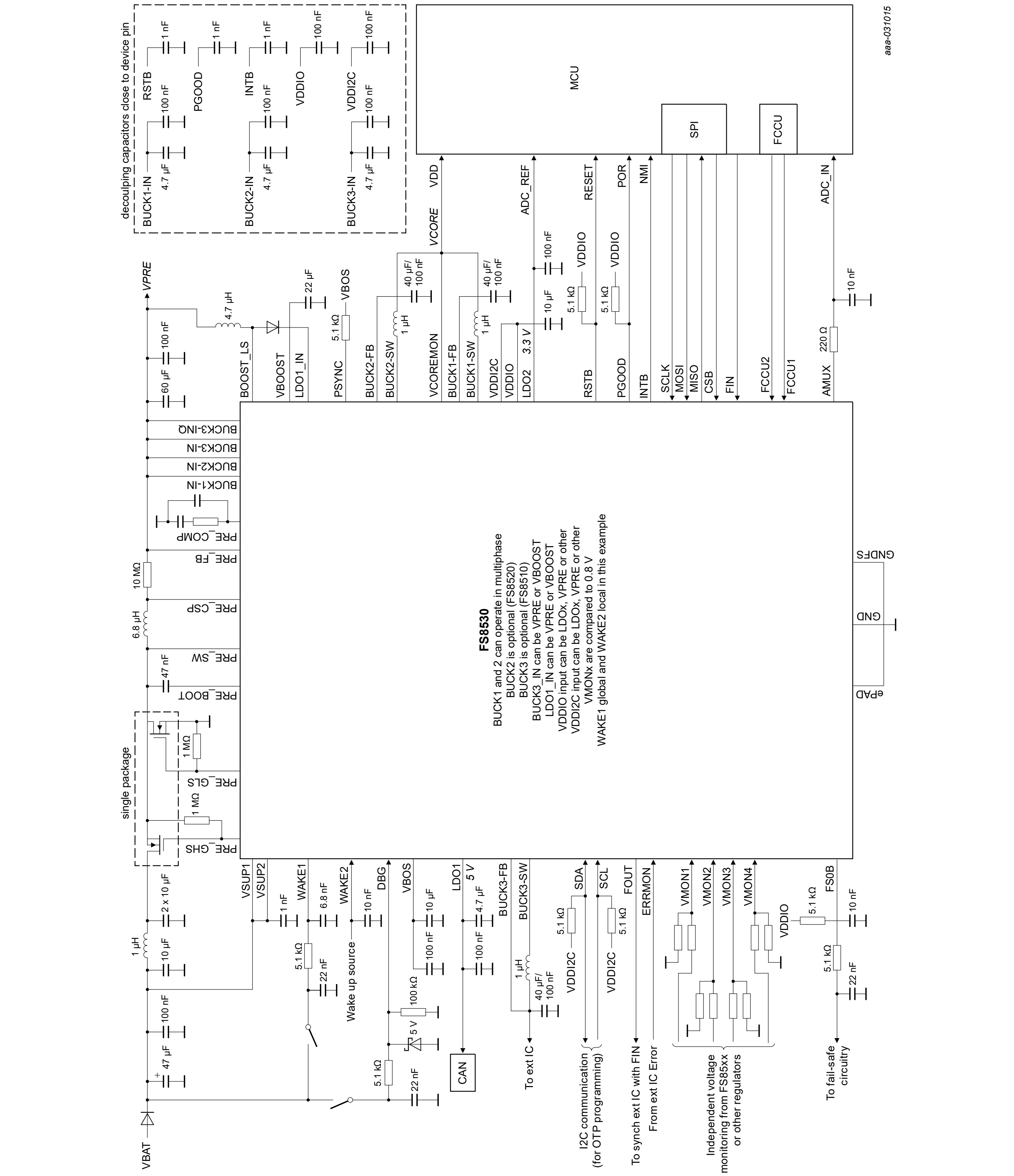


Figure 8. Application schematic - FS8530

6.1 VSUP components

- Reverse battery diode
  - Schottky with Low V_F
  - $I_F > I_{pre}$
  - V_R > 100 V to sustain ISO pulse 1
- Input Ctank capacitor
  - 47 µF or more
  - 50 V rating for 12 V automotive
  - 100 V rating for 24 V truck
- PI filter
  - $F_{RES} = 1 / [2\pi \times \sqrt{(LCpi1)}]$
  - Calculated for Fres < V_{PRE_SW} / 10
  - L = 1 µH
  - Cpi1 = 10 µF
  - 100 nF input decoupling capacitor for conducted emission
- VSUP decoupling capacitor
  - 1 nF decoupling capacitor close to the pin can help the conducted emission
  - 2.2 nF decoupling capacitor before the RBD can help the conducted emission

6.2 VPRE components

- MOSFETs
  - Logical level NMOS, gate drive comes from VBOS (5 V)
  - VDS > 40 V for 12 V automotive applications
  - VDS > 60 V for 24 V truck, bus applications
  - IDS > IPRE_LIM_max
  - At VPRE = 455 kHz:
    - Qg < 15 nC @Vgs = 5 V is recommended
    - At high current (> 6 A), each MOSFETs should be selected in single package to limit the heat exchange between HS and LS. Dual MOSFETs in the same package is OK for low and mid current. (< 6 A)
  - At VPRE = 2.22 MHz:
    - Qg < 7nC @Vgs = 5 V is recommended.
    - Each MOSFETs should be selected in single package to limit the heat exchange between HS and LS.
    - A Schottky diode in parallel to the LS helps to improve the efficiency.
  - Balance the power dissipation between conduction and switching
  - Refer to the *VPRE external MOSFETs* section of the product data sheet for recommended references.
- Inductor
  - Shielded 6.8 µH @ 455 kHz
  - Shielded 2.2 µH @ 2.22 MHz
  - ± 20 % tolerance is preferred but ± 30 % is allowed
  - ISAT > IPRE_LIM
- Output capacitor
  - Ceramic capacitors recommended
  - Typical 66 µF @ 455 kHz. Can be increased depending on load and transient
  - Typical 44 µF @ 2.22 MHz. Can be increased depending on load and transient

- > 3 times VPRE voltage for the DC rating to minimize the DC biasing effect
- Bootstrap capacitor
  - > 10 times the gate source capacitor of Q1, 47 nF used during the validation at NXP
  - 16 V DC rating
- Rshunt
  - Between 10 and 20 mΩ
  - ± 1 % accuracy
  - Inductor DCR current sense can be used at high current to improve the efficiency. See Section 7.
- Compensation network connected at PRE_COMP pin
  - Refer to the *Compensation network and stability* section of the product data sheet to calculate these components.
  - Verify the stability with Simplis model[6]

6.3 VBOOST components

- Diode
  - Schottky with low V_F
  - I_F > IBOOST_LIM
  - V_R > 10 V
- Inductor
  - Shielded 4.7 µH
  - ± 20 % tolerance is preferred but ± 30 % is allowed
  - ISAT > IBOOST_LIM
- Output capacitor
  - Ceramic capacitors recommended
  - Typical 44 µF. Can be increased depending on load and transient
  - > 3 times VBOOST voltage for the DC rating to minimize the DC biasing effect

6.4 LV_BUCK components

- Input capacitor
  - 4.7 µF // 100 nF recommended close to each BUCKx_IN pins
  - > 3 times VPRE voltage for the DC rating to minimize the DC biasing effect
- Inductor
  - Shielded 1 µH
  - ± 20 % tolerance is preferred but ± 30 % is allowed
  - ISAT > IBUCK_LIM
- Output capacitor
  - Ceramic capacitors recommended
  - Minimum 44 µF. Can be adjusted depending on load and transient
  - 100 nF decoupling capacitor can help the conducted emission
  - > 3 times BUCKx voltage for the DC rating to minimize the DC biasing effect

6.5 WAKE components

- WAKE global pin
  - 22 nF input capacitor to damp ESD Gun type of stress
  - 5.1 K to limit the current, minimum 0805 size to avoid arching with high DV / DT like ESD GUN

  - 10 nF decoupling capacitor close to the pin for immunity
- WAKE local pin
  - 6.8 nF decoupling capacitor close to the pin for immunity

6.6 Safety outputs components

- FS0B global pin
  - 22 nF input capacitor to damp ESD gun stress
  - 5.1 K to limit the current, minimum 0805 size to avoid arching with high DV / DT like ESD GUN
  - 10 nF decoupling capacitor close to the pin for immunity
- FS0B, RSTB, PGOOD local pin
  - 1 nF decoupling capacitor close to the pin for immunity

6.7 Automotive schematic used for BOM list

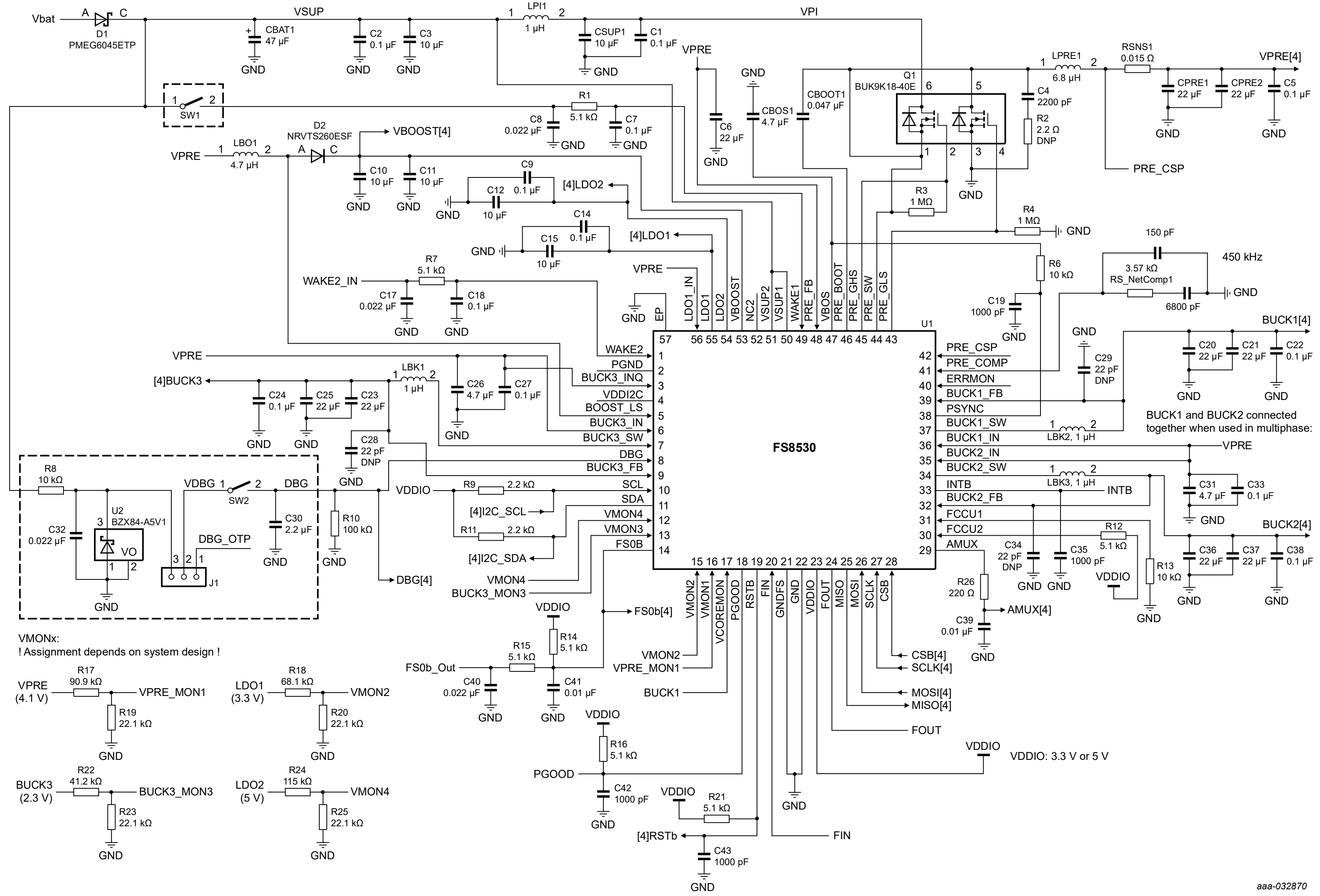


Figure 9. Automotive schematic used for BOM list

6.8 Automotive BOM list

Table 2. Automotive BOM list

Part Reference	Value	Part Manufacturer	Part Number	Description
C1, C2, C5, C7, C9, C14, C18, C22, C24, C27, C33, C38	0.1 µF	TDK	CGA2B3X7R1H104K050BB	CAP CER 0.1 µF 50 V 10 % X7R AEC-Q200 0402
C3, CSUP1	10 µF	Murata	GCM32EC71H106KA03	CAP CER 10 µF 50 V 10 % X7S AEC-Q200 1210
C4	2200 pF	Murata	GCM155R72A222KA37D	CAP CER 2200 pF 100 V 10 % X7R AEC-Q200 0402
C6, C28, C29, C34	22 pF	AVX	04025A220FAT2A	CAP CER 22 pF 50 V 1 % C0G 0402
C8, C17, C40	0.022 µF	Murata	GCM155R71H223KA55D	CAP CER 0.022 µF 50 V 10 % X7R AEC-Q200 0402
C10, C11, C12, C15	10 µF	Murata	GCM21BC71C106ME36	CAP CER 10 µF 16 V 20 % X7S AEC-Q200 0805
C13	150 pF	Murata	GCM1555C1H151JA16D	CAP CER 150 pF 50 V 5 % C0G AEC-Q200 0402
C16	6800 pF	KEMET	C0402C682K5RAC_	CAP CER 6800 pF 50 V 10 % X7R 0402
C19, C35, C42, C43	1000 pF	Murata	GCM155R71H102KA37D	CAP CER 1000 pF 50 V 10 % X7R AEC-Q200 0402
C20, C21, C36, C37	22 µF	Murata	GCM31CR71A226KE02	CAP CER 22 µF 10 V 10 % X7R AEC-Q200 1206
C23, C25, CPRE1, CPRE2	22 µF	Murata	GCM32ER71C226ME19	CAP CER 22 µF 16 V 20 % X7R AEC-Q200 1210
C26, C31	4.7 µF	TDK	CGA4J3X7R1C475K125AB	CAP CER 4.7 µF 16 V 10 % X7R AEC-Q200 0805
C30	2.2 µF	TDK	CGA4J3X7R1C225K125AB	CAP CER 2.2 µF 16 V 10 % X7R AEC-Q200 0805
C32	0.022 µF	TDK	C2012X7R2A223K125AA	CAP CER 0.022 µF 100 V 10 % X7R 0805
C39	0.01 µF	Murata	GCM155R71H103KA55D	CAP CER 0.01 µF 50 V 10 % X7R AEC-Q200 0402
C41	0.01 µF	Murata	GCM155R71E103KA37D	CAP CER 0.01 µF 25 V 10 % X7R AEC-Q200 0402
CBAT1	47 µF	Panasonic	EEE1VA470WAP	CAP ALEL 47 µF 35 V 20% -- AEC-Q200 SMT
CBOOT1	0.047 µF	TDK	CGA2B3X7R1H473K050BB	CAP CER 0.047 µF 50 V 10 % X7R AEC-Q200 0402
CBOS1	4.7 µF	Murata	GCM21BC71A475KA73	CAP CER 4.7 µF 10 V 10 % X7S AEC-Q200 0805
D1	PMEG6045ETP	Nexperia	PMEG6045ETPX	DIODE SCHOTTKY 60 V 4.5 A AEC-Q101 SOD128
D2	NRVTS260ESF	ON Semiconductor	NRVTS260ESFT1G	DIODE PWR SCH RECT 2 A 60 V AEC-Q101 SOD-123FL
LBK1, LBK2, LBK3	1 µH	TDK	TFM252012ALMA1R0MTAA	IND PWR 1.0 µH @ 1 MHz 4.7 A 20 % AEC-Q200 SMD
LBO1	4.7 µH	TDK	TFM252012ALMA4R7MTAA	IND PWR 4.7 µH @ 1 MHz 2.2 A 20 % AEC-Q200 SMD
LPI1	1 µH	TDK	SPM6545VT-1R0M-D	IND PWR 1.0 µH @ 100 kHz 22.9 A 20 % AUTO SMD
LPRE1	6.8 µH	TDK	SPM7054VT-6R8M-D	IND PWR 6.8 µH 10.9 A 20 % AUTO SMD
Q1	BUK9K18-40E	Nexperia	BUK9K18-40E, 115	TRAN NMOS PWR SW DUAL 19.5 mΩ 30 A 40 V AEC-Q101 LFPAK56D
R1, R7, R12, R14, R15, R16, R21	5.1 kΩ	Panasonic	ERA2AEB512X	RES MF 5.1 kΩ 1/16W 0.1% 0402
R2	2.2 Ω	KOA Speer	RK73H1JTTD2R20F	RES MF 2.2 Ω 1/10 W 1 % 0603
R3, R4	1 MΩ	VISHAY	CRCW04021M00FKED	RES MF 1.0 MΩ 1/16 W 1 % AEC-Q200 0402
R5	3.57 kΩ	KOA Speer	RK73H1ETTP3571F	RES MF 3.57 kΩ 1/10 W 1 % AEC-Q200 0402

Table 2. Automotive BOM list *...continued*

Part Reference	Value	Part Manufacturer	Part Number	Description
R6, R8, R13	10 kΩ	Yageo	RC0402FR-1310KL	RES MF 10 kΩ 1/16 W 1 % 0402
R9, R11	2.2 kΩ	Panasonic	ERJ-2RKF2201X	RES MF 2.2 kΩ 1/10 W 1 % AEC-Q200 0402
R10	100 kΩ	Panasonic	ERJ-2RKF1003X	RES MF 100 kΩ 1 % 1/10 W AEC-Q200 0402
R17	90.9 kΩ	KOA Speer	RK73H1ETTP9092F	RES MF 90.9 kΩ 1/10 W 1 % AEC-Q200 0402
R18	68.1 kΩ	KOA Speer	RK73H1ETTP6812F	RES MF 68.1 kΩ 1/16 W 1 % 0402
R19, R20, R23, R25	22.1 kΩ	Panasonic	ERJ-3EKF2212V	RES MF 22.1 kΩ 1/10 W 1 % AEC-Q200 0603
R22	41.2 kΩ	Vishay	CRCW040241K2FKED	RES MF 41.2 kΩ 1/16 W 1 % AEC-Q200 0402
R24	115 kΩ	KOA Speer	RK73H1ETTP1153F	RES MF 115 kΩ 1/10 W 1 % AEC-Q200 0402
RSNS1	0.015 Ω	Vishay	WSLP1206R0150FEA	RES MF 0.015 Ω 1 W 1 % AEC-Q200 1206
U2	BZX84-A5V1	Nexperia	BZX84-A5V1, 215	DIODE ZENER 5.1V 250MW AEC-Q101 SOT23

7 VPRE using inductor DCR current sensing

For high current applications (I_{PRE} > 5 A), the power dissipation in the current sense resistor becomes non-negligible (> 0.25 W). In that case, the DCR current sense technique can be a good alternative, using the intrinsic DCR of the inductor to sense the current. However, the inductor DCR value is less accurate than a shunt resistor which impacts the current limitation. Higher resistance value means lower current limitation and less accuracy means wider current limitation range.

7.1 Low DCR value

When the inductor DCR is low (lower than 15 mΩ as a guideline only), the DCR current sense with a single capacitor C_{LH} is possible. In this case, the current limitation is linked to the inductor DCR value ($I_{LIM\_PRE} = V_{PRE\_LIM\_TH} / R_{DCR}$).

This DCR current sense implementation is visible in Figure 10 using the R_{LL} and C_{LH} components.

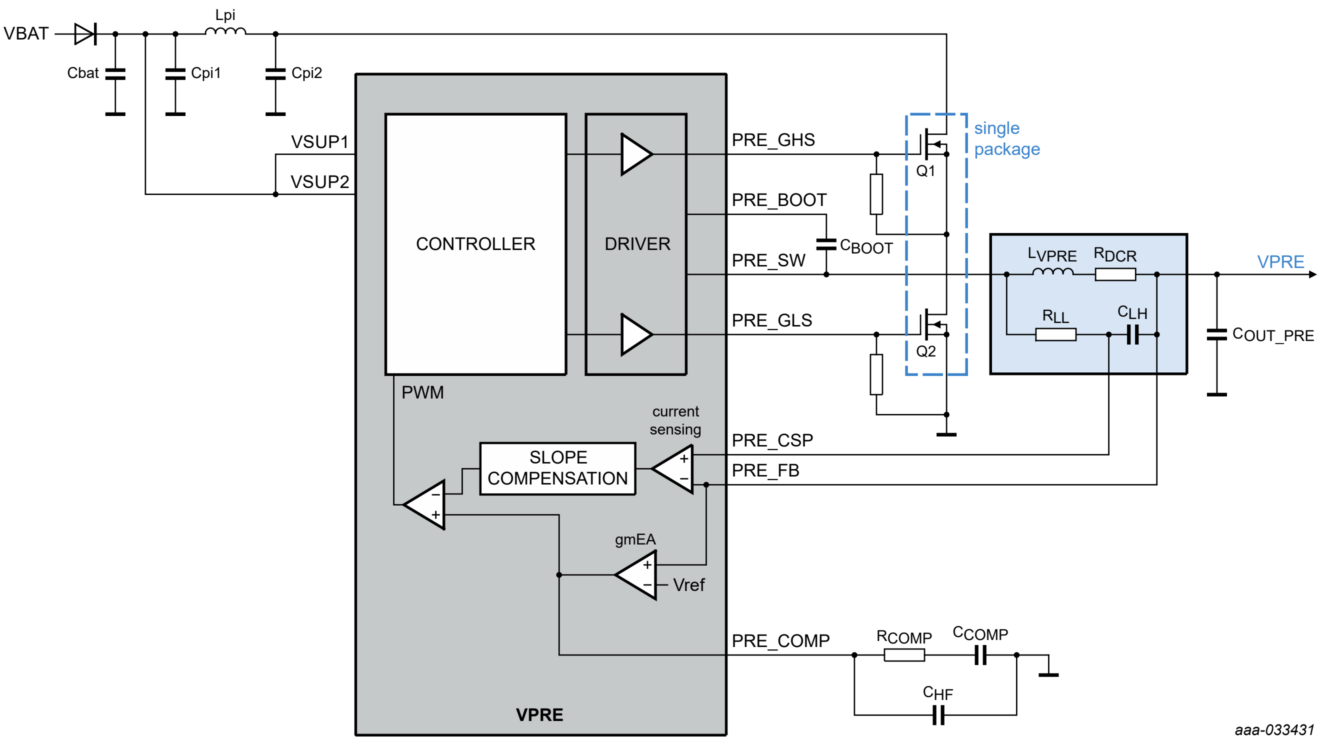


Figure 10. DCR current sense with a single capacitor

7.2 Components calculation

Inductor voltage equation in the Laplace domain:

The initial inductor current $I_{PRE}(0)$ and the initial capacitor voltage $V_{CLH}(0)$ are set to 0.

$$V_{LVPRE}(s) = I_{PRE} * (R_{DCR} + L_{PRE} * s) = V_{RDCR} * (1 + \frac{L_{PRE}}{R_{DCR}} * s)$$

The capacitor voltage $V_{CLH}(s)$ can be written using a voltage divider bridge:

$$V_{CLH}(s) = V_{RDCR} * \frac{\left(1 + \frac{L_{PRE}}{R_{DCR}} * s\right)}{(1 + R_{LL}C_{LH} * s)} = V_{RDCR} * \frac{(1 + \tau_L * s)}{(1 + \tau_c * s)}$$

When R_{LL} and C_{LH} are selected in such a way that the τ_C time constant is equal to the ratio of inductance and its direct current resistor, the capacitor voltage V_{CLH} is directly proportional to the inductor current I_{PRE}.

$$R_{LL}C_{LH} = \frac{L_{PRE}}{R_{DCR}} \quad \leftrightarrow \quad V_{CLH} = R_{DCR} * I_{PRE}$$

If $\tau_L = \tau_C$:

$$R_{DCR\_TARGET} = R_{DCR} \quad \leftrightarrow \quad R_{LL} = \frac{L_{PRE}}{R_{DCR\ TARGET} * C_{LH}}$$

The capacitor C_{LH} value should be selected in the range of several hundred nF to calculate the resistor R_{LL}.

Calculation example for an inductor L_{PRE} = 6.8 µH and R_{DCR} = 10 mΩ:

- R_{LL} = 6.8 kΩ and C_{LH} = 100 nF
- I_{LIM_PRE} = 12 A for $V_{PRE\_LIM\_TH}$ = 120 mV

7.3 Comparative results

V_{SUP} = 14 V, V_{PRE} = 4.1 V, Fsw = 455 kHz

L_{VPRE} = 6.8 µH, R_{DCR} = 10 mΩ, Cout = 66 µF

Rcomp = 3.57 kΩ, Ccomp = 6.8 nF, Chf = 150 pF

Figure 11 shows comparative results between the resistor current sensing with Rshunt = 10 mΩ and the inductor DCR current sensing with R_{DCR} = 10 mΩ, R_{LL} = 6.8 kΩ, C_{LH} = 100 nF

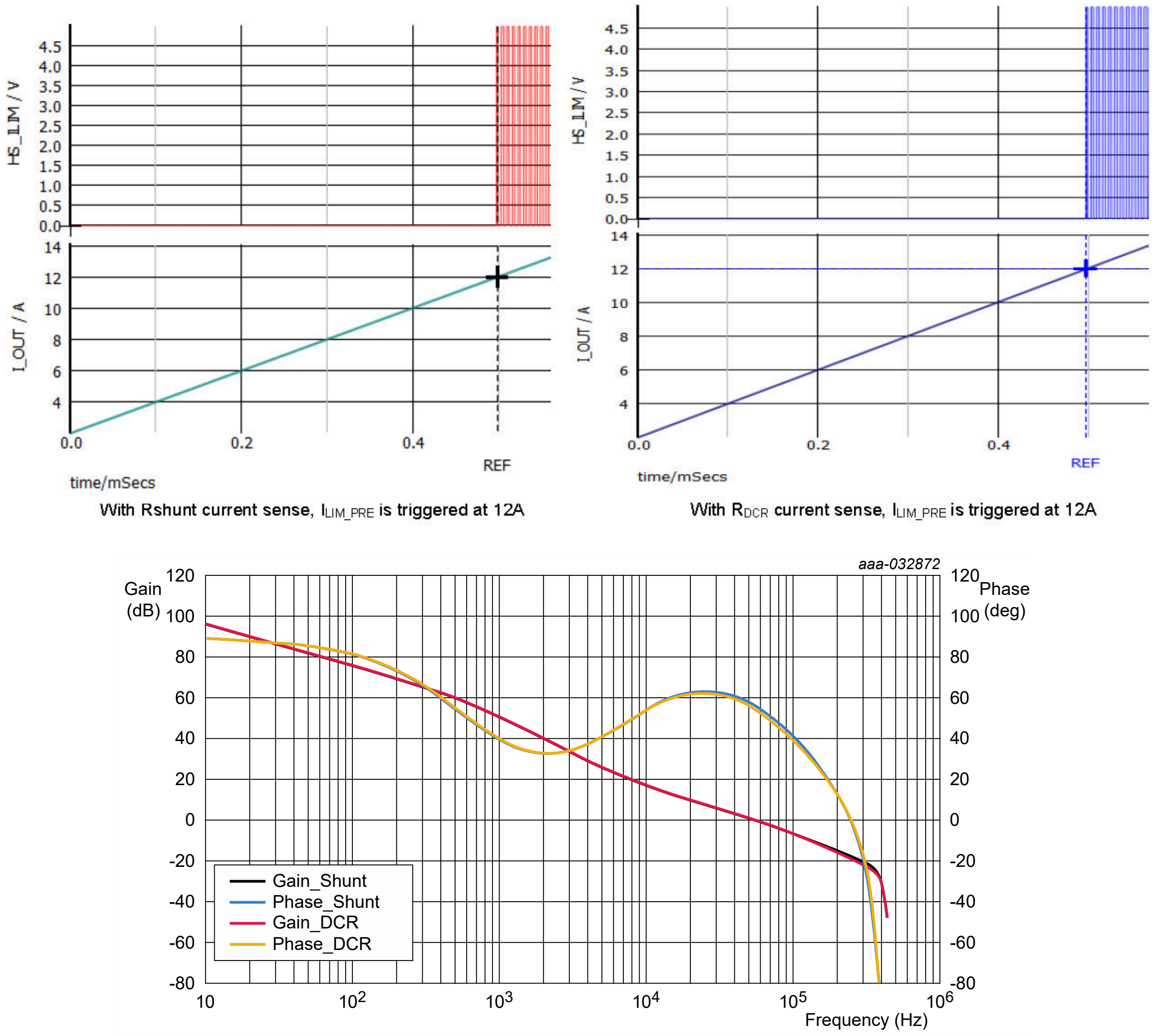


Figure 11. Resistor current sensing with Rshunt = 10 mΩ vs. inductor DCR current sensing with R_{DCR} = 10 mΩ, R_{LL} = 6.8 kΩ, C_{LH} = 100 nF

Current sense	Bandwidth	PM	GM	I_{LIM_PRE}
Rshunt	55 kHz	55 deg	17 dB	12 A
DCR	55 kHz	53 deg	18 dB	12 A

The results obtained with Rshunt current sense or inductor DCR current sense confirms similar performance.

7.4 High DCR value

When the inductor DCR is high (higher than 15 mΩ as a guideline only), the DCR current sense with a resistor divider (R_{LL} + R_{LH}) helps to maintain a high current limitation by feeding a ratio of the current to the differential amplifier.

In that case, the current limitation is linked to the voltage across R_{LH} resistor. The ratio between R_{LL} and R_{LH} to maintain the current limitation is considered in the components calculation.

This DCR current sense implementation is visible in the Figure 12 using R_{LL} + R_{LH} + C_{LH} components.

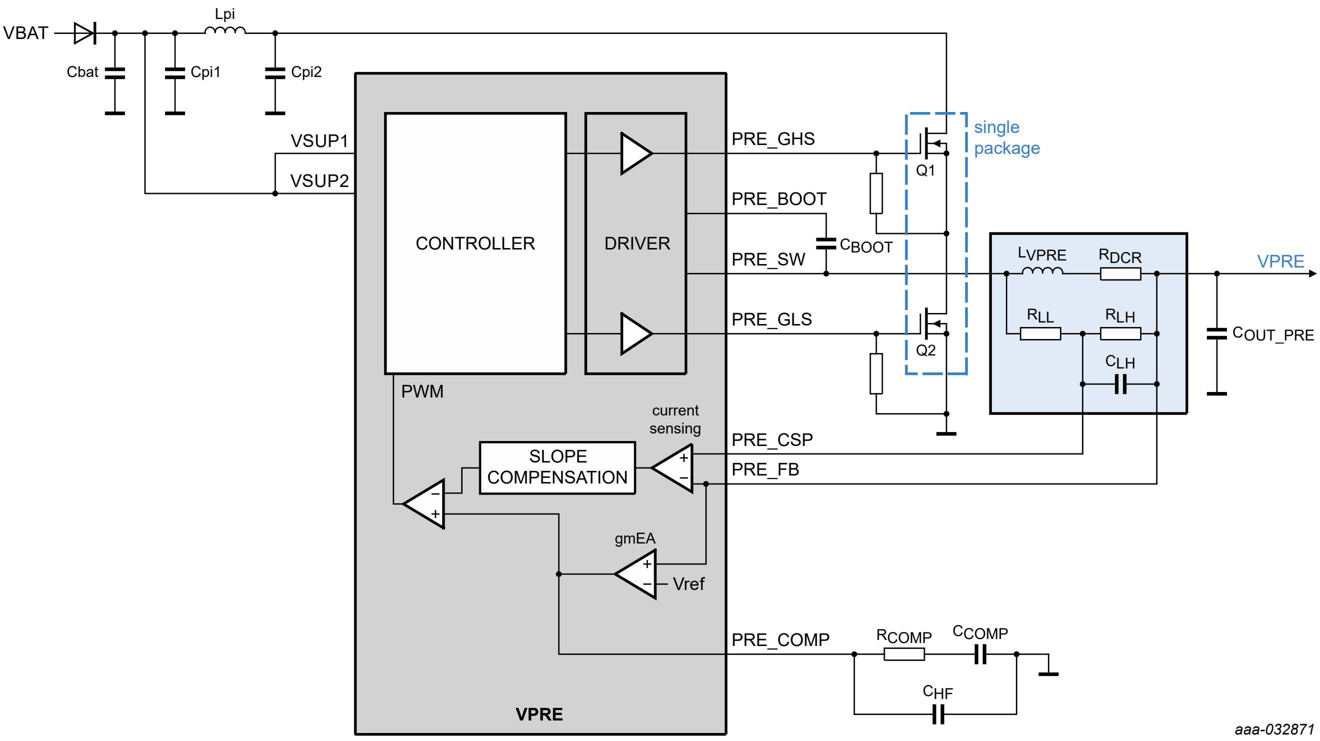


Figure 12. DCR current sense with a capacitor divider

7.5 Components calculation

The inductor voltage equation in the Laplace domain:

The initial inductor current $I_{PRE(0)}$ and the initial capacitor voltage $V_{CLH}(0)$ are set to 0.

$$V_{LPRE}(s) = I_{PRE} * (R_{DCR} + L_{PRE} * s) = V_{RDCR} * (1 + \frac{L_{PRE}}{R_{DCR}} * s)$$

The capacitor voltage $V_{CLH}(s)$ can be written using a voltage divider bridge:

$$V_{CLH}(s) = V_{RDCR} * \frac{R_{LH}}{R_{LL} + R_{LH}} * \frac{\left(1 + \frac{L_{PRE}}{R_{DCR}} * s\right)}{\left(1 + \frac{R_{LL} * R_{LH}}{R_{LL} + R_{LH}} C_{LH} * s\right)} = V_{RDCR} * \frac{R_{LH}}{R_{LL} + R_{LH}} * \frac{(1 + \tau_L * s)}{(1 + \tau_c * s)}$$

When R_{LL}, R_{LH}, and C_{LH} are selected in such a way that the τ_C time constant is equal to the ratio of inductance and its direct current resistor, the capacitor voltage V_{CLH} is directly proportional to the inductor current I_{PRE}.

$$\frac{R_{LL} * R_{LH}}{R_{LL} + R_{LH}} C_{LH} = \frac{L_{PRE}}{R_{DCR}} \quad (1) \quad \leftrightarrow \quad V_{CLH} = R_{DCR} * \frac{R_{LH}}{R_{LL} + R_{LH}} * I_{PRE}$$

If $\tau_L = \tau_C$:

$$R_{DCR\_TARGET} = R_{DCR} * \frac{R_{LH}}{R_{LL} + R_{LH}} \quad (2)$$

R_{LH} and R_{LL} expressions can be derived using equations (1) and (2):

$$R_{LL} = \frac{R_{LL} * L_{PRE} * (R_{DCR} - R_{DCR\_TARGET})}{R_{DCR\ TARGET} * (R_{LL} * R_{DCR} * C_{LH}) - L_{PRE}}$$

$$R_{LL}^2 * R_{DCR_{TARGET}} * R_{DCR} * C_{LH} - (R_{LL} * R_{DCR} * L_{PRE}) = 0$$

Solving this second degree equation gives:

$$R_{LL} = \frac{L_{PRE}}{C_{LH} * R_{DCR\ TARGET}} \quad (3) \qquad OR \qquad R_{LL} = 0 \ (4)$$

Use result (3) to find the R_{LH} resistor value:

$$R_{LH} = \frac{L_{PRE}}{(R_{DCR} - R_{DCR\ TARGET}) * C_{LH}}$$

The capacitor C_{LH} value should be selected in the range of several hundred nF to calculate the resistor R_{LL} and R_{LH}.

Calculation example for an inductor L_{PRE} = 6.8 µH and R_{DCR} = 20 mΩ

- I_{LIM_PRE} = 12 A for $V_{PRE\_LIM\_TH}$ = 120 mV:
- C_{LH} is selected at 100 nF
- R_{LL} and R_{LH} are calculated.

Table 3. Calculation example

Parameter	Value	Unit	Comments
L_{PRE}	6.8	µH	°
R_{DCR_REAL}	0.020	Ω	°
$V_{PRE\_LIM\_TH}$	0.12	V	ILIM (OTP)
I_{PRE_MAX}	12	A	°
R_{DCR_TARGET}	0.010	Ω	$V_{PRE\_LIM\_TH}/I_{PRE\_MAX}$
Ratio	2.0	°	$R_{DCR\_REAL} - R_{DCR\_TARGET}$
C_{LH}	100	nF	Selected
R_{LL}	6.8	kΩ	$L_{PRE}/R_{DCR\_TARGET}/C_{LH}$
R_{LH}	6.8	kΩ	$L_{PRE}/(R_{DCR\_REAL} - R_{DCR\_TARGET})/C_{LH}$
V_{RDCR}	0.3	V	$R_{DCR\_REAL} \times I_{PRE\_MAX}$

7.6 Comparative results

V_{SUP} = 14 V, V_{PRE} = 4.1 V, Fsw = 455 kHz

L_{VPRE} = 6.8 µH, R_{DCR} = 20 mΩ, Cout = 66 µF

Rcomp = 3.57 kΩ, Ccomp = 6.8 nF, Chf = 150 pF

Figure 13 shows comparative results between the resistor current sensing with Rshunt = 10 mΩ and the inductor DCR current sensing with R_{LL} = 6.8 kΩ, R_{LH} = 6.8KΩ, C_{LH} = 100 nF

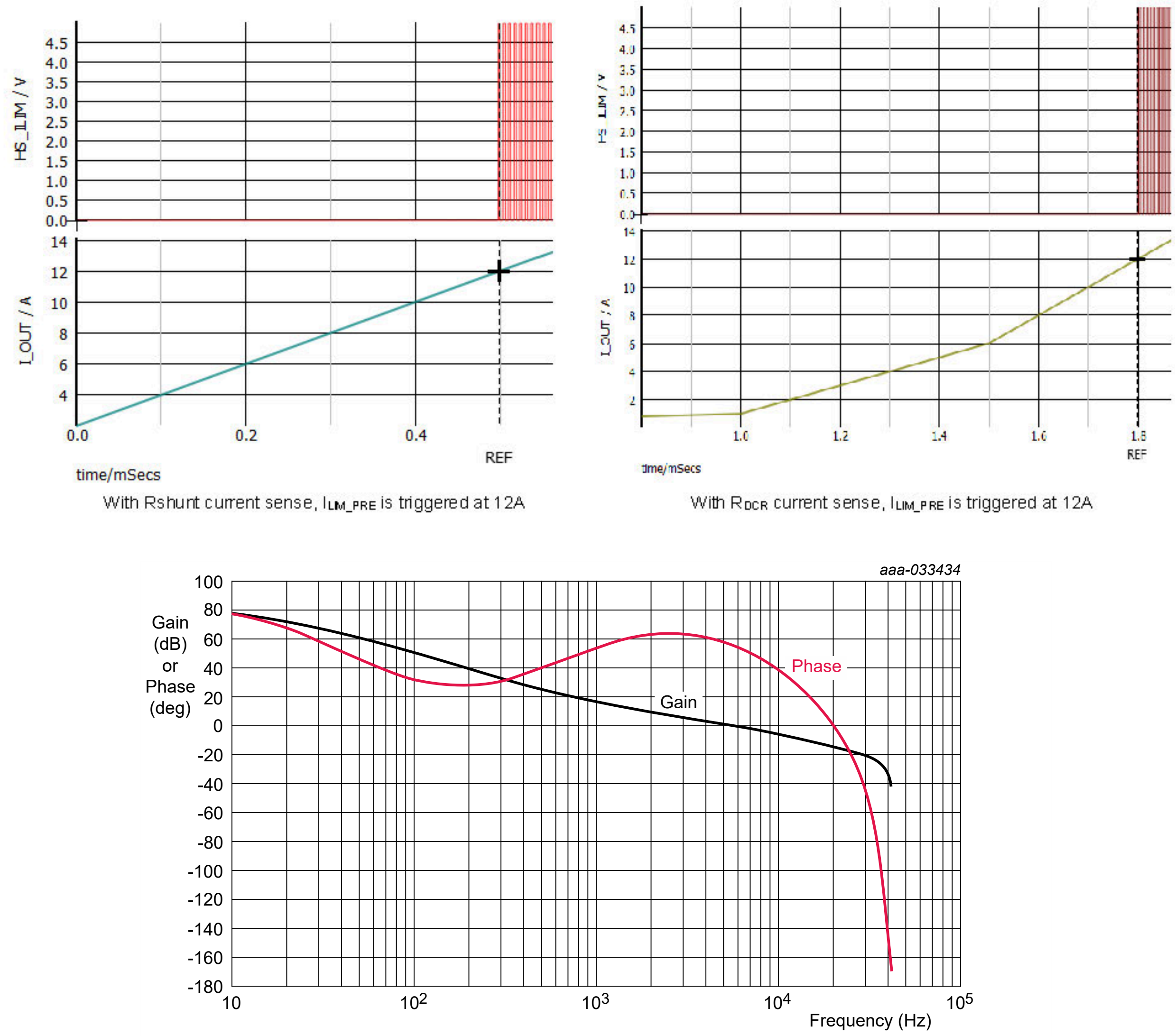


Figure 13. Resistor current sensing with Rshunt = 10 mΩ vs. inductor DCR current sensing with R_{LL} = 6.8 kΩ, R_{LH} = 6.8KΩ, C_{LH} = 100 nF

Current sense	Bandwidth	PM	GM	I_{LIM_PRE}
Rshunt	58 kHz	55 deg	14 dB	12 A
DCR	58 kHz	55 deg	14 dB	12 A

The results obtained with Rshunt current sense or inductor DCR current sense confirms similar performance.

7.7 Impedance and current limit frequency analysis

This section provides information on deriving the frequency analysis from the Laplace transform using s = jw.

Following assumptions are made before the analysis:

- The switching period T_{switch} is way lower than the two-time constants τ_C and τ_L.
- The two time constants are equal ($\tau_C = \tau_L$)

7.7.1 Frequency analysis without RLH

The capacitor impedance module equation is provided below:

$$|ZC_{LH}(jw)| = \frac{|V_{CLH}(jw)|}{|I_{PRE}(jw)|} = R_{DCR} * \frac{\sqrt{\left(\left(\frac{L_{PRE} * w}{R_{DCR}}\right)^2 + 1\right)}}{\sqrt{\left((R_{LL}C_{LH} * w)^2 + 1\right)}}$$

Table 4. Impedance and current limit frequency analysis without RLH

	w → 0	w → ∞
$\|ZC_{LH}(jw)\|$	R_{DCR}	$\frac{L_{PRE}}{R_{LL} * C_{LH}}$
$\|ZC_{LH}(jw)\|$	$\frac{V_{PRELIM\ TH}}{R_{DCR}}$	$\frac{V_{PRELIM\ TH} * R_{LL} * C_{LH}}{L_{PRE}}$

If $\tau_L = \tau_C$, then:

$$\begin{cases} |ZC_{LH}(jw)|_{w\to 0} = |ZC_{LH}(jw)|_{w\to\infty} \\ \left|I_{PRE\ MAX}(jw)\right|_{w\to 0} = \left|I_{PRE\ MAX}(jw)\right|_{w\to\infty} \end{cases}$$

The capacitor impedance and the current limit maximum are constant with frequency.

7.7.2 Frequency analysis with RLH

The capacitor impedance module equation is provided below:

$$|ZC_{LH}(jw)| = \frac{|V_{CLH}(jw)|}{|I_{PRE}(jw)|} = R_{DCR} * \frac{R_{LH}}{R_{LL} + R_{LH}} * \frac{\sqrt{\left(\left(\frac{L_{PRE} * w}{R_{DCR}}\right)^2 + 1\right)}}{\sqrt{\left(\left(\frac{R_{LL} * R_{LH}}{R_{LL} + R_{LH}} C_{LH} * w\right)^2 + 1\right)}}$$

Table 5. Impedance and current limit frequency analysis with RLH

	w → 0	**w → ∞**
$\lvert ZC_{LH}(jw)\rvert$	$R_{DCR} * \frac{R_{LH}}{R_{LL} + R_{LH}}$	$\frac{L_{PRE}}{R_{LL} * C_{LH}} * \frac{R_{LH}}{R_{LL} + R_{LH}}$
$\lvert I_{PRE\,MAX}(jw)\rvert$	$\frac{V_{PRELIM\,TH}}{R_{DCR} * \frac{R_{LH}}{R_{LL} + R_{LH}}}$	$\frac{V_{PRELIM\,TH} * R_{LL} * C_{LH}}{L_{PRE} * \frac{R_{LH}}{R_{LL} + R_{LH}}}$

If $\tau_L = \tau_C$, then:

$$\begin{cases} |ZC_{LH}(jw)|_{w \to 0} = |ZC_{LH}(jw)|_{w \to \infty} \\ \left|I_{PRE\,MAX}(jw)\right|_{w \to 0} = \left|I_{PRE\,MAX}(jw)\right|_{w \to \infty} \end{cases}$$

The capacitor impedance and the current limit maximum are constant with frequency.

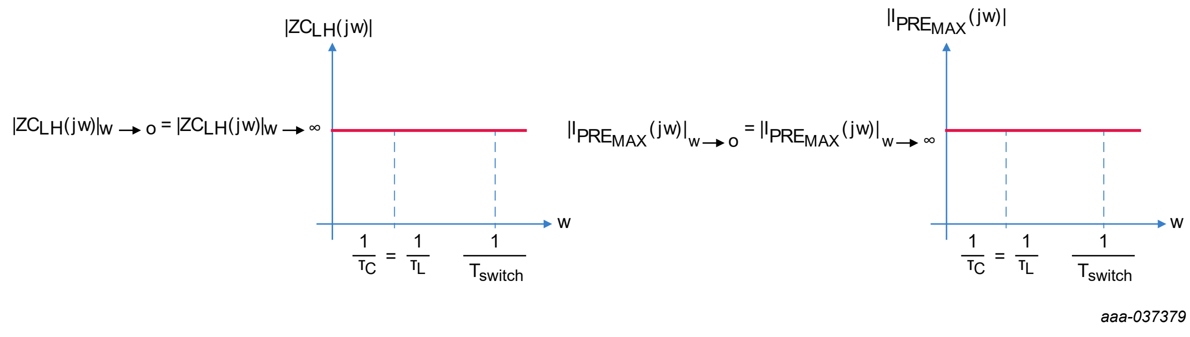


Figure 14. Frequency variation of the capacitor impedance and the current limit max for both cases

7.8 Components calculation summary

The equations of both DCR current sense methods are summarized in the following table:

Table 6. DCR current sense equations

Parameter	R_{LH} not populated		R_{LH} populated	
$V_{CLH}(s)$	$V_{CLH}(s) = V_{RDCR} * \frac{\left(1+\frac{L_{PRE}}{R_{DCR}} * s\right)}{(1+R_{LL}C_{LH} * s)}$		$V_{CLH}(s) = V_{RDCR} * \frac{R_{LH}}{R_{LL}+R_{LH}} * \frac{\left(1+\frac{L_{PRE}}{R_{DCR}} * s\right)}{\left(1+\frac{R_{LL} * R_{LH}}{R_{LL}+R_{LH}}C_{LH} * s\right)}$	
Time constants	τ_L	τ_C	τ_L	τ_C
	$\frac{L_{PRE}}{R_{DCR}}$	$R_{LL}C_{LH}$	$\frac{L_{PRE}}{R_{DCR}}$	$\frac{R_{LL} * R_{LH}}{R_{LL}+R_{LH}}C_{LH}$
V_{CLH} at $\tau_L = \tau_C$	$V_{CLH} = V_{RDCR}$		$V_{CLH} = V_{RDCR} * \frac{R_{LH}}{R_{LL}+R_{LH}}$	
I_{PRE_MAX}	$\frac{V_{PRELIM\ TH}}{R_{DCR}}$		$\frac{V_{PRELIM\ TH}}{R_{DCR} * \frac{R_{LH}}{R_{LL}+R_{LH}}}$	
V_{PRESC}	$V_{PRESC} > \frac{V_{PRE}}{L_{PRE}} * R_{DCR} * Acs$		$V_{PRESC} > \frac{V_{PRE}}{L_{PRE}} * R_{DCR} * \frac{R_{LH}}{R_{LL}+R_{LH}} * Acs$	
Equations	$R_{DCR\ TARGET} = R_{DCR}$		$R_{DCR\_TARGET} = R_{DCR} * \frac{R_{LH}}{R_{LL}+R_{LH}}$	
	$R_{LL}C_{LH} = \frac{L_{PRE}}{R_{DCR}}$		$\frac{R_{LL} * R_{LH}}{R_{LL}+R_{LH}}C_{LH} = \frac{L_{PRE}}{R_{DCR}}$	
R_{LL}	$R_{LL} = \frac{L_{PRE}}{R_{DCR\ TARGET} * C_{LH}}$		$R_{LL} = \frac{L_{PRE}}{R_{DCR\ TARGET} * C_{LH}}$	
R_{LH}	n/a		$R_{LH} = \frac{L_{PRE}}{(R_{DCR} - R_{DCR\ TARGET}) * C_{LH}}$	

8 How to use FS84 without BUCK1

In case the FS84 does not supply the MCU core or in case the MCU core requires only 3.3 V or 5 V, BUCK1 may not be required. Since BUCK1 cannot be disabled by OTP, follow this procedure to use FS84 without BUCK1:

1. BUCK1_IN connected to VPRE to keep VPRE_FB_OV protection otherwise BUCK1_IN can be left open
2. BUCK1_SW and BUCK1_FB pins open
3. BUCK1 in power up slot 7 by OTP to not start automatically
4. VCOREMON pin open
5. VCOREMON not assigned to PGOOD and ABIST1
6. Permanent VCOREMON_UV will be reported. To be discarded since BUCK1 is not used.
7. Configure VCOREMON_UV_FS_IMPACT[1:0] = VCOREMON_OV_FS_IMPACT[1:0] = 00 during INIT_FS for no effect on RSTB and FS0B by VCOREMON and to allow FS0B release

9 MCU with CORE_SENSE connection

Some high power MCUs have a sense connection for the CORE supply in order to regulate the CORE voltage at the MCU silicon, instead of through the input pin of the package. See Figure 15 for the recommended connection.

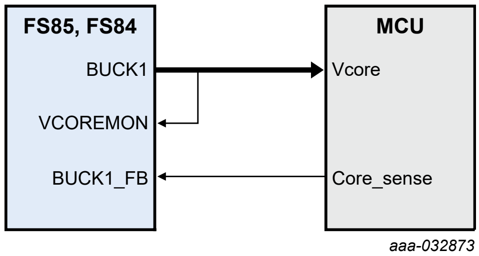


Figure 15. Recommended connection to regulate CORE voltage at MCU silicon

10 PGOOD and RSTB connections

10.1 FS84/FS85 connection to MCU

- FS84/FS85 PGOOD output connected to MCU PORB input for hardware reset
- PGOOD assertion is configured by OTP
- FS84/FS85 bidirectional RSTB connected to MCU reset input for functional reset
- RSTB assertion is configured by SPI/I²C during INIT_FS

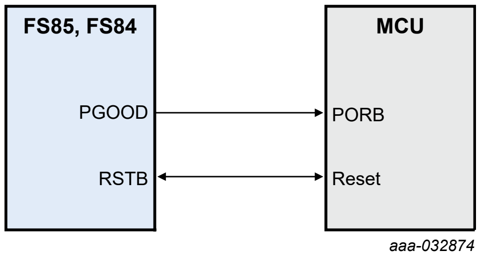


Figure 16. FS85/84 connection to MCU

10.2 ASIL D capable connection with external PMIC

- PMIC is enabled when last FS85 VREGx regulator is started with to respect MCU power sequence (High Voltage first down to Low Voltage)
- For power down sequence, the MCU sends SPI/I²C command to FS85 then VREGx and VCORE will be shut down at the same time.

- FS85_VMONx is used as redundant monitoring to fit for ASIL D capability with OV set for maximum VCORE and UV set for minimum VCORE.
- FS85_VMONx is taken at PMIC regulator output
- FS85_VMONx is assigned to ABIST1 to release FS85_PGOOD after VCORE is available

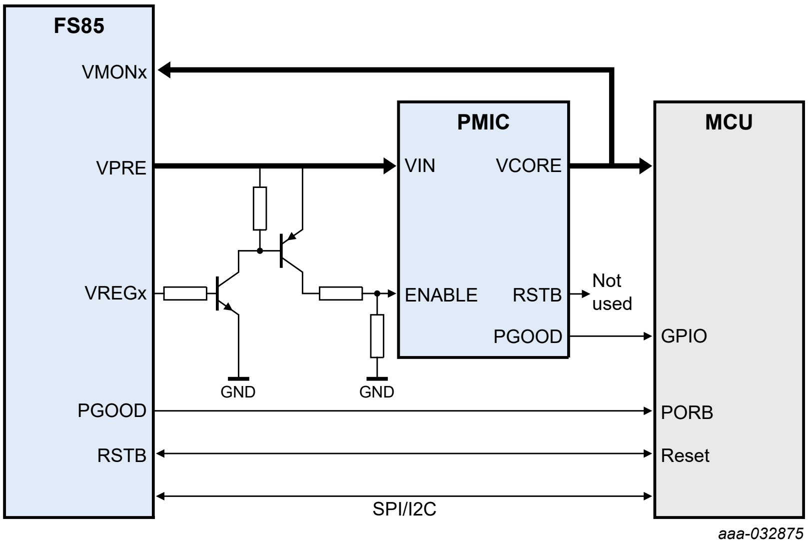


Figure 17. ASIL D connection with external PMIC to MCU

10.3 ASIL B capable connection with external PMIC

- PMIC manages MCU_PGOOD and FS84 manages MCU_Reset
- PMIC is enabled by FS84_PGOOD with respect to the MCU power sequence (high voltage first down to low voltage)
- For power down sequence, MCU send SPI/I^{2}C command to FS84 and VCORE will be shut down when first SBC regulator assert PGOOD
- FS84_RSTB released before MCU_PORB
- When FS84_PGOOD is asserted, PMIC is disabled.

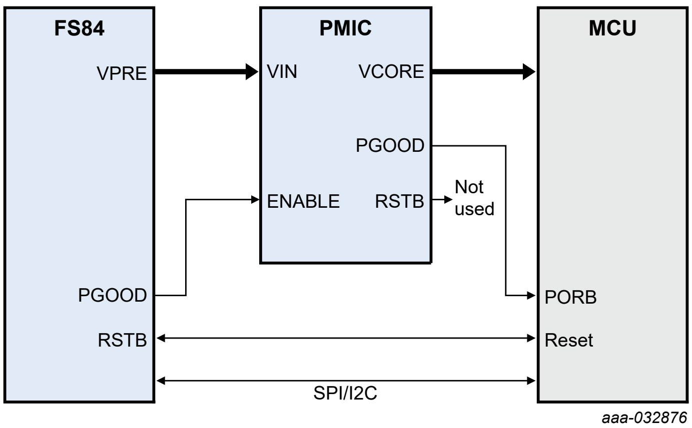


Figure 18. ASIL B connection with external PMIC to MCU

11 External clock synchronization

As stated in Section 25.5 "External clock synchronization" of the FS84/FS85 datasheet, when an external clock synchronization is used, the external clock must be applied on pin FIN before setting the bit EXT_FIN_SEL. The external clock must be active as long as EXT_FIN_SEL is set.

The MCU shall regularly check the state of the CLK_FIN_DIV_OK bit to identify an external clock failure. If CLK_FIN_DIV_OK = 0, then the MCU must read the PLL_LOCK_RT bit to verify if the fault condition is persistent or not. If PLL_LOCK_RT = 1, the fault condition can be considered as a transient condition and the system is ready to switch over to the external clock by setting EXT_FIN_SEL bit again. If PLL_LOCK_RT = 0, the fault is considered as a permanent fault and the MCU must take action to send the system to safe operation.

It is the responsibility of the system designer to define the tolerance time with the external frequency lost before taking an action, such as stopping the system or placing the system in safe state.

12 FS_OSC_DRIFT bit

The FS84/FS85 features two oscillators: one in the main domain and one in the fail-safe domain. If one of the oscillators is drifting too much compared to the other one, the bit FS_OSC_DRIFT is set in the FS_OVUVREG_STATUS register.

This bit is set to 0 at startup in normal cases. In case the device is woken up by a slow ramp (slower than 0.25 V/ms) on the WAKE1/2 pin and V_{SUP} is already over V_{SUP_uvh}, the flag FS_OSC_DRIFT is set in FS_OVUVREG_STATUS during the INIT_FS phase.

To check if a real drift issue has occured, it is recommend to clear the bit in the INIT_FS phase by writing a 1 and reading it back again. If the bit is still set, it means there is an oscillator drift issue. Otherwise, this is linked to slow ramp on the wake pin.

13 ISO pulses

13.1 ISO-pulse description

For a description and images of test pulses, see Table 7.

Table 7. Pulse reference documents

Pulse	Reference documents[1]
Figure 5 — Test pulse 1, page 12. Figure 6 — Test pulse 2a, page 13 Figure 8 — Test pulse 3a, page 15 Figure 9 — Test pulse 3b, page 16	ISO 7637-2:2011(E)[18]
Figure 11: Cold start test pulse, page 29. 4a, 4b (former cranking pulses)	VW 80000: 2009-10[24]
Figure 9 — Test with centralized load dump suppression, (Test pulse 5b), page 12	ISO 16750-2:2012[20]
Figure 9 — Test with centralized load dump suppression, (Test pulse 5b1), page 13	ISO 16750-2:2010(E)[19]

[1] See Section 19 for a list of documents referenced in this application note.

13.1.1 12 V automotive system

- **Pulse 1:** Ua = 14 V, Us = –150 V, Ri = 10 Ω, Td = 2 ms, Tr = 1 µs, T 1 = 0.5 s, T2 = 200 ms, T3 < 100 µs, 500 pulses
- **Pulse 2a:** Ua = 14 V, Us = 112 V, Ri = 2 Ω, Td = 50 µs, Tr = 1 µs, T1 = 0.2 s, 500 pulses
- **Pulse 3a:** Ua = 14 V, Us = –220 V, Ri = 50 Ω, Td = 150 ns, Tr = 5 ns, T1 = 100 µs, T4 = 10 ms, T5 = 90 ms, 1 Hr
- **Pulse 3b:** Ua = 14 V, Us = 150 V, Ri = 50 Ω, Td = 150 ns, Tr = 5 ns, T1 = 100 µs, T4 = 10 ms, T5 = 90 ms, 1 Hr
- **Pulse 4a:** Ub = 11V, Ut = Us = 4.5V, Ua = 6.5V, Ur = 2V, Tf = 1ms, T4 = T5 = 0, T6 = 19ms, T7 = 50ms, T8 = 10s, Tr = 100 ms, F = 2Hz, 10 cycles at interval 2 s
- **Pulse 4b:** Ub = 11V, Ut = 3.2V, Us = 5.0 V, Ua = 6.0 V, Ur = 2 V, Tf = 1 ms, T4 = 19 ms, T5 = 1 ms, T6 = 329 ms, T7 = 50 ms, T8 = 10 s, Tr = 100 ms, F = 2Hz, 10 cycles at interval 2 s
- **Pulse 5b:** Ua = 14V, Us = 35 V, Ri = 1 Ω, Td = 400 ms, Tr = 5 ms, 10 pulses at interval of 1 min

13.1.2 24 V truck system

- **Pulse 1:** Ua = 28 V, Us = –600 V, Ri = 50 Ω, Td = 1 ms, Tr = 3 µs, T1 = 0.5s, T2 = 200 ms, T3 < 100 µs, 500 pulses
- **Pulse 2a:** Ua = 28 V, Us = 112 V, Ri = 2 Ω, Td = 50 µs, Tr = 1 µs, T1 = 0.2 s, 500 pulses
- **Pulse 3a:** Ua = 28 V, Us = –300 V, Ri = 50 Ω, Td = 150 ns, Tr = 5 ns, T1 = 100 µs, T4 = 10 ms, T5 = 90 ms, 1 Hr
- **Pulse 3b:** Ua = 28 V, Us = 300 V, Ri = 50 Ω, Td = 150 ns, Tr = 5 ns, T1 = 100 µs, T4 = 10 ms, T5 = 90 ms, 1 Hr
- **Pulse 5b:** Ua = 28 V, Us = 58 V, Ri = 2 Ω, Td = 350 ms, Tr = 5 ms, 10 pulses at interval of 1 min
- **Pulse 5b1:** Ua = 28 V, Us = 65 V, Ri = 2 Ω, Td = 350 ms, Tr = 5 ms, 10 pulses at interval of 1 min

13.2 Product setup and failing criteria for ISO pulses

All the ISO test pulses are applied to VBAT, at 25 °C, with all regulators loaded according to Table 8.

Table 8. Regulators setting

Output	Vout (V)	Iout (A)
VPRE	4.1	3.3
Buck1	1.25	1.25
Buck2	1.8	1.2
Buck3	2.3	1
Boost	5.74	Loaded by LDO
LDO1	1.8	0.1
LDO2	3.3	0.1

Class A: FS0B remains released during the stress

Class C: FS0B and RSTB are asserted during the stress but released after the stress

13.3 ISO pulse results

Table 9. ISO pulse results

System Voltage	Pulse	Duration	Result
12 V	Pulse 1	500 pulses	**Class C**[1]
24 V	Pulse 1	500 pulses	**Class A**
12 V	Pulse 2a	500 pulses	**Class A**
24 V	Pulse 2a	500 pulses	**Class A**
12 V	Pulse 3a	1 hour	**Class A**
24 V	Pulse 3a	1 hour	**Class A**
12 V	Pulse 3b	1 hour	**Class A**
24 V	Pulse 3b	1 hour	**Class A**
12 V	Pulse 5b	10 pulses	**Class A**
24 V	Pulse 5b	10 pulses	**Class A**
24 V	Pulse 5b1	10 pulses	**Class A**[2]
12 V	LV 124[24] E-11 (4a)	1 pulses	**Class A**
12 V	LV 124[24] E-11 (4b)	1 pulses	**Class A**

[1] Negative pulse 1 generates a device reset after each pulse, inducing RSTB and FS0B assertion. Re-initialization needed to release again FS0B.
[2] External TVS protection required in front of VSUP1/2 pins. MMSZ56T1G TVS reference was used in combination with VPRE MOSFET SQJB80EP-T1 (80 V capable).

14 Non-ISO pulses

14.1 Non-ISO pulse description

For a description and images of test pulses described and documented in various ISO documents, see Table 10.

Table 10. Pulse reference documents

Pulse	Reference documents[1]
Figure 6: Test pulse E-07 Slow decrease and increase of the supply voltage, page 20	VW 80000: 2009-10[24]
Figure 7: Test pulse E-08 Slow decrease, quick increase of the supply voltage, page 22	VW 80000: 2009-10[24]
Figure 9: Test pulses E-10 Short interruptions, page 27	VW 80000: 2009-10[24]

[1] See Section 19 for a list of documents referenced in this application note.

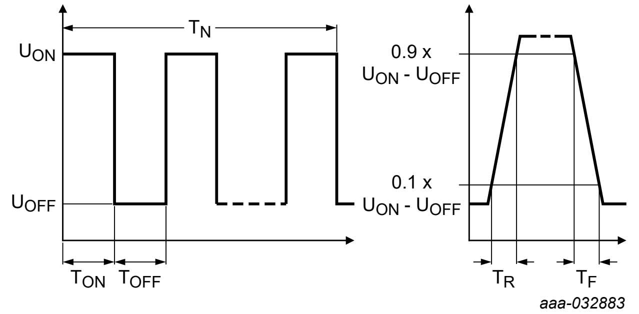


Figure 19. Battery voltage dropout

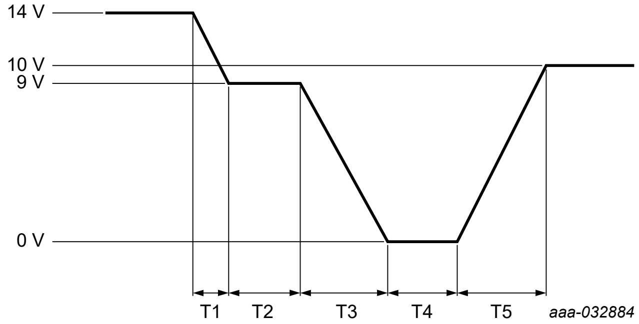


Figure 20. Battery brownout/recovery

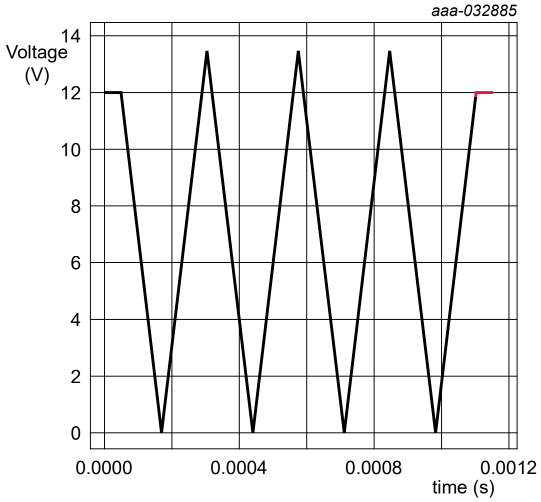


Figure 21. Triangular pulse 1

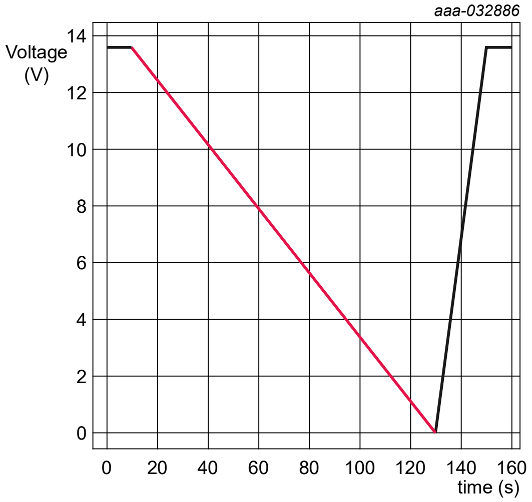


Figure 22. Triangular pulse 2

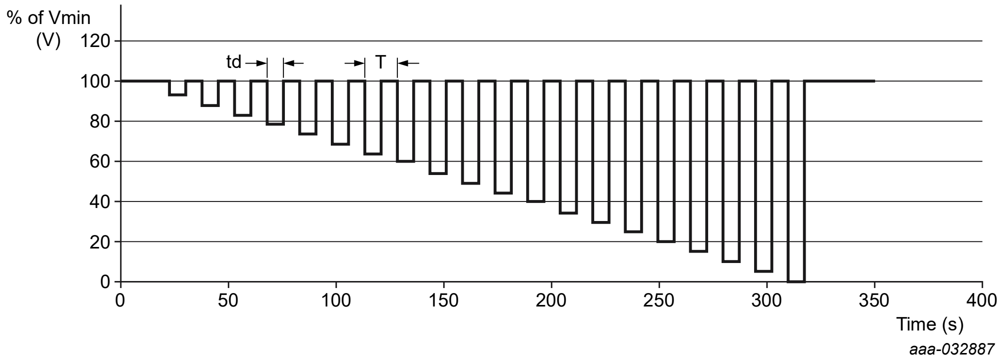


Figure 23. Re-init pulse

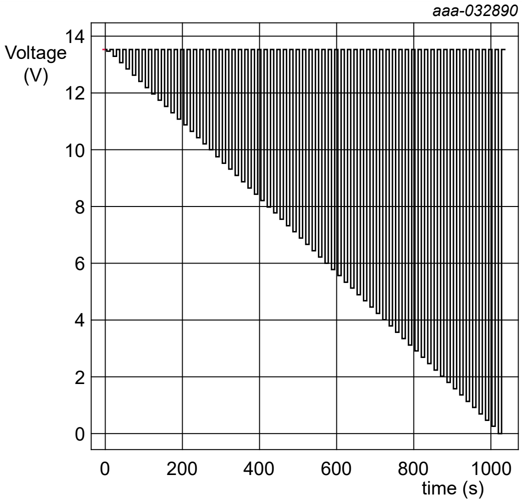


Figure 24. LV124[24] E-09

14.2 Product setup and failing criteria for non-ISO pulses

All the non ISO test pulses are applied at VBAT. They are executed in temperature (at Ta = – 40 °C, Ta = + 25 °C and Ta = + 125 °C), with VPRE at 455 kHz and 2.2 MHz, without load and with loads according to Table 11.

Table 11. Regulators setting

Output	Vout (V)	Iout (A)
VPRE	4.1	3.3
Buck1	1.25	1.25
Buck2	1.8	1.2
Buck3	2.3	1
Boost	5.74	Loaded by LDO
LDO1	1.8	0.1
LDO2	3.3	0.1

Class A: FS0B remains released during the stress

Class C: FS0B and RSTB are asserted during the stress but released after the stress

14.3 Non-ISO pulse results

Table 12. Non-ISO pulse results

Pulse type	Pulse description	No. of pulses	Results
Truck jump start	VBAT = 48 V during 15 min	1	Class A
Battery Voltage Dropout VBAT = UON = 13.5 V, UOFF = 0 V, tr/tf ≤ 1 µs, Ri = 0.01 Ω	t_{ON} = 0.9 ms, t_{OFF} = 0.1 ms	4000	Class A
	t_{ON} = 9 ms, t_{OFF} = 1 ms	10	Class C
	t_{ON} = 9 ms, t_{OFF} = 6 ms	10	Class C
	t_{ON} = 200 ms, t_{OFF} = 10 ms	10	Class C
	t_{ON} = 200 ms, t_{OFF} = 100 ms	10	Class C
Battery Brownout/Recovery VBAT = 13.5 V	T1 = 1 s, T2 = 10 s, T3 = 28800 s, T4 = 10 s, T5 = 7200 s	1	Class C
Triangular Pulse 1 VBAT_start = 12 V, VBAT_stop = 0 V, VBAT_max = 13.5 V	Slope = 0.1 V / µs	3	Class A
	Slope = 1 V / s	3	Class C
	Slope = 1 V / min	3	Class C
Triangular Pulse 2 VBAT_start = 12 V, VBAT_stop = 0 V	Fall time from 2 min to 30 min by step of 2 min	1	Class C
	Fall time from 1 h to 7 h by step of 2 h	1	Class C
	Rise time from 2 min to 30 min by step of 2 min	1	Class C
	Rise time from 1 h to 7 h by step of 2 h	1	Class C
Re-init pulse VBAT = 13.5 V	tr/tf = 1 ms, td = 5 s, T = 10 s, 20 steps by 5 %	1	Class C
LV124[24] E-07 UBmax = VBATmax = 12 V, UBmin = VBATmin = xV	Slope 0.5 V / min	1	Class C
LV124[24] E-08 UBmax = VBATmax = 12 V, UBmin = VBATmin = xV	Slope = 0.5 V/min Holding at 0 V = 1 min Tr < 0.5 s	1	Class C
LV124[24] E-09 VBAT_start = 13.5 V, VBAT_stop = 0 V,	Frequency = 0.06 Hz duty cycle = 0.5	1	Class C
LV124[24] E-10 VBAT = 11 V, T2 = 10s	T1 > 10 µs to 100 µs with interval of 10 µs T1 = 100 µs to 1 ms with interval of 100 µs	1	Class A
	T1 = 1 ms to 10 ms with interval of 1 ms T1 = 10 ms to 100 ms with interval of 10 ms T1 = 100 ms to 2 s with interval of 100 ms	1	Class C

Results depend on the use case condition. Table 12 does not include all the possible, custom non-ISO test pulses applied to FS84/FS85. Only one third of the most common tests are listed. Contact your local NXP representative if custom pulses are needed for your application.

15 EMC performance

15.1 PCB components placement

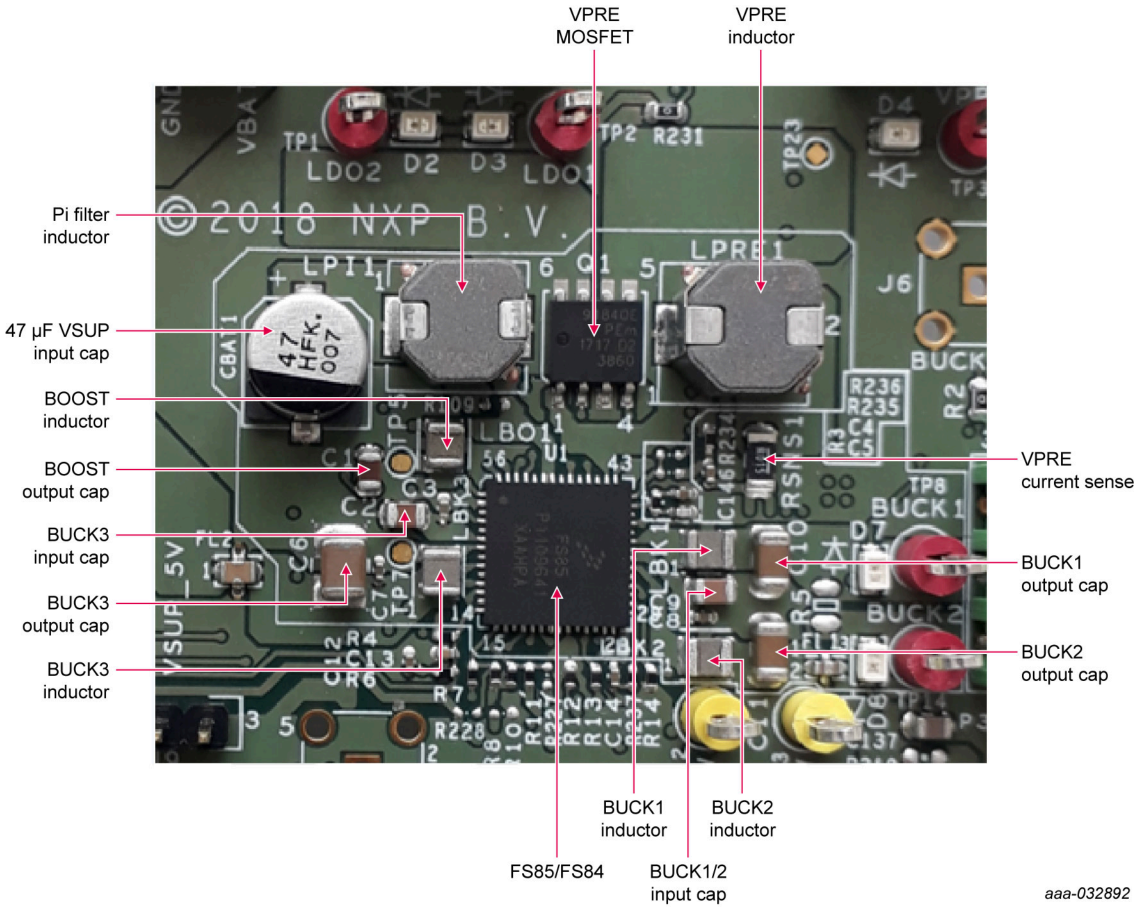


Figure 25. PCB component placement

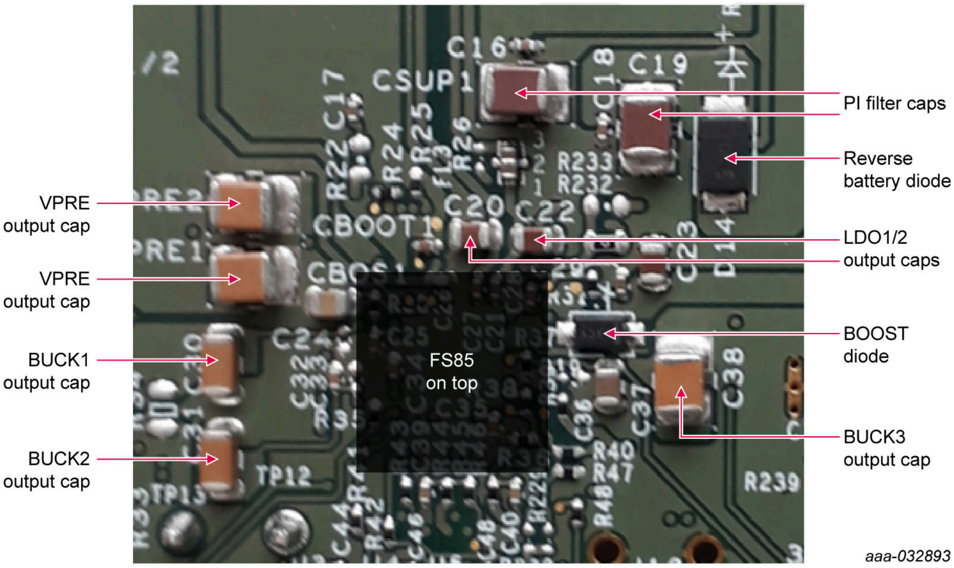


Figure 26. PCB component placement

15.2 Layout guidelines

- Design uses 6 PCB layers:
  - L1 : Top layer used as DC/DC power plane
  - L2 : System ground
  - L3 : Power Island / Signal
  - L4 : System Ground
  - L5 : Signal
  - L6 : DC/DC local power plane
- If a high current loop is going through multiple PCB layers, multiple vias are recommended to limit the parasitic (R and L) in the high current path
- When a signal is going thru multiple PCB layers, ground vias around the layer interconnection are recommended to contain the electrical field
- Avoid low level signals below SMPS power components
- Connect components with high-impedance signals close to device pin to avoid noise injection
- SMPS current loop as small as possible with wide tracks
- SMPS feedback lines shall be shielded
- BUCK1/2/3 feedbacks shall be connected close to the load
- When BUCK1/2 are used in multiphase, BUCK1 and BUCK2 layout shall be as symmetrical as possible
- VPRE feedback is also used for Current Sense Negative, so VPRE feedback shall be connected to Rshunt and not to the load
- Layout of VDDIO (VDDI2C) must avoid parasitic coupling with global pins
- Add decoupling capacitors on VDDIO (VDDI2C) close to the power supply pins of level shifters
- All global pins connected to a single connector is the best solution for EMC system level tests
- Change VPRE HS slew rate to slower settings to improve above 200/300 MHz (in Radiated Emission)
- Preferable to use suggested inductors' references for PI filter and VPRE
- Radiated Emission can be minimized if VPRE ripple is minimized, pay close attention on BOM selection (compensation network, capacitors, etc) to minimize ripple
- Keep close attention to VPRE layout and follow datasheet guidelines

Refer to the *Layout and PCB guidelines* section of the product data sheet for additional information

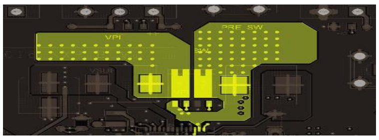
15.3 Thermal management

15.3.1 Package with exposed pad

The FS84/FS85 package is a QFN 56-pin package with an exposed pad for enhanced thermal dissipation. Details of the PCB footprint design are available in the section titled *PCB footprint design* of AN1902[15].

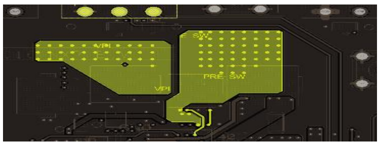
15.3.2 VPRE MOSFET power dissipation

- To minimize the power dissipation in VPRE external MOSFETs, a minimum PCB copper area can be used for this purpose. The application note, AN10874[16] provides useful information.
- On NXP EVB design, 70 µm copper layer thickness for top and bottom layers are used to improve the dissipation. The power dissipation in the MOSFETs is optimized by the copper areas on Layers 1 (Figure 27), 3 (Figure 28) and 6 (Figure 29).



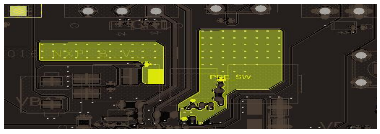
aaa-032894

Figure 27. Layer 1



aaa-032895

Figure 28. Layer 3



aaa-032896

Figure 29. Layer 6

15.4 Product setup

All EMC tests are performed at 25 °C, with all regulators configured and loaded according to the *EMC compliance* section of the product data sheet.

15.5 Conducted Emission (CE)

Compliance to IEC 61967-4:[21]

- Global pins: VBAT (Vsup1 and Vsup2), FS0B, 150 Ω method, 12-M level
- Local pins: VPRE, VBOOST, BUCK1/2/3, LDO1/2, 150 Ω method, 10-K level

The main parameters for the emission measurements are described in Table 13 according to the IEC specification.

Table 13. Emission measurements main parameters

Frequency range	Resolution bandwidth RBW	Step size
150 kHz to 30 MHz	9 kHz	4.5 kHz
30 MHz to 1 GHz	120 kHz	60 kHz

VBAT results are obtained with spread spectrum enabled and the external components discussed in Section 6. For spread spectrum information, refer to the *Spread spectrum* section of the product data sheet.

VPRE results are obtained after ferrite Murata BLM31PG601SH1 + 100 nF to GND.

VBOOST results are obtained after ferrite Murata BLM31PG601SH1 + 47 nF to GND.

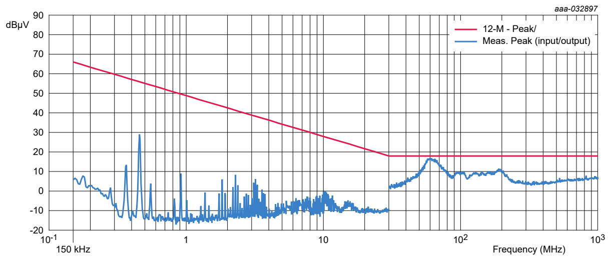


Figure 30. VBAT with VPRE = 455 kHz

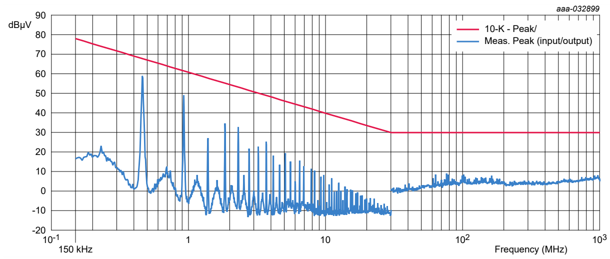


Figure 31. VPRE @ 455 kHz

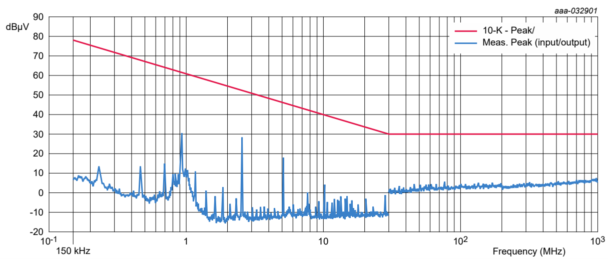


Figure 32. VBOOST @ 2.22 MHz

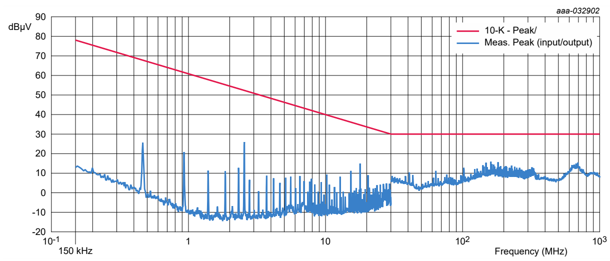


Figure 33. LDO1/2

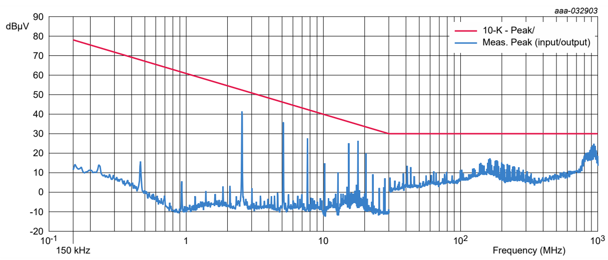


Figure 34. BUCK1/2 @ 2.22 MHz

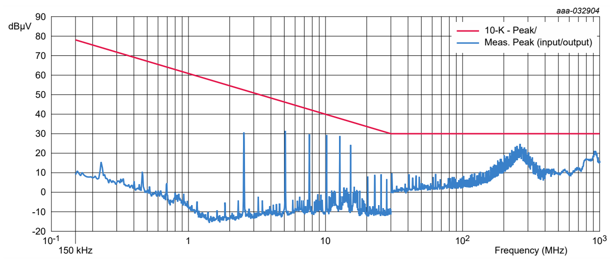


Figure 35. BUCK3 @ 2.22 MHz

15.6 Direct Power Injection (DPI)

Compliance to IEC 62132-4:[22]

- Global pins (supplies): VBAT (Vsup1 and Vsup2), 36 dBm, Class A
- Global pins (non-supplies): WAKE1, WAKE2, FS0B, 30 dBm, Class A
- Local pins (supplies): VPRE @455 kHz, BUCK1/2/3 @ 2.22 MHz, LDO1/2, 12 dBm, Class A
- Local pins (non-supplies): RSTB, PGOOD, VDDIO, VDDI2C, VBOS, 12 dBm, Class A

Class A: no state change on FS0B, RSTB, PGOOD state and all regulators in spec

Table 14. DPI results

Pin	Classification	Level	Result
VBAT (Vsup1, Vsup2)	Global	36 dBm	**PASS**
WAKE1 and WAKE2	Global	30 dBm	**PASS**
FS0B	Global	30 dBm	**PASS**
WAKE2	Local	12 dBm	**PASS**
VPRE	Local	12 dBm	**PASS**
BUCK1, BUCK2	Local	12 dBm	**PASS**
LDO1, LDO2	Local	12 dBm	**PASS**

Table 14. DPI results*...continued*

Pin	Classification	Level	Result
BUCK3, VDDIO	Local	12 dBm	**PASS**
VDDI2C	Local	12 dBm	**PASS**
VBOS	Local	12 dBm	**PASS**
RSTB	Local	12 dBm	**PASS**
PGOOD	Local	12 dBm	**PASS**

15.7 Radiated Emission (RE)

Compliance with FMC1278[23] RE 310 Level 2 Requirement in Normal mode

Table 15. Limits in dB µV/m, level 2

Frequency (MHz)	G1 0.53 - 1.7	NA1 45 - 48	G2 65 - 88	JA1 75 - 91	G3 89 - 109	G4 140 - 176	G5 172 - 242
Limit A, PK	20	20	20	20	20	20	20
Limit A, AV	12	12	12	12	12	12	12
Limit B, QP	30	24	24	24	24	24	24

Frequency (MHz)	G6a 310 - 320	EU3 380 - 430	G6b 429 - 439	G7a 868 - 870	G67b 902 - 904	EU4 1598 - 1604
Limit A, PK	20	20	25	30	30	—
Limit A, AV	14	14	19	24	24	4
Limit B, QP	30	30	30	—	—	—

Frequency (MHz)	G8 1567 - 1574	G8 1574 - 1576	G8 1576 - 1583
Limit A, AV	44 – 20664 × log(f/1567)	4	4 + 20782 × log(f/1576)

15.7.1 RE setup

- VBAT = 13.5 V, Room temperature (23 °C)
- LISN is used only on Battery +
- Battery ground is connected on the ground plane.
- Ground to DUT is done with a wire.

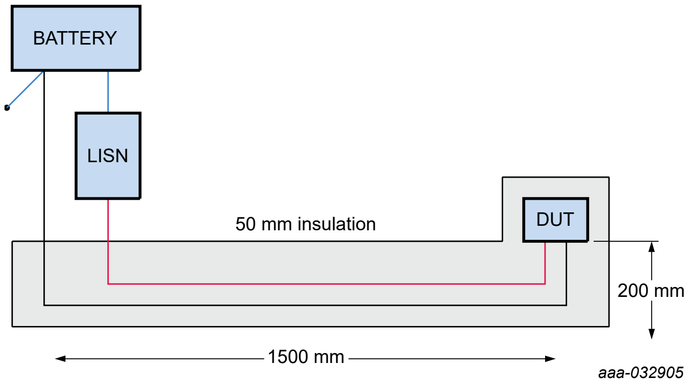


Figure 36. Radiated emission setup diagram

Table 16. Radiated emission test settings

Setting	Range
Frequency Range	0.15 - 1605 MHz
Bandwidth acc. to CISPR 25	1 / 9 / 120 kHz
Frequency Step Δf	0.25 / 2.25 / 30 kHz (FFT)
Measuring time	200 ms / QP: 1000 ms
Detector	Peak (PK) / Average (AV) / Quasi-Peak (QP)

15.7.2 RE results

Figure 37. Radiated emission test setup: board shielded, spread spectrum enabled, VPRE @ 455 kHz, SRLS = 11, SRHS = 00

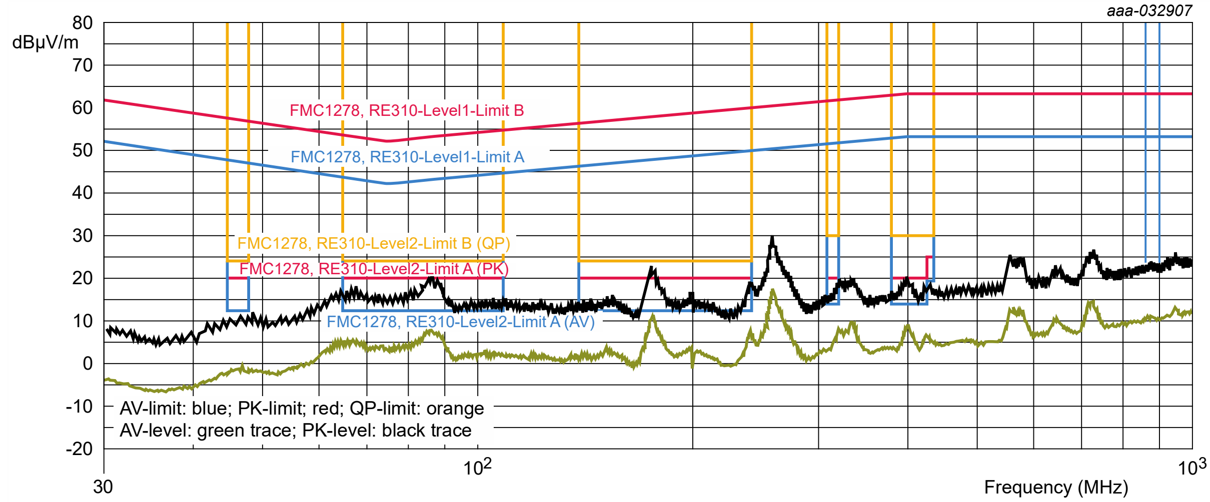


Figure 38. Radiated emission results: compliant for 12 kHz PK/AV BW limits

Table 17. Settings for radiated emission results: compliant for 12 kHz PK/AV BW limits

Setting	Value
f	30 - 1000 MHz
Δf	30 kHz (FFT)
Det.	PK / AV
BW	120 kHz
T	200 ms
Antenna	Horizontal

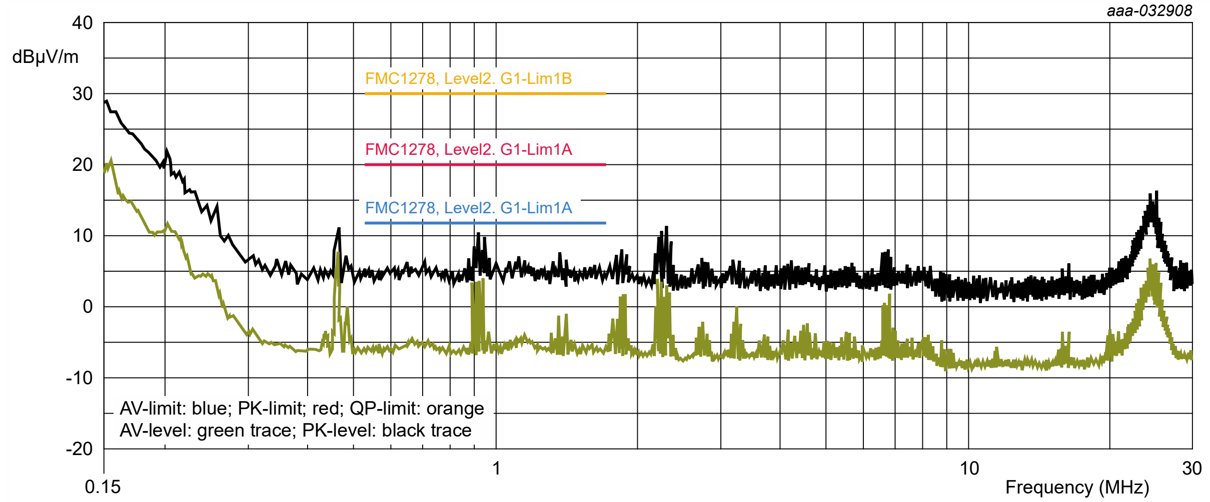


Figure 39. Radiated emission results: compliant for 9 kHz PK/AV BW limits

Table 18. Settings for radiated emission results: compliant for 9 kHz PK/AV BW limits

Setting	Value
f	0.15 - 30 MHz
Δf	2.25 kHz (FFT)

Table 18. Settings for radiated emission results: compliant for 9 kHz PK/AV BW limits*...continued*

Setting	Value
Det.	PK / AV
BW	9 kHz
T	200 ms
Antenna	Vertical

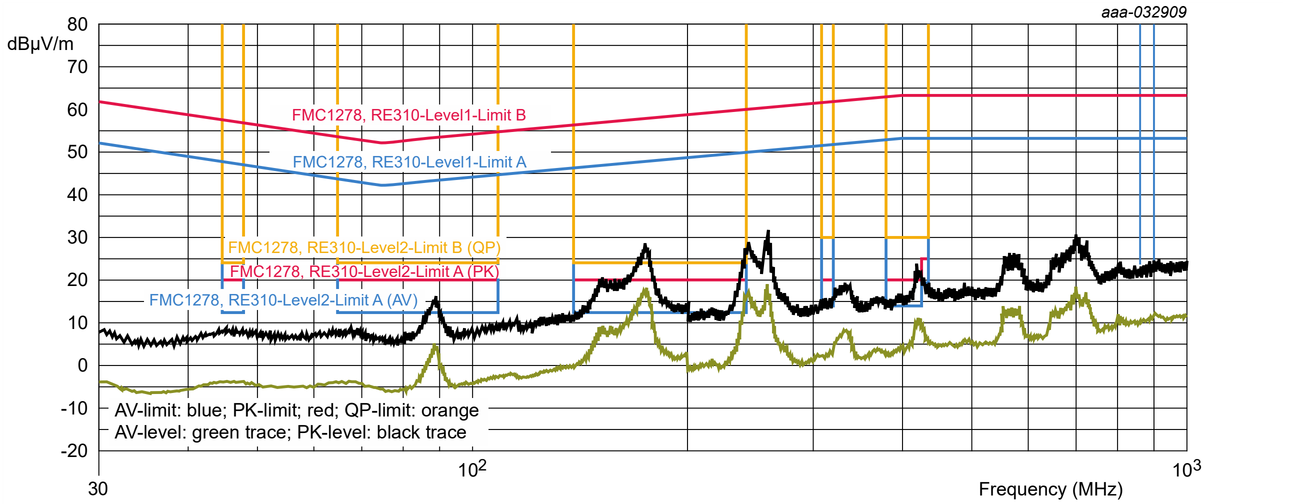


Figure 40. Radiated emission results: compliant for 12 kHz PK/AV BW limits

Table 19. Settings for radiated emission results: compliant for 12 kHz PK/AV BW limits

Setting	Value
f	30 - 1000 MHz
Δf	30 KHz (FFT)
Det.	PK / AV
BW	120 kHz
T	200 ms
Antenna	Vertical

15.8 Bulk Current Injection (BCI)

- Injection level per FMC1278[23] RI 112 Level 2 Requirement in Normal mode, FS0B released and no assertion
- Injection level per FMC1278[23] RI 112 Level 2 Requirement in Normal mode, FS0B asserted and no release
- No wake up when injecting FMC1278[23] RI 112 Level 2 Requirement in standby mode

15.8.1 BCI setup

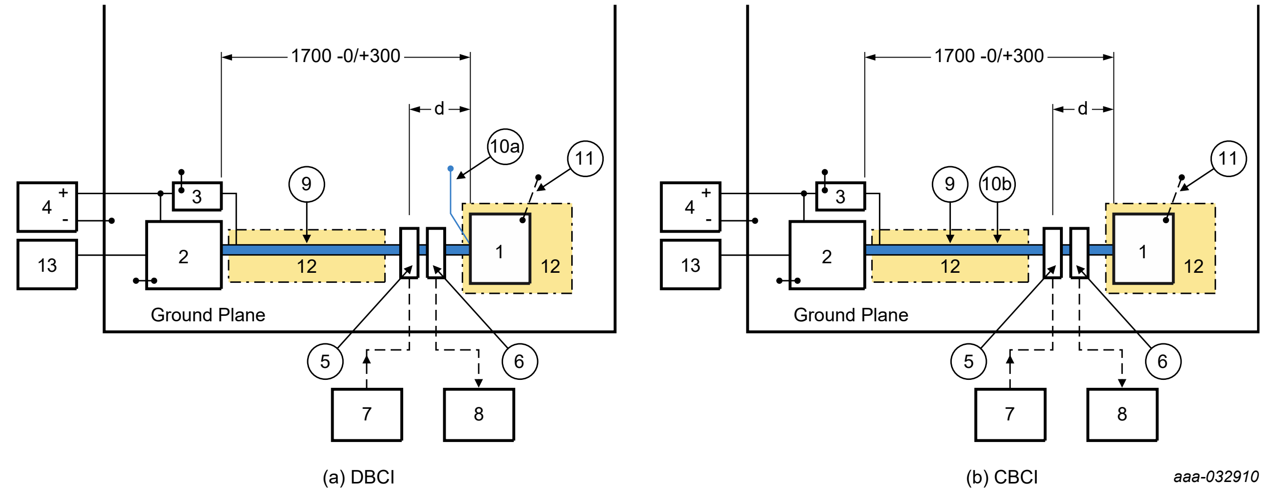


Figure 41. Bulk current injection setup

Table 20. BCI setup

Key	
1. DUT	8. Current monitoring equipment
2. Load simulator	9. DUT wire harness
3. Artificial network	10a. DUT power return removed from wire harness and connected directly to sheet metal. Wire length is 200 mm ± 50 mm.
4. Power supply	10b. DUT power return included in DUT wire harness
5. Injection probe	11. DUT case ground (refer to section 12.2, *Generic Test Setup* of FMC1278[23])
6. Monitor probe (requires prior approval by FMC EMC approval to use).	12. dielectric support ($\varepsilon_r \leq 1.4$)
7. RF generation equipment	13. Support/monitoring equipment

15.8.2 BCI results

Table 21. BCI test results

BCI test	Mode	Result
CBCI 150 mm	Normal	**PASS**
CBCI 450 mm	Normal	**PASS**
CBCI 750 mm	Normal	**PASS**
DBCI 150 mm	Normal	**PASS**
DBCI 450 mm	Normal	**PASS**
CBCI 150 mm	Standby	**PASS**
CBCI 450 mm	Standby	**PASS**
CBCI 750 mm	Standby	**PASS**
DBCI 150 mm	Standby	**PASS**

Table 21. BCI test results*...continued*

BCI test	Mode	Result
DBCI 450 mm	Standby	**PASS**

16 VBOOST to supply CAN transceivers

The VBOOST block can be used to supply CAN transceivers' peripherals. A critical topic to supply a CAN transceiver, such as the TJA1042, is the transient load requirement. To estimate what transient requirement the CAN supply must be compliant with, the system designer shall consider the various CAN short scenario possible. There are different scenarios of a CAN shorted, the worst case scenario among them being CANH short to Battery. In the case of TJA0142, this scenario draws 110 mA max while CAN is in the dominant state, and 10 mA max while CAN is in the recessive state. See Chapter 3 of https://www.nxp.com/docs/en/data-sheet/TJA1042.pdf.

In most cases, CAN is in the dominant state 50 % of the time and recessive state 50 % of the time, involving a short current of 110 × 0.5 + 10 × 0.5 = 60 mA. Worst case, CAN can be considered to be dominant for 80 % of the time, and thus bringing the short current to 110 × 0.8 + 10 × 0.2 = 90 mA.

Based on this scenario, a CAN shorted worst case would involve a 90 mA peak current on its input VCC.

To prevent fast transient on VCC pin from the CAN transceiver, there must be a decoupling capacitor. For a decoupling capacitor of 100 nF on VCC, and taking in consideration a 100 mA peak for a CAN input of 5 V (50 ohm load), the time constant is R × C = 50 × 100 nF = 5 µs. Thus, it means the capacitor will be fully discharged after 6 × Tau = 30 µs.

Based on this study, the CAN supply must be compliant with 100 mA short within 5 µs, so 20 mA/µs transient load.

The TJA1042 VCC input voltage requirement is 5 % overall. The VBOOST from FS8500 is rated at 3 % DC accuracy, so the VBOOST must be compliant with 2 % on AC accuracy. For a 5 V supply, a transient of 2 % means the supply overshoot/undershoot upon a transient event on VBOOST must be within 100 mV. Based on FS8500 datasheet and validation data, which shows that for such use case the VBOOST sustain an overshoot below 100 mV, it confirms the VBOOST as a technical working solution to supply such CAN transceiver.

Additional information can be found in application note (https://www.nxp.com/docs/en/supporting-information/AH1014.pdf), on Chapter 7.1.1 for VCC input cap, and 7.1.3 on bypass cap (VBOOST cap) dimensioning. Refer to these documents to confirm that VBOOST can properly supply this CAN transceiver.

17 Interface customer module with NXP GUI by I^2C

During engineering development only, it is possible to emulate or program an OTP configuration in FS84/FS85 device on customer module using a KL25z freedom interface. This board is providing USB to I^2C interface. The hardware connection between the freedom board and the customer board is detailed in Figure 42.

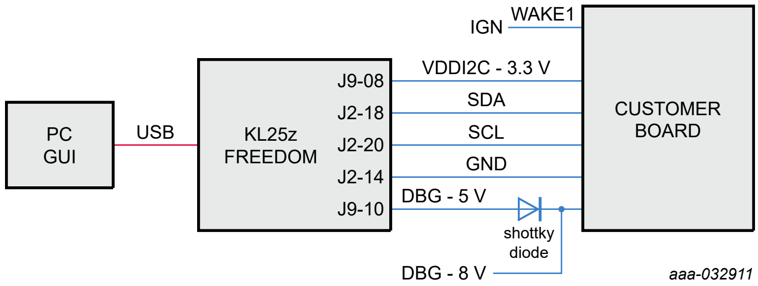


Figure 42. I²C interface with KL25z freedom board

- Ignition connected to WAKE1 to start the device
- DBG = 5 V used for emulation mode
- DBG = 8 V used for OTP burning (external power supply)
- GUI revision:
  - 0.5.4 with fs85-b0-i2c-config-freedom-v1.0.3-ctm.flgi configuration file
  - or 0.7.4 or above selecting FS85_with_KL25z_board_interface kit at startup
- KL25z firmware: NXP_FlexGUI_Firmware_v0.2.1.s19
- Default I²C address configured: 0x20 for the Main and 0x21 for the Fail-safe. If different, to be configured in the GUI before starting communication

OTP Emulation:

- Apply DBG voltage (5 V) and Vsup.
- Apply Wake 1.
- Load OTP script with the GUI.
- Release DBG voltage (back to GND with on board pull down).

OTP Burning:

- Apply DBG voltage (5 V) and Vsup.
- Apply Wake 1.
- Load OTP script with the GUI.
- Burn the OTP with the GUI.
- The GUI will open some pop-up to follow.
- The user will be asked to apply DBG = 7.95 V at DBG - 8 V input. See Figure 42.

18 Known behaviors

18.1 Set FLT_ERR_CNT_LIMIT[1:0] = 00

When the device powers up, FLT_ERR_CNT = 1 is set by default. When FLT_ERR_CNT_LIMIT[1:0] = 00 is set by the software during the INIT_FS phase, the Fault error counter intermediate value is configured to 1. RSTB is asserted for each value of FLT_ERR_CNT >= intermediate value.

The action of the configuration is done immediately after writing in the FS_I_FSSM register, it’s not waiting until the related FS_I_NOT_FSSM is also written. That means the fault error counter intermediate value generates a reset by default. As a consequence, the device goes out of INIT_FS and sets the REG_CORRUPT to a value of 1, then releases RSTB and enters INIT_FS again.

There are three possible solutions to avoid RSTB pulse:

1. Decrement the FLT_ERR_CNT before changing FLT_ERR_CNT_LIMIT[1:0] = 00.
   a. Write the initialization configuration on INIT_FS state without changing FLT_ERR_CNT_LIMIT[1:0]
   b. Write one good watchdog refresh to close the INIT_FS phase
   c. Decrement the FLT_ERR_CNT with several good watchdog refreshes (see WD_RFR_LIMIT[1:0])
   d. Write GOTO_INITFS = 1 to go back to INIT_FS state
   e. Change FLT_ERR_CNT_LIMIT[1:0] = 00
   f. Complete the initialization configuration
   g. Write one good watchdog refresh to close the INIT_FS phase
2. Disable the FLT_ERR_IMPACT[1:0] reaction on RSTB before closing the INIT_FS phase, then re-enable RSTB reaction.
   a. Write the initialization configuration on INIT_FS state
   b. Write FLT_ERR_IMPACT[1:0] = 01
   c. Change FLT_ERR_CNT_LIMIT[1:0] = 00
   d. Write one good watchdog refresh to close the INIT_FS phase
   e. Decrement the FLT_ERR_CNT with several good watchdog refreshes (see WD_RFR_LIMIT[1:0])
   f. Write GOTO_INITFS = 1 to go back to INIT_FS state
   g. Write FLT_ERR_IMPACT[1:0] = 11
   h. Complete the initialization configuration
   i. Write one good watchdog refresh to close the INIT_FS phase
3. Disable the FLT_ERR_IMPACT[1:0] reaction on RSTB before closing the INIT_FS phase.
   a. Write the initialization configuration on INIT_FS state
   b. Write FLT_ERR_IMPACT[1:0] = 01
   c. Change FLT_ERR_CNT_LIMIT[1:0] = 00
   d. Write one good watchdog refresh to close the INIT_FS phase

After operation options 1 and 2, the device will still generate an RSTB pulse when FLT_ERR_CNT = 1. After option 3, the device won’t generate an RSTB pulse when FLT_ERR_CNT = 1, because the RSTB reaction is disabled.

19 References

[1] **FS84_FS85C** — Fail-safe system basis chip with multiple SMPS and LDO product data sheet
http://www.docstore.nxp.com
FS8400 product information web page https://www.nxp.com/FS8400
FS8500 product information web page https://www.nxp.com/FS8500

[2] **FS85_PDTCALC** — VPRE compensation network calculation and power dissipation tool (Excel file)
https://www.nxp.com/downloads/en/calculators/FS85-PDTCALC.xlsx

[3] **FS85_FS84_OTP_Config.xlsm** — OTP programming configuration (Excel file)
https://www.nxp.com/webapp/Download?colCode=FS85-FS84-OTP&appType=moderatedWithoutFAE

[4] **FS85_Dynamic_FMEDA_C**[1] http://www.docstore.nxp.com — FMEDA analysis

[5] **FS84_FS85SMUGC** — FS84/FS85 functional safety manual http://www.docstore.nxp.com

[6] **FS85_VPRE_Simplis_Model**[1] — Simplis model for stability and transient simulations

[7] **Schematic**[1] — Reference schematic in Cadence and PDF formats

[8] **Layout**[1] — Reference layout in Cadence format

[9] **KITFS85FRDMEVM** — FS84/FS85 12 V safety SBC evaluation board (EVB) for automotive
http://www.nxp.com/KITFS85FRDMEVM

[10] **KITFS85AEEVM** — FS84/FS85 24 V/36 V safety SBC evaluation board (EVB) for truck
http://www.nxp.com/KITFS85AEEVM

[11] **KITFS85SKTEVM** — FS84/FS85 safety SBC programming board http://www.nxp.com/KITFS85SKTEVM

[12] **FlexGUI** — Software Tool for Evaluation of Reference Design Kits https://www.nxp.com/design/:FLEXGUI-SW

[13] **SW drivers rev 1.1** — SDK software drivers https://www.nxp.com/design/:FS8500-FS8400-SW-DRIVER

[14] **UM10204** — I^2C-bus specification and user manual https://www.nxp.com/docs/en/user-guide/UM10204.pdf

[15] **AN1902** — Assembly guidelines for QFN (quad flat no-lead) and SON (small outline no-lead) packages application note https://www.nxp.com/files/analog/doc/app_note/AN1902.pdf

[16] **AN10874** — LFPAK MOSFET thermal design guide application note
http://assets.nexperia.com/documents/application-note/AN10874.pdf

[17] **AN12540** — FS85 VPRE stability application note https://www.nxp.com/docs/en/application-note/AN12540.pdf

[18] **ISO 7637-2:2011(E)** — *Road Vehicles – Electrical disturbances from conduction and coupling – Part 2: Electrical transient conduction along supply lines only*, International Standards Organization.

[19] **ISO 16750-2:2010(E)** — *Road vehicles – Environmental conditions and testing for electrical and electronic equipment – Part 2: Electrical loads*, International Standards Organization.

[20] **ISO 16750-2:2012(E)** — *Road vehicles – Environmental conditions and testing for electrical and electronic equipment – Part 2: Electrical loads*, International Standards Organization.

[21] **IEC 61967-4:2002** — *Integrated circuits – Measurement of electromagnetic emissions, 150 kHz to 1 GHz - Part 4: Measurement of conducted emissions, 1 ohm/150 ohm direct coupling method*, International Electrotechnical Commission.

[22] **IEC 62132-4:2006** — *Integrated circuits – Measurement of electromagnetic immunity 150 kHz to 1 GHz – Part 4: Direct RF power injection method*, International Electrotechnical Commission.

[23] **FMC1278:2016** — *General Specification, Electrical/Electronic – Electromagnetic Compatibility Specification For Electrical/Electronic Components and Subsystems*, Ford Motor Company.

[24] **VW 80000: 2009-10**, Volkswagen AG implementation of LV 124, v 1.3 — *Electric and Electronic Components in Motor Vehicles up to 3.5 t – General Component Requirements, Test Conditions and Tests*

[1] Contact your NXP sales representative.

20 Revision history

Table 22. Revision history

Document ID	Release date	Description
AN12333 v.8	13 March 2024	• Section 3.5: Added copyright information to code block. • Section 20 was updated and relocated from the front of this document to the end to conform with NXP's document style and content hierarchy. • Updated Legal information
AN12333 v.7	12 September 2023	• Added Section 18
AN12333 v.6	15 February 2022	• Section 15.2: Added the last seven items in the list • Added Section 16
AN12333 v.5	22 September 2020	• Added Section 11 and Section 12.
AN12333 v.4	17 April 2020	• Section 7.2: revised calculation explanation to calculate DCR current sense components • Section 7.5: revised calculation explanation to calculate DCR current sense components • Section 7.7: added frequency analysis of the capacitor impedance and the current limit • Section 7.8: added a DCR components equations summary
AN12333 v.3	13 March 2020	• Section 4.3, Figure 7, revised the X-axis unit from "(µs)" to "(ms)" and revised the V(wake1) line to display at 12 V from 10 ms through 13 ms. • Section 6.7, Figure 9, updated the image adding a connection to VPRE near C27.
AN12333 v.2	06 November 2019	• Revised all "data sheet" references in the document to "the product data sheet" for brevity, leaving the full title of the data sheet in the reference section. • Section 4.2, revised 2nd and and 4th paragraphs. • Section 4.3, revised section including Figure 6 and Figure 7. • Section 6.1, removed "For VPRE = 455 kHz" from "PI filter". • Section 6.2, revised and added new bullet items under MOSFETs, Inductor, Output capacitor, Bootstrap capacitor and Rshunt. • Section 6.3, revised "Output capacitor" bullet from "Minimum 22 µF" to "Typical 44 µF". • Section 6.5, and Section 6.6, performed minor revisions to content • Section 6.7: revised the image in Figure 9. • Section 7.1, revised the title of the section from "DCR value lower than 15 mΩ" to "Low DCR value" and performed minor revisions to content. • Section 7.2, removed "(C_{LL} +" from 3rd paragraph. • Section 7.3, revised "109 mΩ" to "10 mΩ" in two locations. • Section 7.4, revised section title from "DCR value higher than 15 mohms" to "High DCR value", content, and Figure 12. • Section 7.5, revised content, including Table 3. • Section 7.6, revised "25 mΩ" to "20 mΩ", revised the paragraph before Figure 13, revised Figure 13, and the values in the supporting table. • Section 13.2, revised Table 8. • Section 14.2, revised the first paragraph and Table 11. • Section 14.3, revised the paragraph below Table 12. • Section 15.2, revised existing and added new content. • Section 15.7.2, revised titles for Table 17, Table 18, and Table 19. • Section 19, added new entries, revised existing entries and updated links.
AN12333 v.1	02 April 2019	Initial release

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Date of release: 13 March 2024
Document identifier: AN12333