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The MC145170 in Basic HF and VHF Oscillators

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Phase–locked loop (PLL) frequency synthesizers are commonly found in communication gear today. The carrier oscillator in a transmitter and local oscillator (LO) in a receiver are where PLL frequency synthesizers are utilized. In some cellular phones, a synthesizer can also be used to generate 90 MHz for an offset loop. In addition, synthesizers can be used in computers and other digital systems to create different clocks which are synchronized to a master clock.

The MC145170 is available to address some of these applications. The frequency capability of the newest version, the MC145170–2, is very broad — from a few hertz to 185 MHz.

ADVANTAGES

Frequency synthesizers, such as the MC145170, use digital dividers which can be placed under MCU control. Usually, all that is required to change frequencies is to change the divide ratio of the N Counter. Tuning in less than a millisecond is achievable.

The MC145170 can generate many frequencies based on the accuracy of a single reference source. For example, the reference can be a low–cost basic crystal oscillator or a temperature–compensated crystal oscillator (TCXO). Therefore, high tuning accuracies can be achieved. Boosting of the reference frequency by 100x or more is achievable.

ELEMENTS IN THE LOOP

The components used in the PLL frequency synthesizer of Figure 1 are the MC145170 PLL chip, low–pass filter, and voltage–controlled oscillator (VCO). Sometimes a voltage–controlled multivibrator (VCM) is used in place of the VCO. The output of a VCM is a square wave and is usually integrated before being fed to other sections of the radio. The VCM output can be directly used in computers and other digital equipment. The output of a VCO or VCM is typically buffered, as shown.

As shown in Figure 2, the MC145170 contains a reference oscillator, reference counter (R Counter), VCO/VCM counter (N Counter), and phase detector. A more detailed block diagram is shown in the data sheet.

HF SYNTHESIZER

The basic information required for designing a stable high–frequency PLL frequency synthesizer is the frequencies required, tuning resolution, lock time, and overshoot. For the example design of Figure 3, the frequencies needed are 9.20 MHz to 12.19 MHz. The resolution (usually the same as the frequency steps or channel spacing) is 230 kHz. The lock time is 8 ms and a maximum overshoot of approximately 15% is targeted. For purposes of this example, lock is considered to be when the frequency is within about 1% of the final value.

HF SYNTHESIZER LOW–PASS FILTER

In this design, assume a square wave output is acceptable. To generate a square wave, a MC1658 VCM chip is chosen. Per the transfer characteristic given in the data sheet, the MC1658 transfer function, K_{VCM}, is approximately 1×10^8 radians/second/volt. The loading presented by the MC1658 control input is large; the maximum input current is 350 μA. Therefore, an active low–pass filter is used so that loading does not affect the filter's response. See Figure 3. In the filter, a 2N7002 FET is chosen because it has very high transconductance (80 mmhos) and low input leakage (100 nA).

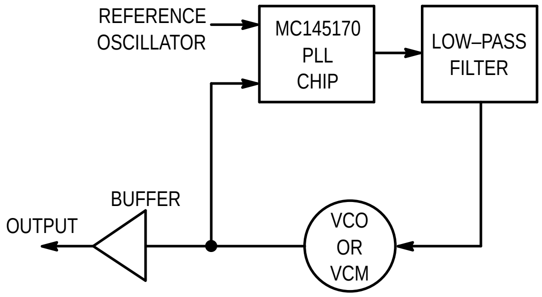

Figure 1. PLL Frequency Synthesizer

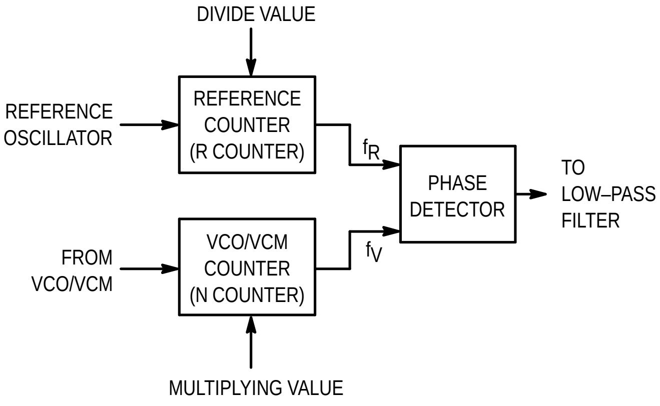

Figure 2. Detail of the MC145170

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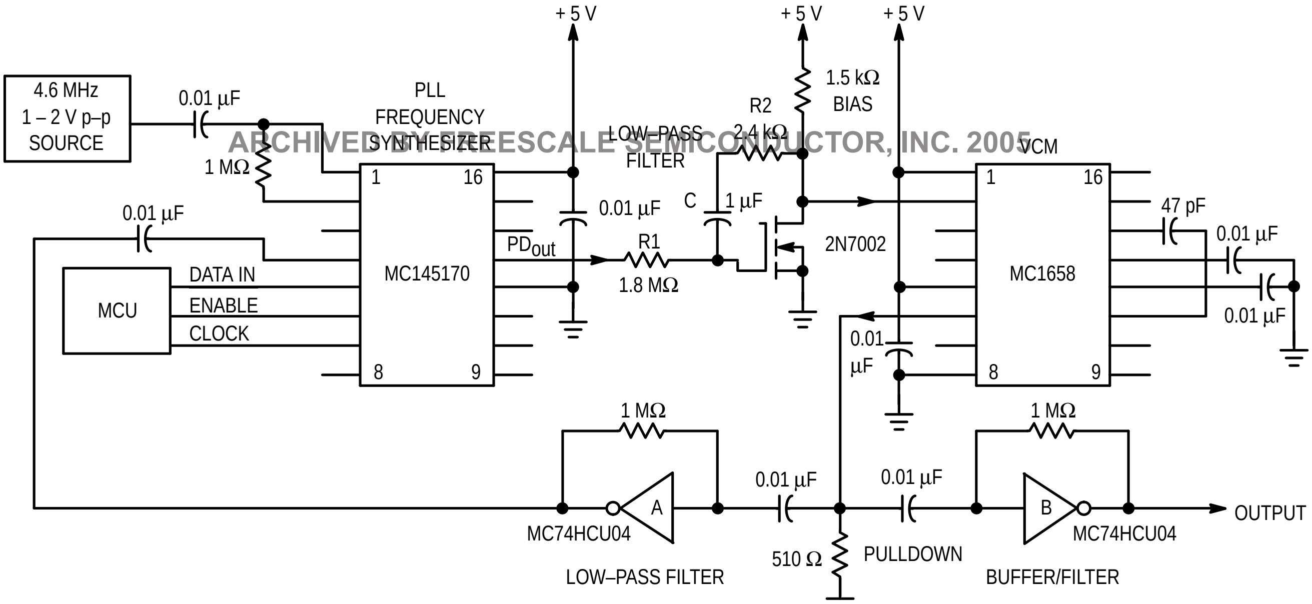

Figure 3. HF Synthesizer

In order to calculate the average divide value for the N Counter, follow this procedure. First, determine the average frequency; this is (12.19 + 9.2)/2 = 10.695 MHz or approximately 10.7 MHz. Next, divide this frequency by the resolution: 10.7 MHz/230 kHz = about 47.

Next, reference application note AN535 (see book DL136/D Rev 3 or 4). The active filter chosen takes the form shown in Figure 9 of the application note. This filter is used with the single–ended phase detector output of the MC145170, PD_{out}. The phase detector associated with PD_{out} has a gain $K_{\phi} = V_{DD}/4\pi$. For a supply of 5 V, this is $5/4\pi$ = 0.398 V/rad. The system's step response is shown in Figure 4. To achieve about 15% overshoot, a damping factor of 0.8 is used. This causes frequency to settle to within 1% at $\omega_n t$ = 5.5.

The information up to this point is as follows.

f_{ref} = 230 kHz
f_{VCM} = 9.2 to 12.19 MHz; the average is 10.7 MHz, average N = 47
power supply = 5 V for the phase detector
$K_{VCM} = 1 \times 10^8$ rad/s/V
overshoot = approximately 15%, yields a damping factor = 0.8
lock time t = 8 ms settling to within 1%, $\omega_n t = 5.5$
$K\phi$ or K_p = 0.398 V/rad.

From the application note, equation 61, $\omega_n = 5.5/t = 5.5/0.008 = 687.5$ rad/s.

Equation 59 is $R1C = (K_p K_V)/\omega_n^2 N$
$= (0.398 \times 1 \times 10^8)/687.5^2 \times 47$
$= 1.79$

Equation 59 is used because of the high–gain FET.

Next, the capacitor C is picked to be 1 µF. Therefore, R1 = 1.79/C which is 1.79 MΩ. The standard value of 1.8 MΩ is used for R1.

Equation 63 is $R2 = (2\zeta)/C\,\omega_n$
$= (2 \times 0.8)/(1 \times 10^{-6} \times 687.5)$
$= 2.33$ kΩ.

A standard value for R2 of 2.4 kΩ is utilized.

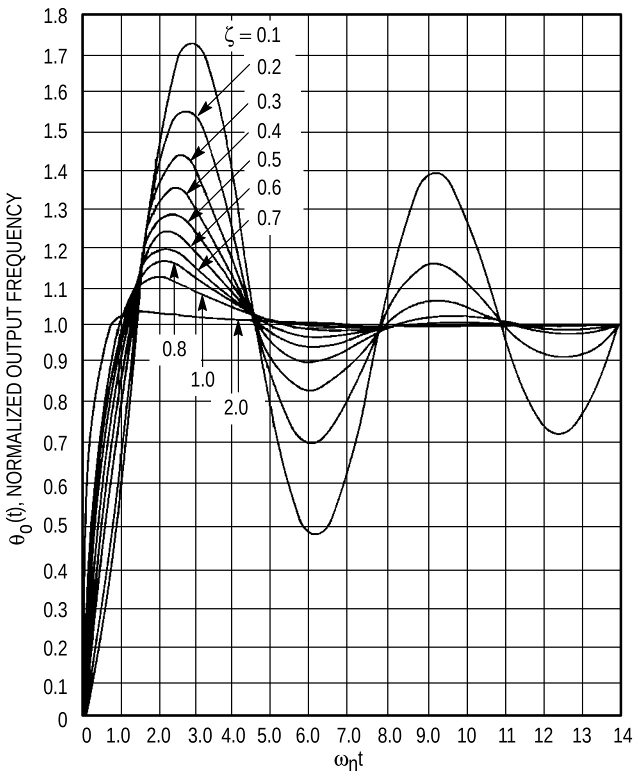

Figure 4. Type 2 Second Order Step Response

HF SYNTHESIZER PROGRAMMING

Programming the MC145170 is straightforward. The three registers may be programmed in a byte–oriented fashion. The registers retain their values as long as power is applied. Thus, usually both the C and R Registers are programmed just once, right after power up.

The C Register, which configures the device, is programmed with $C0 (1 byte). This sets the phase detector to the proper polarity and activates PD_{out}. This also turns off the unused outputs. The phase detector polarity is determined by the filter and the VCM. For this example, the MC1658 data sheet shows that a higher voltage level is needed if speed is to be increased. However, the low–pass filter inverts the signal from the phase detector (due to the active element configuration). Therefore, the programming of the polarity for the phase detector means that the POL bit must be a “1.”

The R Register is programmed for a divide value that results in the proper frequency at the phase detector reference input. In this case, 230 kHz is needed. Therefore, with the 4.6 MHz source shown in Figure 3, the R Register needs a value of $000014 (3 bytes, 20 in decimal).

The N Register determines the frequency tuned. Tuning 9.2 MHz requires the proper value for N to multiply up the reference of 230 kHz to 9.2 MHz. This is 40 decimal. For 12.19 MHz, the value is 53 decimal. To tune over the range, change the value in the N Register within the range of 40 to 53 with a 2–byte transfer. Table 1 shows the possible frequencies.

Table 1. The HF Oscillator Frequencies

N Value	Frequency, MHz
40	9.20
41	9.43
42	9.66
43	9.89
44	10.12
45	10.35
46	10.58
47	10.81
48	11.04
49	11.27
50	11.50
51	11.73
52	11.96
53	12.19

EXTRA FILTERING FOR THE HF LOOP

When the HF oscillator was built, the proper frequencies could not be tuned. The output of the MC1658 was examined with an oscilloscope and the switching edges were discovered to be “ragged.” That is, the output did not appear to be a square wave with clean transitions.

The f_{in} input of the MC145170 is sensitive to 500 mV p–p signals, and the ragged edges were being amplified and counted down by the N Counter. Therefore, the edges needed cleaning up. One method would have been to add a low–pass filter between the MC1658 and MC145170. However, because an additional buffer was needed elsewhere in the circuit, an MC74HCU04 inverter was used in place of the filter. This inverter’s frequency response is low enough to clean up the ragged edges. That is, filtering of the ragged edges occurred, and the output had smoother transitions. As mentioned previously, one of the elements in the inverter package was used to buffer the output of the VCM before feeding it to the outside world. See Figure 3.

VHF SYNTHESIZER

The MC145170 may be used in VHF designs, also. The range for this next example is 140 to 160 MHz in 100 kHz increments.

VHF SYNTHESIZER LOW–PASS FILTER

To illustrate design with the doubled–ended phase detector, the ϕ_R and ϕ_V outputs are used. This requires an operational amplifier, as shown in Figure 5. From the design guidelines shown in the MC145170 data sheet, the following equations are used:

$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{N\,C\,R_1}} \tag{1}$$

$$\text{damping factor} \quad \zeta = \frac{\omega_n R_2 C}{2} \tag{2}$$

where, from the data sheet, the equation for the ϕ_R and ϕ_V phase detector,

$$K_\phi = \frac{V_{DD}}{2\pi} = \frac{5}{2\pi} = 0.796 \text{ V/rad} \tag{3}$$

$$\zeta = 0.707,$$

$$\omega_n = \frac{2\pi f_R}{50} = \frac{2\pi \times 100 \text{ kHz}}{50} = 12{,}566 \text{ rad/s} \tag{4}$$

and

$$K_{VCO} = \frac{2\pi\,\Delta\, f_{VCO}}{\Delta\, V_{VCO}} = \frac{2\pi \times (160 - 140 \text{ MHz})}{10 - 2}$$

$$= 1.57 \times 10^7 \text{ rad/s/V} \tag{5}$$

The control voltage range on the input to the VCO is picked to be 2 to 10 V.

The average frequency = (140 + 160)/2 = 150 MHz. Therefore, the average N = 1500.

The above choices for ζ and ω_n are rules of thumb that are a good design starting point. A larger ω_n value results in faster loop lock times and higher reference frequency VCO sidebands for similar sideband filtering. (See Advanced Considerations.)

Choosing C_1 to be 4700 pF, R_1 is calculated from the rearranged expression for ω_n as:

$$R_1 = \frac{K_\phi K_{VCO}}{C_1 \omega_n^2 N} = \frac{(0.796 \text{ V/rad})(1.57 \times 10^7 \text{ rad/s/V})}{(4700 \text{ pF})(12{,}566 \text{ rad/s})^2\,(1500)}$$

$$= 11.23 \text{ k}\Omega \tag{6}$$

Therefore, chose an 11 kΩ standard value resistor.

R_2 is determined from:

$$R_2 = \frac{2\zeta}{\omega_n C_1} = \frac{(2)(0.707)}{(12{,}566)(4700 \text{ pF})}$$

$$= 23.94 \text{ k}\Omega \text{ or } 24 \text{ k}\Omega \text{ (standard value)} \tag{7}$$

VHF SYNTHESIZER EXTRA FILTERING

For more demanding applications, extra filtering is sometimes added. This reduces the VCO sidebands caused by a small amount of the reference frequency feeding through the filter. One form of this filtering consists of spitting R1 into two resistors; each resistor is one–half the value of R1, as indicated by R1/2 in Figure 5. Capacitors C_C are added from the

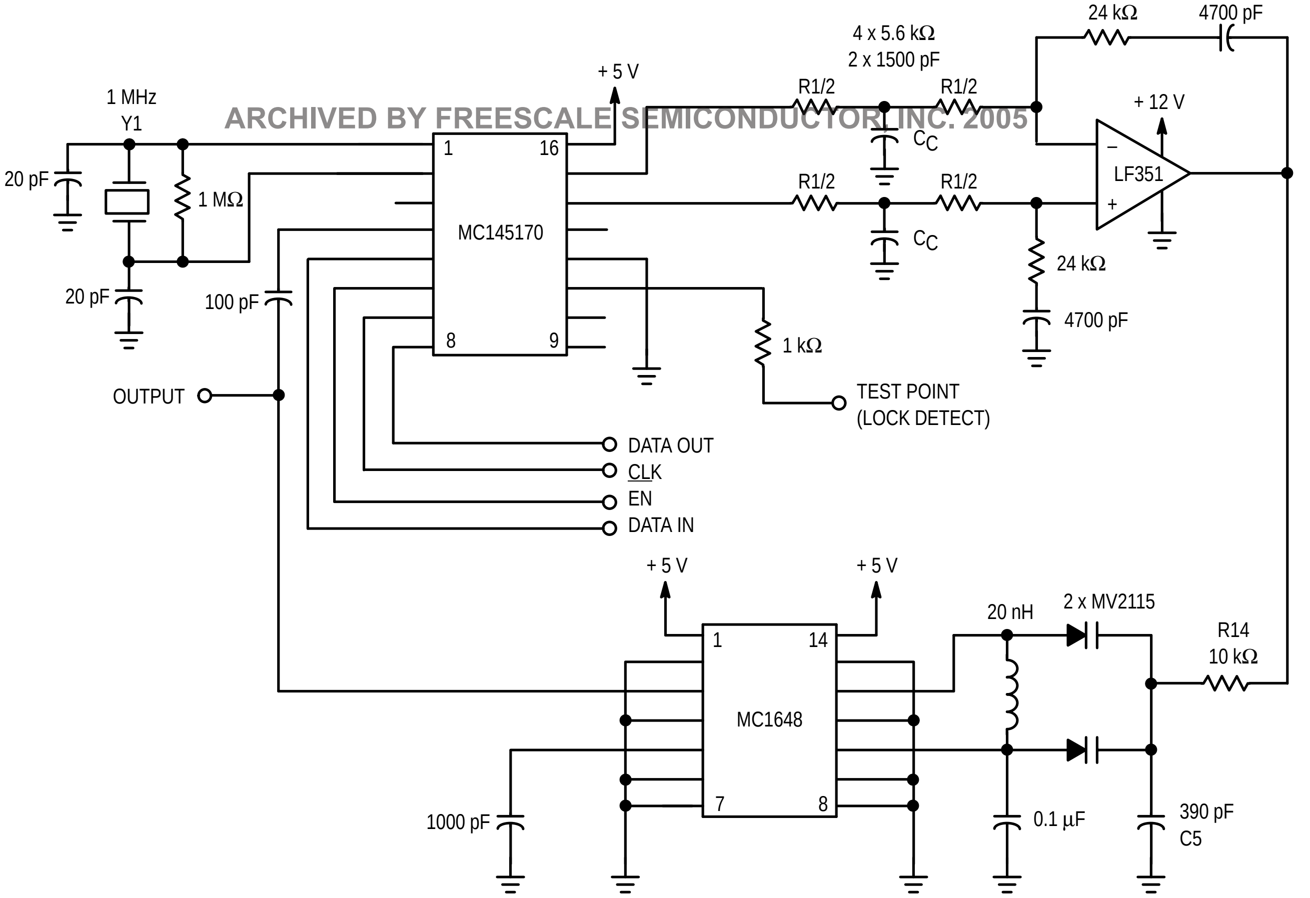

Figure 5. VHF Synthesizer

midpoints to ground to further filter the reference sidebands. The value of C_C is chosen so that the corner frequency of this added network does not significantly affect the original loop bandwidth ω_B.

The rule of thumb for an initial value is $C_C = 4 / (R1\ \omega_{RC})$, where ω_{RC} is the filter cutoff frequency. A good value is to choose ω_{RC} to be 10 x ω_B, so as to not significantly impact the original filter.

$$\omega_B = \omega_n \sqrt{1 + 2\zeta^2 + \sqrt{2 + 4\zeta^2 + 4\zeta^4}} \quad (8)$$

$$= 12{,}566\sqrt{1+(2)(0.707)^2+\sqrt{2+(4)(0.707)^2+(4)(0.707)^4}}$$

$$= 25{,}860 \text{ rad/s}$$

$$\omega_{RC} = 10\ \omega_B = (10)(25{,}860) = 258{,}600 \text{ rad/s} \quad (9)$$

$$C_C = \frac{4}{R1\omega_{RC}} = \frac{4}{(11.23\ k\Omega)(258{,}600 \text{ rad/s})} \quad (10)$$

$$= 1377 \text{ pF} \approx 1500 \text{ pF}$$

There is also a filter formed at the input to the VCO. Again, this should be selected to ensure that it does not significantly affect the loop bandwidth. For this example, the filter is dominated by R14 with C5. The capacitance of the varactors (in series with the rest of the circuit) is much smaller than C5 and can therefore be neglected for this calculation.

As above, let ω_{RC} = 258,600 rad/s be the cutoff of this filter. R14 is chosen to be 10 kΩ. Therefore,

$$C_5 = \frac{1}{\omega_{RC}R_{14}} = \frac{1}{(258{,}600)(10\ k\Omega)} \quad (11)$$

$$= 387 \text{ pF} \approx 390 \text{ pF}$$

THE VARACTOR

The MV2115 was selected for its tuning ratio of 2.6 to 1. The capacitance can be changed from 49.1 pF to 127.7 pF over a reverse bias swing of 2 to 30 volts. Contact your Motorola representative for information regarding the MV2115 varactor diode.

For example, three parameters are considered.

C_T = Nominal capacitance
CR = Capacitance ratio
fR = Frequency ratio

$$CR = \frac{C_V min}{C_V max} = \left(\frac{V_{max}}{V_{min}}\right)^{\rho} \quad (12)$$

where ρ = the capacitance exponent

Therefore,

$$CR = 2.6 = \left(\frac{30}{2}\right)^{\rho} \qquad (13)$$

$$\log(2.6) = \rho\log(15) \qquad (14)$$

$$\rho = \log(2.6)/\log(15) = 0.3528 \qquad (15)$$

Using the nominal capacitance of 100 pF at 4 volts:

$$\frac{100\text{ pF}}{C_v\text{max}} = \left(\frac{10}{4\text{ V}}\right)^{0.3528} \qquad (16)$$

$$\frac{100\text{ pF}}{C_v\text{max}} = 1.382$$

Solving for $C_v$max:

$$\frac{100\text{ pF}}{1.382} = 72.4\text{ pF}$$

Solving for $C_v$min:

$$2.6 = \frac{C_v\text{min}}{49.1\text{ pF}} \qquad (17)$$

$$C_v\text{min} = (2.6)(49.1\text{ pF})$$

$$C_v\text{min} = 127.7\text{ pF}$$

THE VCO

For convenience, the MC1648 VCO is selected. The tuning range of the VCO may be calculated as

$$\frac{f_{max}}{f_{min}} = \frac{(C_d\text{max} + C_S)^{0.5}}{(C_d\text{min} + C_S)^{0.5}} \qquad (18)$$

where

$$f_{min} = \frac{1}{2\pi[L(C_d\text{max} + C_S)]^{0.5}} \qquad (19)$$

As shown in Figure 8 of the data sheet, the VCO tank circuit is comprised of two varactors and an inductor. Typically, a single varactor might be used in either a series or parallel configuration. However, the second varactor has a two–fold purpose. First, if the 10 kΩ isolating impedance is left in place, the varactors add in series for a smaller capacitance. Second, the added varactor acts to eliminate distortion due to the tank voltage changing.

Therefore, with the two varactors in series, $C_d\text{max}' = C_d\text{max}/2$. The shunt capacitance (input plus external capacitance) is symbolized by C_S.

Therefore, solving for the inductance:

$$L = \frac{1}{(2\pi f_{min})^2(C_d\text{max}' + C_S)} = 19.9\text{ nH} \approx 20\text{ nH} \qquad (20)$$

The Q of the inductor should be more than 100 for best performance.

$$f_{min} = \frac{1}{2\pi[(19.9\text{ nH})(69.85\text{ pF})]^{0.5}} = 135\text{ MHz} \qquad (21)$$

$$f_{max} = \frac{1}{2\pi[(19.9\text{ nH})(42.2\text{ pF})]^{0.5}} = 173\text{ MHz} \qquad (22)$$

The frequency ratio is 1.5 to 1 and is impacted by the tuning range of the MV2115 varactor diode used in the tank circuit. Therefore, the required range of 140 to 160 MHz is not limited by this VCO design.

A pc board should be used to obtain favorable results with this VHF circuit. The lead lengths in the tank circuit should be kept short to minimize parasitic inductance. The length of the trace from the VCO output to the PLL input should be kept as short as possible. In addition, use of surface–mount components is recommended to help minimize strays.

VHF SYNTHESIZER PROGRAMMING

Again, programming the three registers of the MC145170 is straightforward. Also, usually both the C and the R Registers are programmed only once, after power up.

The C Register configures the device and is programmed with $80 (1 byte). This sets the phase detector to the correct polarity and activates the ϕ_R and ϕ_V outputs while turning off the other outputs. Like the HF oscillator, the phase detector polarity is determined by how the filter is hooked up and the VCO.

The R Register is programmed for a divide value that delivers the proper frequency at the phase detector reference input. In this case, 100 kHz is needed. Therefore, with the 1 MHz crystal shown, the R Register needs a value of $00000A (3 bytes, 10 in decimal).

The N Register determines the frequency tuned. To tune 140 MHz, the value required for N to multiply up the reference of 100 kHz to 140 MHz is 1400 decimal. For 160 MHz, the value is 1600 decimal. To tune over the range, simply change the value in the N Register with a 2–byte transfer.

ADVANCED CONSIDERATIONS

The circuit of Figure 5 may not function at very–high temperature. The reason is that the MC145170 is guaranteed to a maximum frequency of 160 MHz at 85°C. Therefore, there is no margin for overshoot (reference Figure 4) at high temperature. There are two possible solutions: (1) use the MC145170–1 or MC145170–2 which are rated to 185 MHz, or (2) limit the tuning to less than 160 MHz.

Operational amplifiers are usually too noisy for critical applications. Therefore, if an active element is required in the integrator, one or more discrete transistors are utilized. These may be FETs or bipolar devices. However, active filter elements are not needed if the VCO loading is not severe, such as is encountered with most discrete VCO designs. Because active elements add noise, some performance parameters are improved if they are not used. On the other hand, an active filter can be used to scale up the VCO control voltage. For example, to tune a wide range, the control voltage may have to range up to 10 V. For a 5 V PLL output, this would be scaled by 2x via use of active elements.

Some applications have requirements that must be met in the areas of phase noise and reference suppression. These parameters are in conflict with fast lock times. That is, as lock times are reduced, reference suppression becomes more difficult. Both reference suppression and phase noise are advanced areas that are covered in several publications. As an example, consider that the VCO input voltage range for the above VHF loop was merely picked to be 8 V. Advanced techniques demand a trade off between this voltage range and the spectral purity of the VCO output. This is because the lower the control voltage range, the more sensitive the VCO is to noise coming into its control input.

A VCO IC may not offer enough performance for some applications. Therefore, the VCO may have to be designed from discrete components.

Figure 6 shows the performance of the VHF Oscillator prototype on a spectrum analyzer. Note that the reference sidebands appear at 100 kHz as expected, and are 50 dB down.

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REFERENCES

Motorola data sheet MC145170/D
Motorola data sheet MC145170–1/D
Motorola data sheet MC145170–2/D
Motorola application note AN535/D

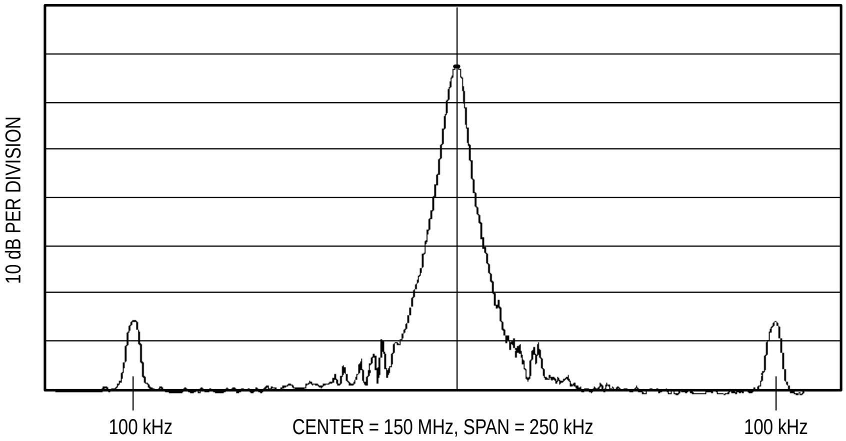

Figure 6. VHF Oscillator Performance

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