

AN11761

Flip chip die

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Application note

Document information

Information	Content
Keywords	Flip chip dies, bumped die
Abstract	This application note provides guidelines for the use of flip chip dies using plated solder bumps, or copper pillar bumps.



Revision history

Rev	Date	Description
5	20210929	updated Table 1 and Table 2
4	20200303	added copper pillar bumps
3	20161003	added additional remark in Section 2
2	20160510	replaced "bump pitch of 220 μm " by "bump pitch of 200 μm " throughout the document
1	20151207	initial version

1 Introduction

This application note provides guidelines for the use of flip chip dies with plated solder bumps, or copper pillar bumps, which are shipped to customers in tape and reel or on film frame carrier.

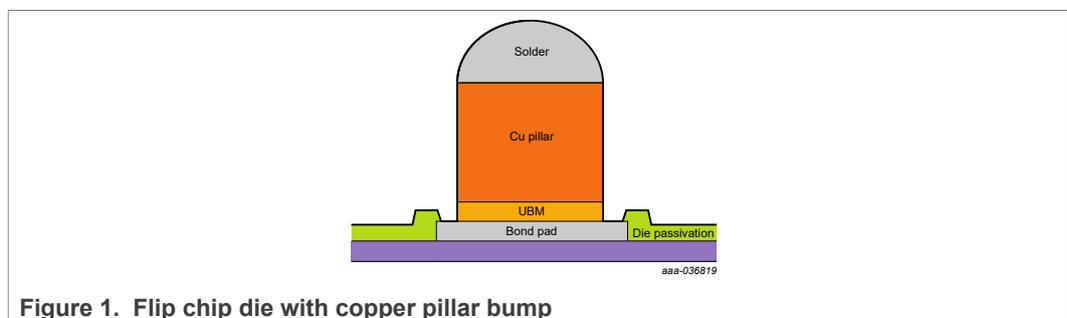
2 Package description

As with wafer level chip scale packages, flip chip dies offer the smallest package size possible with package size equal to die size. Solder or copper pillar bumps provide the interconnect means to the outside world. The difference between Wafer Level Chip Scale Packages (WLCSP) and flip chip dies is the application area. Whereas WLCSPs are mounted on a standard Printed-Circuit Board (PCB), flip chip dies are only used on high definition substrates, typically for interposers in modules and packages. Therefore, the bump diameter and bump pitch of flip chip dies are smaller than for WLCSP. Application notes for WLCSP are given in [AN10439 \[1\]](#). The interposer is the substrate that is used within a package or module.

To guarantee that board level reliability requirements are met, flip chip dies might require application-specific measures.

For of flip chip dies, two bump constructions can be distinguished:

Direct Bump: A copper pillar bump is placed on top of the IO without a repassivation layer. The Under Bump Metallization (UBM) is within the die passivation opening and provides adhesion and acts as barrier layer. [Figure 1](#) shows an example of such construction with copper pillar.



Repassivation: A plated solder bump is placed on top of the pad with a repassivation layer between the Under Bump Metallization (UBM) and the passivation of the die. The repassivation layer prevents cracking of the die passivation during temperature cycling. The UBM provides adhesion, acts as barrier layer, and ensures solder wetting. [Figure 2](#) shows an example of such construction with plated solder bump.

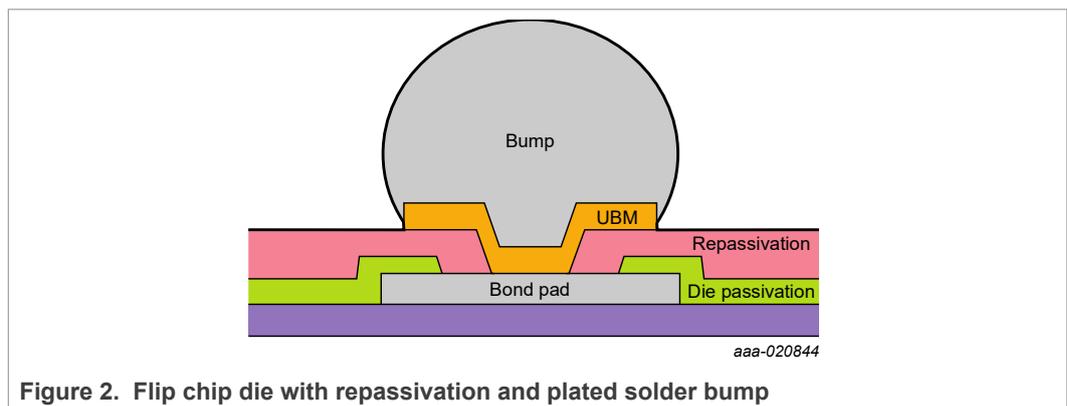


Figure 2. Flip chip die with repassivation and plated solder bump

3 Interposer design guidelines

A good interposer design ensures high electrical reliability performance when using a flip chip die. This design applies not only to the footprint design, but also to the location of the flip chip die product on the board.

3.1 Footprint layout

Figure 3 shows the commonly used Solder Mask Defined (SMD) solder pad for flip chip dies. SMD solder pads are used to avoid solder flow out on the part of the tracks. The recommended interposer solder pad dimensions are given in Table 1. Non-Solder Mask Defined (NSMD) solder pads are only used for pitches $\geq 300 \mu\text{m}$.

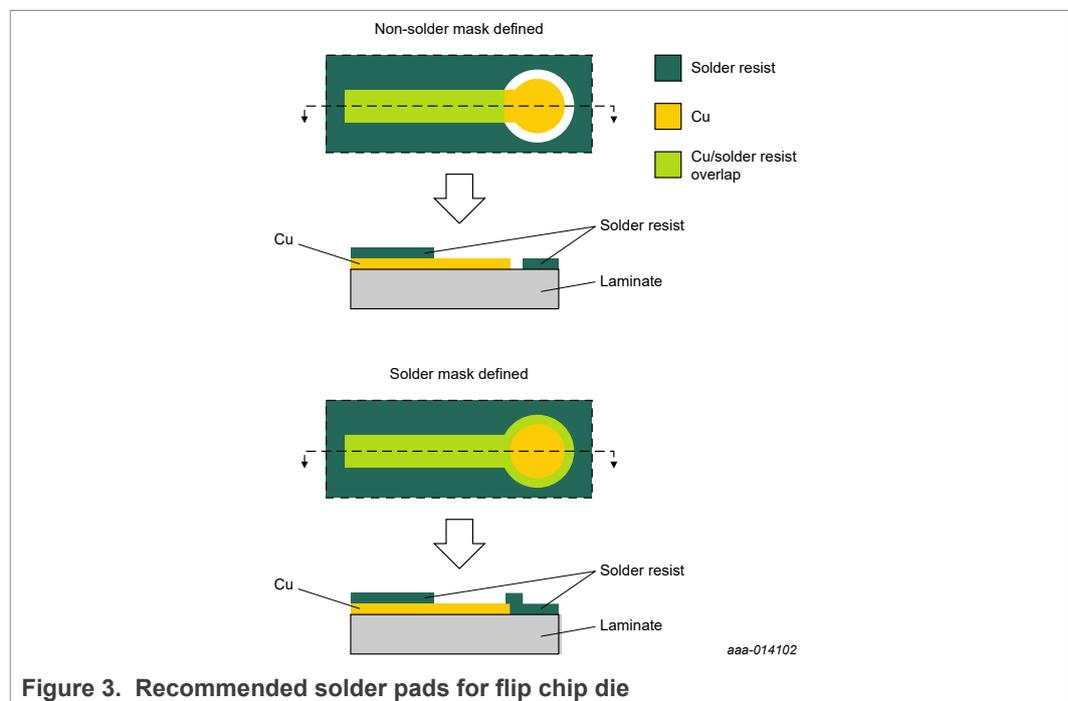


Figure 3. Recommended solder pads for flip chip die

Table 1. Interposer solder pad dimensions. Cu pad shape and solder resist opening shape must be circular. BD = Bump Diameter, as shown in the Product data sheet.

Bump type	Bump pitch	Pad type	Cu solder pad (tolerance)	Solder resists opening (tolerance)
Plated solder bump	$\geq 300 \mu\text{m}$	NSMD	$130 \mu\text{m} (\pm 15 \mu\text{m})$	$170 \mu\text{m} (\pm 15 \mu\text{m})$
Plated solder bump	$190 \mu\text{m} \leq \text{pitch} < 300 \mu\text{m}$	SMD	$\text{BD} + 40 \mu\text{m} (\pm 15 \mu\text{m})$	$\text{BD} - 10 \mu\text{m} (\pm 10 \mu\text{m})$
Copper pillar bump	$\geq 150 \mu\text{m}$	SMD	$\text{BD} + 35 \mu\text{m} (\pm 15 \mu\text{m})$	$\text{BD} + 10 \mu\text{m} (\pm 10 \mu\text{m})$

It is recommended that the whole internal area of the pad to be flat. The use of vias under the bumps should be avoided wherever possible, as non-flat surfaces can create voids in the solder joint and affect the reliability. If via-in-pad structures (micro-via) are employed, filled micro-vias are preferred.

For NSMD pads, the maximum advisable trace width is $75 \mu\text{m}$. Reducing copper (Cu) thickness of the top layer of the PCB is recommended to improve tolerances.

3.2 Interposer surface finish

For internal qualification, Cu-pad finishes on the board used are Cu-OSP (Organic Solderability Preservatives (OSP)) and NiAu (Electroless Nickel Immersion Gold (ENIG)). These finishes ensure good reliability of the end product.

3.3 Clearances/location

For a typical advanced interposer used in modules, clearance around the maximum size of the flip chip die should be considered. This clearance is to ensure pick and place accuracy of the flip chip die, taking into account the surrounding components.

When underfill is applied, sufficient space should be available for dispensing. As with all other surface-mounted components, the placing of the flip chip die near mounting holes, connectors, clamps, and so on, is not recommended. Usually during module/package assembly, multiple interposers are part of a larger panel. The separation of this panel in single interposers can result in mechanical stress to components that are mounted near the separation lanes. The amount of clearance from the separation lane depends on the separation process.

4 Assembly

4.1 Stencil printing of solder paste

Table 2 gives an overview of the recommended stencil dimensions for flip chips dies. For bump pitches below 300 µm, flux dipping or dispensing is advised instead of solder paste printing.

Table 2. Recommended stencil dimensions

Bump pitch	Stencil		
	Thickness	Shape	Opening
≥ 300 µm	80 µm	circular	200 µm

An electroformed stencil can be used. Before using the stencil, the dimensional accuracy should be checked.

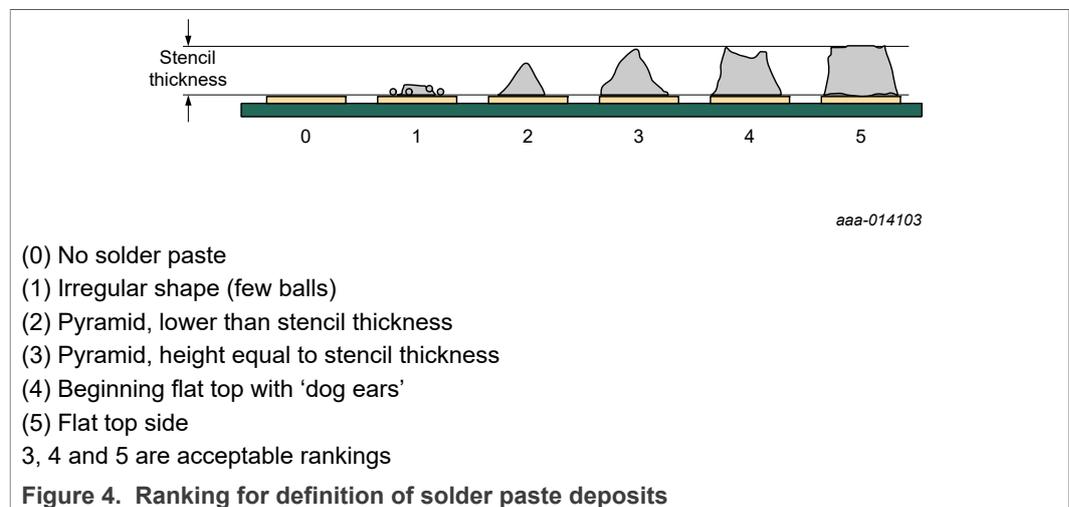
Guideline for stencil opening dimensions:

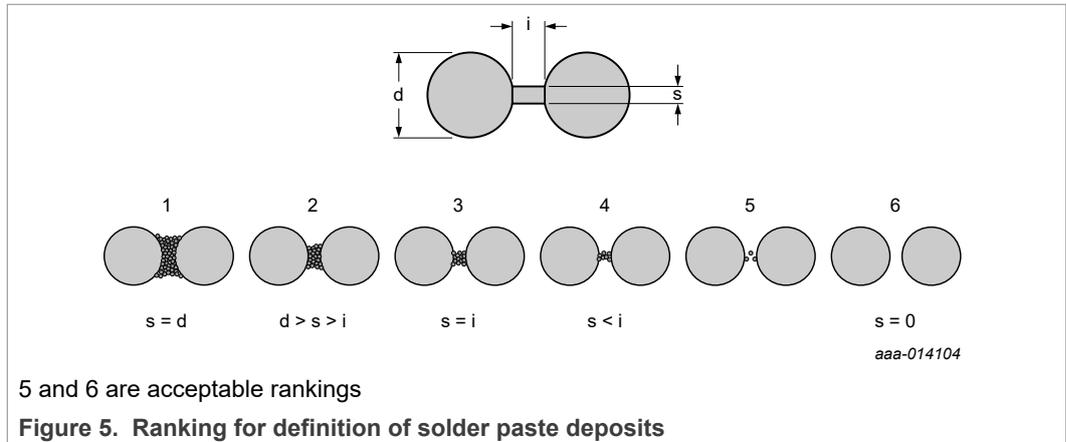
- Top (print) side: design value +0/-20 µm
- Substrate side: design value ± 12 µm

It is advised that a lead-free SAC solder paste is used. Type 5 solder particles or smaller should be used for best print definition. The storage and use conditions should be followed as specified by the solder paste supplier. A solder ball test can be used to verify the reflow properties of the solder paste (IPC-TM-650, Solder Ball Test; see Ref. [2]). Before applying the paste on the stencil, it should be at room temperature and thoroughly mixed.

Adjust print speed and pressure so that the stencil is wiped clean of paste, and the solder paste rolls smoothly in front of the squeegee. If needed, the bottom side of the stencil can be cleaned regularly to avoid smearing. Criteria for print definition and smearing are given in Figure 4 and Figure 5.

The print result depends on the rheology of the solder paste, the dimensions of the stencil opening, the print parameters, and the solder land definition on the interposer. A larger aperture gives a better definition, but worse smearing.





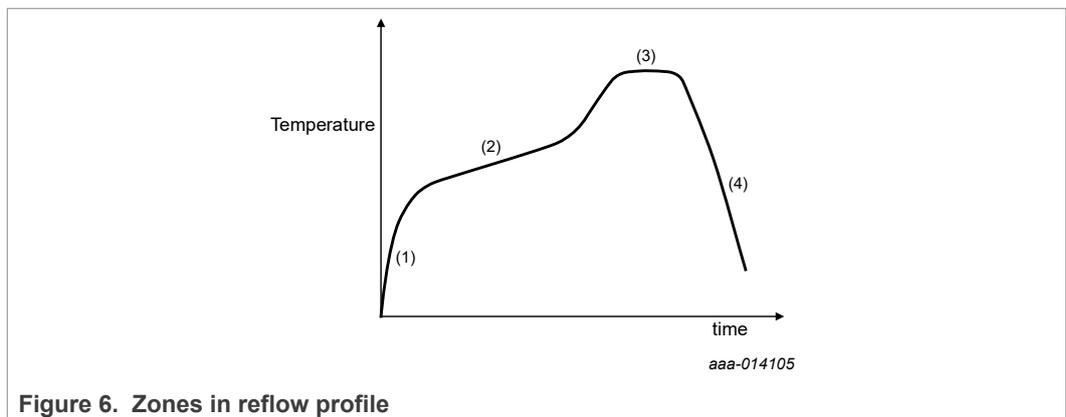
The flux should provide sufficient thickness to keep the flip chip die in place during reflow. Flux is either applied onto the interposer (dispensing, printing), or the flip chip die (dipping). The rheology of the flux is optimized for the particular application method. Flux can be applied onto the complete flip chip die area or in individual dots per bump.

The maximum advised component displacement is 30 % of metal pad diameter. As an alignment method, use local fiducials and a vision system.

4.2 Reflow

A general reflow profile consists of four steps (see [Figure 6](#)):

1. Heating zone: fast heating to reach a certain minimum temperature across the whole board
2. Equalization zone: equalization of the temperatures across the board up to a certain temperature range to avoid large temperature differences in the reflow zone; depending on the component mix
3. Reflow zone: zone in which the actual soldering is done
4. Cooling zone: ramp down zone



Follow the recommendations of the solder paste or flux supplier on the optimum shape of the reflow curve, taking into account the mix of components on the board. At the same time, the profile should not be more stringent than the JEDEC profile requirements for MSL assessment (see Ref. [\[3\]](#)). For good wetting, typical minimum temperature in the peak zone is 235 ° C for SAC or SnAg1.8 solder.

Proper board support during all steps of the reflow profile is essential to avoid board sagging resulting in stress on the soldered joints.

4.3 Underfill

Underfill can improve the protection and reliability of the flip chip die. The underfill material bridges the CTE mismatch between flip chip die and interposer and improves the protection of the flip chip die against moisture and contamination. Especially for larger flip chip dies, underfill can improve the board level reliability behavior.

Two main underfill types can be distinguished:

- Conventional underfill: fills the gap between the flip chip die and the interposer
- Molded underfill: encapsulates the complete flip chip die; fills the gap between the flip chip die and the interposer, and protects the side walls and back side.

The underfill type is application-dependent. It is recommended to follow the use conditions as defined by the supplier. A board level reliability evaluation can help in the underfill selection. A careful assessment is advised to assess the influence of the underfill material on the electrical performance and the potential impact of the halogen content in the underfill material on the biased (humidity) reliability performance in the end application.

The underfill storage, processing and curing conditions as defined by the supplier should be followed.

5 Rework process

Flip chip dies can be reworked only when reworkable underfill is used. Molded underfill samples cannot be reworked.

A BGA rework system can be used for rework. Manual handling of flip chip dies should be limited to the absolute minimum. If necessary, a vacuum pick-up tool should be used. Since the rework process damages the bumps, removed flip chip dies cannot be reused.

Rework consists of the following steps:

- Device removal
- Site preparation
- Application of solder paste to the site (if applicable)
- Device placement
- Device attachment

Refer to the 'Repair' section in *Application note AN10439* Ref. [1] for information on board cleaning and site preparation.

6 Returning flip chip dies to NXP

If flip chip dies are sent to NXP for analysis, the whole module or package should be returned. Removing the flip chip die from the interposer damages the bumps and most probably also the device. If the whole module or package cannot be sent to NXP, cut out a part around the device as large as possible by sawing.

During sawing the interposer, clamps should not be placed on top of the flip chip die. Clamping too tightly should be avoided, because it can cause the interposer to warp and damage the device.

The best packing medium for shipment of devices on interposers is gel pack. If the interposer is too large for a gel pack, place the interposer between two ElectroStatic Discharge (ESD) hard foam materials, securing with tape along all edges. Demounted flip chip dies are best packed in gel pack. Both flip chip dies on interposers, and demounted flip chip dies should be packed in ESD-bags and preferably in dry pack for shipping.

7 Reliability

NXP has carried out extensive testing of flip chip dies to provide the optimum manufacturing conditions for assembly and to ensure the necessary quality and reliability over the life time of the product.

During the qualification, reliability tests are performed on wafer level, standalone device level and on board level to ensure the quality level. Product-related reliability data are included in the product qualification report.

When a flip chip die is a particular design for a specific customer, or application (for example, thermo-compression bonding and/or interposer type, such as flex foil or ceramic), NXP does not perform board level reliability tests.

8 Moisture sensitivity level

The default Moisture Sensitivity Level (MSL) for flip chip dies is 1.

9 Storage conditions

The label on the packing specifies the shelf life and floor life conditions.

After expiration date, or when the humidity indicator shows > 10 %, solderability should be checked. See Ref. [5] J-STD-002D, solderability tests for component leads, terminations, lugs, terminals, and wires.

Baking is not allowed for flip chip dies.

10 References

- [1] **AN10439** - Wafer Level Chip Size Package, application note
- [2] **IPC-TM-650** - solder ball test
- [3] **J-STD-020D** - moisture/reflow sensitivity classification for nonhermetic Solid-State surface mount devices
- [4] **J-STD-033** - standard for handling, packing, shipping, and use of moisture/reflow sensitive surface mount devices
- [5] **J-STD-002D** - solderability tests for component leads, terminations, lugs, terminals, and wires

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Contents

1	Introduction	3
2	Package description	3
3	Interposer design guidelines	5
3.1	Footprint layout	5
3.2	Interposer surface finish	6
3.3	Clearances/location	6
4	Assembly	7
4.1	Stencil printing of solder paste	7
4.2	Reflow	8
4.3	Underfill	9
5	Rework process	10
6	Returning flip chip dies to NXP	10
7	Reliability	10
8	Moisture sensitivity level	10
9	Storage conditions	11
10	References	11
11	Legal information	12

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