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LPC11U6x vs. LPC11U3x feature comparison

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Document information

Info	Content
Keywords	LPC11U67JBD48 LPC11U68JBD64 LPC11U68JBD100 LPC11U6x
Abstract	This application note will illustrate the new features of the LPC11U6x device family compared to the LPC11U3x device family.

Revision history

Rev	Date	Description
1	20140311	Initial version.

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1. Introduction

The LPC11Uxx are an ARM Cortex-M0/M0+ based[1], low-cost 32-bit MCU family, designed for 8/16-bit microcontroller applications, offering performance, low power, simple instruction set and memory addressing together with reduced code size compared to existing 8/16-bit architectures.

The LPC11U3x and LPC11U6x are two series in the LPC11Uxx family that stand out due to their feature set, with the LPC11U6x being the latest series.

An important feature common to both the series is that they are equipped with highly flexible and configurable Full Speed USB 2.0 device controllers.

The LPC11U6x has some new features compared to the LPC11U3x; the details of the new features are described in the following sections:

- Processor (M0+, MTB)
- Memory size
- Operating temperature range
- Package and pin out (GPIO, Glitch free pads, XTAL w/GPIO, RSTOUT)
- I2C interface
- MinUART (wake up feature)
- USB (circuit design notice, Low-speed mode)
- 12-bit A/D converter
- State Configurable Timers (SCT)
- DMA controller
- Real-Time Clock (RTC)
- On-chip temperature sensor
- Cyclic Redundancy Check (CRC) engine

2. Processor (M0+, MTB)

The LPC11U3x is integrated with an ARM Cortex-M0 processor, whereas the LPC11U6x is integrated with an ARM Cortex-M0+ processor with the addition of the following features:

- Two-stage pipeline
- Single-cycle multiplier
- Fast single-cycle I/O port
- External debug request input is supported from MTB (Micro Trace Buffer)

3. Memory size

The LPC11U3x supports up to 128 kB of on-chip flash program memory and up to 12 kB of SRAM data memory.

The LPC11U6x supports up to 256 kB of on-chip flash program memory, up to 32 kB of SRAM data memory (SRAM0) with two additional SRAM blocks of 2 kB each (SRAM1, USB SRAM).

1. LPC11U1X/2X/3X M0-based, LPC11U6X M0+ based.

4. Operating temperature range

The operating temperature range of LPC11U3x is –40 °C to +85 °C.

The operating temperature range of LPC11U6x is –40 °C to +105 °C.

5. Package and pin out (GPIO, glitch-free pads, XTAL w/GPIO, RSTOUT)

5.1 LPC11U3x

The LPC11U3x is available in LQFP64, LQFP48, TFBGA48, and HVQFN33 packages and has up to 54 General Purpose I/O (GPIO) pins.

Select pins (pins PIO0_22, PIO0_23, and PIO0_11 to PIO0_16) provide the option of turning on or off a 10 ns input glitch filter. The glitch filter is turned on by default. The RESET pin has a 20 ns glitch filter (not configurable).

XTALIN and XTALOUT are provided with dedicated pins. If an external crystal is not used, these two pins cannot be used as GPIOs.

5.2 LPC11U6x

The LPC11U6x is available in LQFP48, LQFP64, and LQFP100 packages and has up to 80 General-Purpose I/O (GPIO) pins.

All GPIO pins are equipped with a programmable digital glitch filter.

XTALIN pin is shared with GPIO PIO2_0 and XTALOUT pin is shared with GPIO PIO2_1.

An RSTOUT pin is added to indicate the internal reset status.

6. I2C interface

The LPC11U3x contains one I2C interface.

LPC11U6x contains two I2C interfaces.

- I2C0 is the same as LPC11U3x and supports fast mode plus with bit rates up 1Mbits/s.
- I2C1 uses standard digital pins. The I2C1 interface supports fast mode with bit rates up to 400 Kbits/s.

7. MinUART (wake up feature)

The LPC11U3x contains one USART.

The LPC11U6x contains five USARTs.

USART0 is the same as LPC11U3x.

USART1 to USART4 are MinUART which use a different register interface to achieve the same UART functionality as UART0 except for modem and smart card control.

USART3 and USART4 are available only on part LPC11U68JBD100.

Interrupts generated by the USART1/2/3/4 peripherals can wake up the processor from Deep-sleep and power-down modes if the USART is in synchronous mode or the 32 kHz mode is enabled or the CTS interrupt is enabled. This wake-up mechanism is not available with USART0.

8. USB (circuit design notice, Low-speed mode)

Compared to the LPC11U3x, the LPC11U6x USB controller has some new features:

- Software can control the USB_CONNECT signal by setting the DCON bit in the DEVCMDSTAT register. There is no need to have a dedicated USB_CONNECT pin on the chip.
- Supports SoftConnect through internal 1.5 kΩ pull-up resistor between USB_DP and VDD.
- USB pads include internal SoftConnect and 33 Ω series termination resistor for USB_DP and USB_DM signal lines.
- Support for XTAL-less low-speed USB (1.5 Mbit/s)
- USB-IF Full/Low Speed Certified MCU with USB drivers in ROM.

8.1 USB interface circuit design reference

Typically, the LPC11U3x USB circuit (self-powered for example) can be designed as:

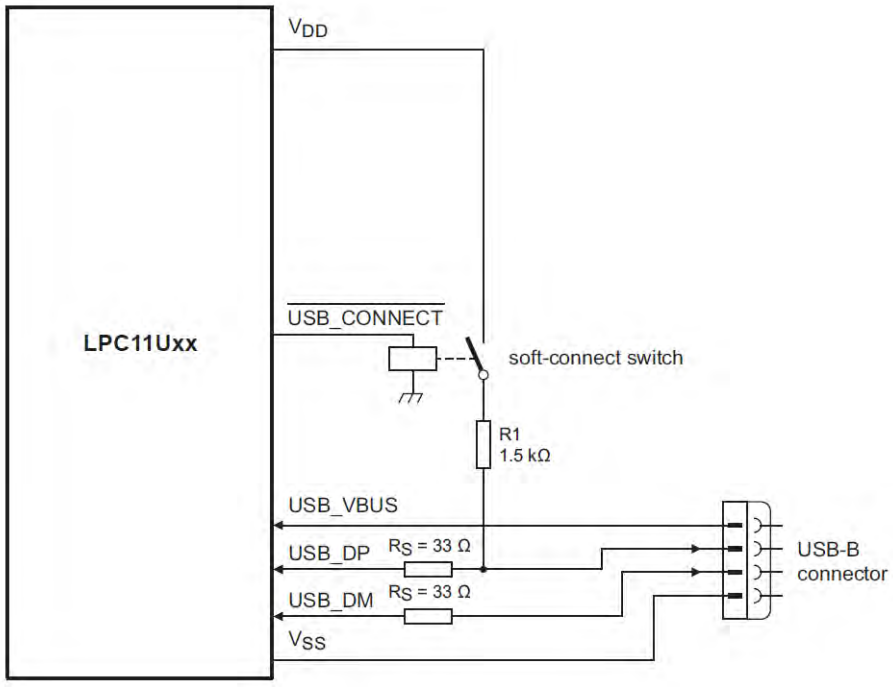

Fig 1. USB interface on a self-powered device (for 11U3x)

The LPC11U6x USB circuit design is changed to Fig 2 for self-powered device and Fig 3 for bus-powered device:

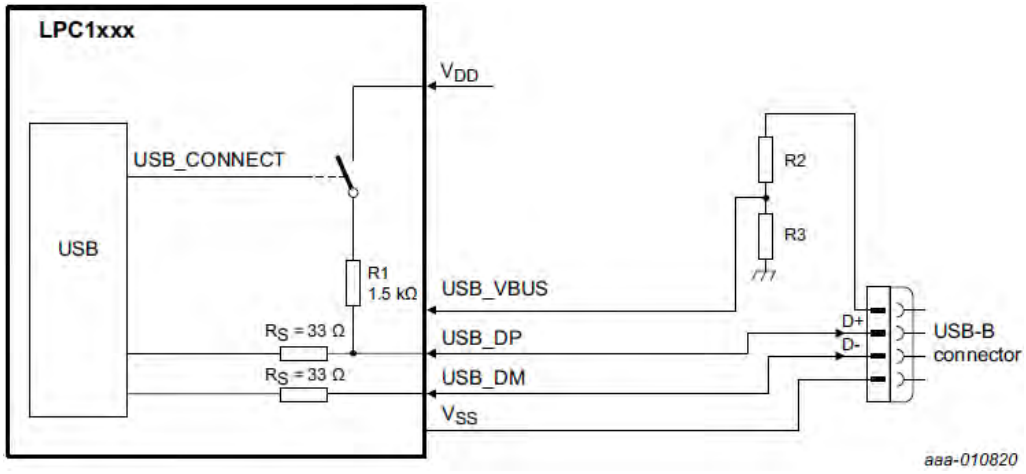

Fig 2. USB interface on a self-powered device where USB_VBUS = 5 V

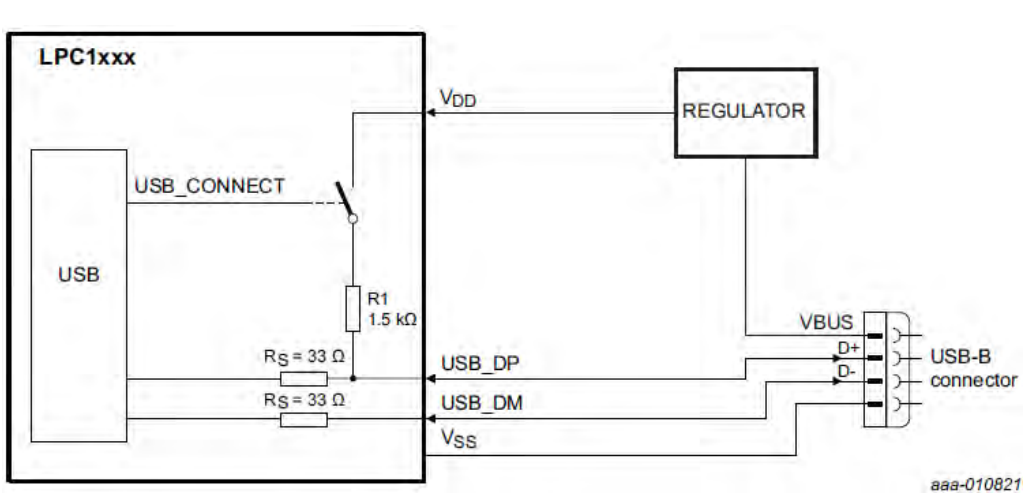

Fig 3. USB interface on a bus-powered device

As the 33 Ω termination resistor and the 1.5k Ω pull up resistor are integrated on the chip, user does not need to provide external termination resistor and 1.5k Ω pull up resistor. This reduces BOM and hardware cost.

For more details on the LPC11U6x USB interface design, refer to chapter 14.2 - “Suggested USB interface solutions” on the LPC11U6x datasheet.

8.2 USB low-speed operation

The USB device controller can be used in low-speed mode supporting 1.5 Mbit/s data exchange with a USB host controller.

To operate in low-speed mode, change the board connections as follows:

- Connect USB_DP to the D– pin of the connector
- Connect USB_DM to the D+ pin of the connector

Use the IRC as clock source for the USB PLL to generate 48 MHz, then set the USB clock divider USBCLKDIV to 8 for a 6 MHz USB clock.

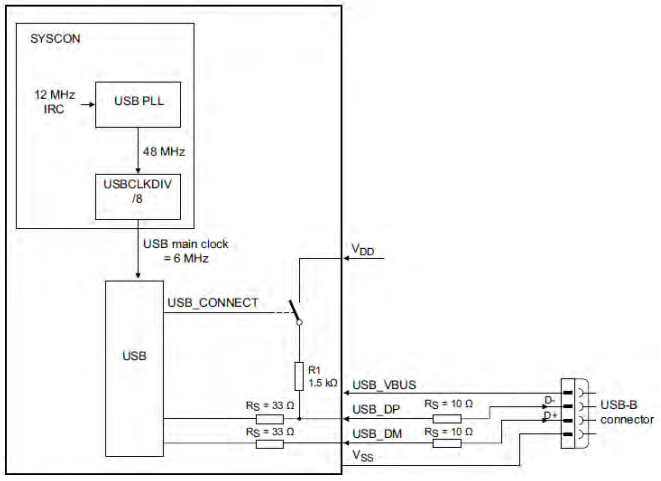

Fig 4. USB interface for low-speed, XTAL-less operation

External 10 Ω resistors are recommended in low-speed mode to reduce overshoot and accommodate for 5 m cable length required for USB-IF testing.

For design details on USB Low-speed operation, refer to chapter 14.2.1 -“USB Low-speed operation” on the LPC11U6x datasheet.

9. 12-bit A/D converter

The LPC11U3x has a 10-bit ADC with a maximum 10-bit conversion rate of 400 kSamples/s. For LPC11U3x ADC, the analog voltage supply and ADC reference voltage shared with VDD.

The LPC11U6x has a 12-bit ADC with a maximum 12-bit conversion rate of 2 MSamples/s (VDD = 2.7 V to 3.6 V) or 1 MSamples/s (VDD = 2.4 V to 2.7 V).

The LPC11U6x ADC uses dedicated pins for Analog voltage supply (VDDA) and ADC reference voltage (VREFP, VREFN).The A/D converter includes a built-in, hardware self-calibration mode. In order to achieve the specified ADC accuracy, the A/D converter must be recalibrated, at a minimum, following every chip reset before initiating normal ADC operation.

10. State Configurable Timers (SCT)

LPC11U6x contains two State Configurable Timers (SCTimer0/PWM and SCTimer1/PWM).

The state configurable timer can create timed output signals such as PWM outputs triggered by programmable events. Combinations of events can be used to define timer states. The SCTimer/PWM can control the timer operations, capture inputs, change states and toggle outputs triggered entirely only by events without CPU intervention.

If multiple states are not implemented, the SCTimer/PWM simply operates as one 32-bit or two 16-bit timers with match, capture and PWM functions.

Each SCTimer/PWM supports: 4 inputs, 4 outputs, 6 events, 8 states and 5 capture/match registers.

LPC11U3x does not contain a State Configurable Timer.

11. DMA controller

LPC11U6x is integrated with a DMA controller.

The DMA controller can access all memories and the USART and SSP peripherals using DMA requests. DMA transfers can also be triggered by internal events like the ADC interrupts, timer match outputs, the pin interrupts (PINT0 and PINT1) and the SCTimer DMA requests.

12. Real-Time Clock (RTC)

LPC11U6x contains a Real-Time Clock (RTC) with 32 kHz oscillator.

The RTC resides in a separate always-on voltage domain with battery back-up. The RTC uses an independent oscillator, also located in the always-on voltage domain.

13. On-chip temperature sensor

LPC11U6x contains an on-chip temperature sensor.

The temperature sensor transducer uses an intrinsic p-n junction diode reference and outputs a CTAT voltage (Complement to Absolute Temperature). The output voltage varies inversely with device temperature with an absolute accuracy of better than 5°C over the full temperature range (–40 °C to +105 °C).

After power-up and after switching the input channels of the ADC, the temperature sensor output must be allowed to settle to its stable value before it can be used as an accurate ADC input.

For an accurate measurement of the temperature sensor by the ADC, the ADC must be configured in single-channel burst mode. The last value of a nine-conversion (or more) burst provides an accurate result.

14. Cyclic Redundancy Check (CRC) engine

A CRC engine is available on the LPC11U6x.

The Cyclic Redundancy Check generator with programmable polynomial settings supports several CRC standards commonly used (CRC-CCITT, CRC-16, and CRC-32).

The LPC11U3x does not have a CRC engine.

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16. List of figures

Fig 1. USB interface on a self-powered device (for 11U3x) 5
Fig 2. USB interface on a self-powered device where USB_VBUS = 5 V 6
Fig 3. USB interface on a bus-powered device 6
Fig 4. USB interface for low-speed, XTAL-less operation 7

17. Contents

1. Introduction 3
2. Processor (M0+, MTB) 3
3. Memory size 3
4. Operating temperature range 4
5. Package and pin out (GPIO, glitch-free pads, XTAL w/GPIO, RSTOUT) 4
5.1 LPC11U3x 4
5.2 LPC11U6x 4
6. I2C interface 4
7. MinUART (wake up feature) 4
8. USB (circuit design notice, Low-speed mode) . 5
8.1 USB interface circuit design reference 5
8.2 USB low-speed operation 7
9. 12-bit A/D converter 7
10. State Configurable Timers (SCT) 8
11. DMA controller 8
12. Real-Time Clock (RTC) 8
13. On-chip temperature sensor 8
14. Cyclic Redundancy Check (CRC) engine 8
15. Legal information 9
15.1 Definitions 9
15.2 Disclaimers 9
15.3 Trademarks 9
16. List of figures 10
17. Contents 11

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