AN11415

PTN3355 PCB Layout Guideline, Reference Schematics and BOM

Rev. 1 — 16 December 2014 Application note

Document information

Info	Content
Keywords	DisplayPort, PTN3355
Abstract	This document provides a practical guideline to PTN3355 application design and layout.

Revision history

Rev	Date	Description
1	20141216	Initial version

Contact information

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1. Introduction

This document provides a guideline for PTN3355 application and layout guide line in ULT notebook, docking station and dongle designs.

PTN3355 is low power DisplayPort to VGA bridge IC with integrated 1-2 VGA switch. PTN3355 is in an HVQFN40 package, 6 mm x 6 mm, with 0.5 mm pitch. PTN3355 consumes approximately 200 mW of power for video streaming in WUXGA resolution and 890 uW of power in low-power mode. The VGA output is powered down when there is no valid DisplayPort source data being transmitted. PTN3355 is suitable for Ultra Low Power Notebook and other low power devices. PTN3355 also offers second VGA port for docking design.

PTN3355 is powered from a 3.3 V power supply, and generated 1.5 V through an internal step-down switch regulator and buck converter for internal core usage and DAC usage.

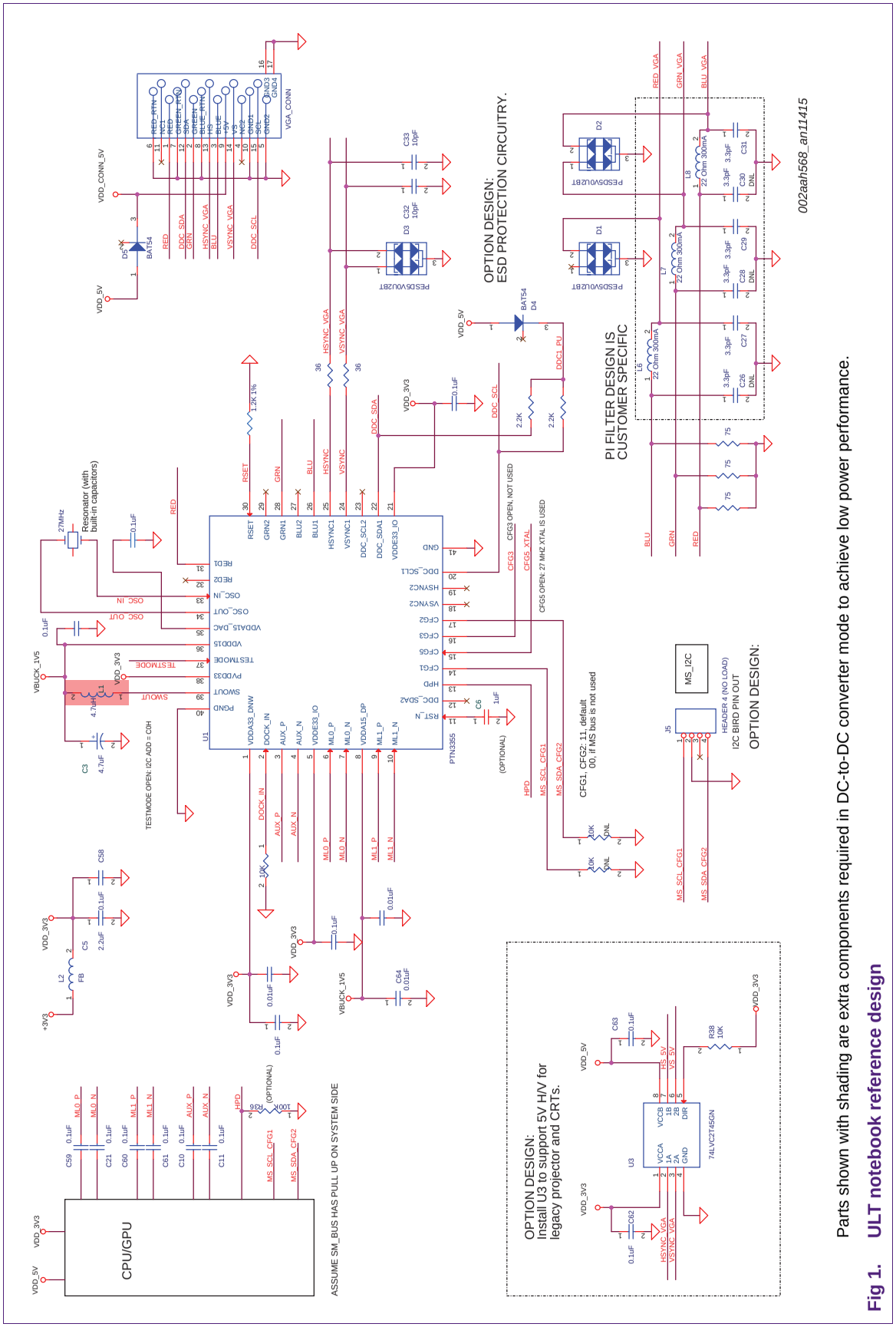
2. Reference designs

2.1 ULT notebook design

PTN3355 can be connected directly to the DP lanes on mother board, or on docking station.

Connect PTN3355 to one of the DP ports on PCH/GPU with 0.1uF AC caps in series for DP data lanes and AUX lanes. PTN3355 probably will be used as a primary display; make sure the BIOS is set accordingly.

Below is a reference design for one VGA application.



Parts shown with shading are extra components required in DC-to-DC converter mode to achieve low power performance.

Fig 1. ULT notebook reference design

2.2 Dongle design

PTN3355 can also be used on DP-VGA dongles.

Connect PTN3355 DPVGA to one of the DP ports on the system board.

DPVGA dongle gets 3V3 power from DP connector for PTN3355 IC operation, then boost up to 5 V for VGA connector.

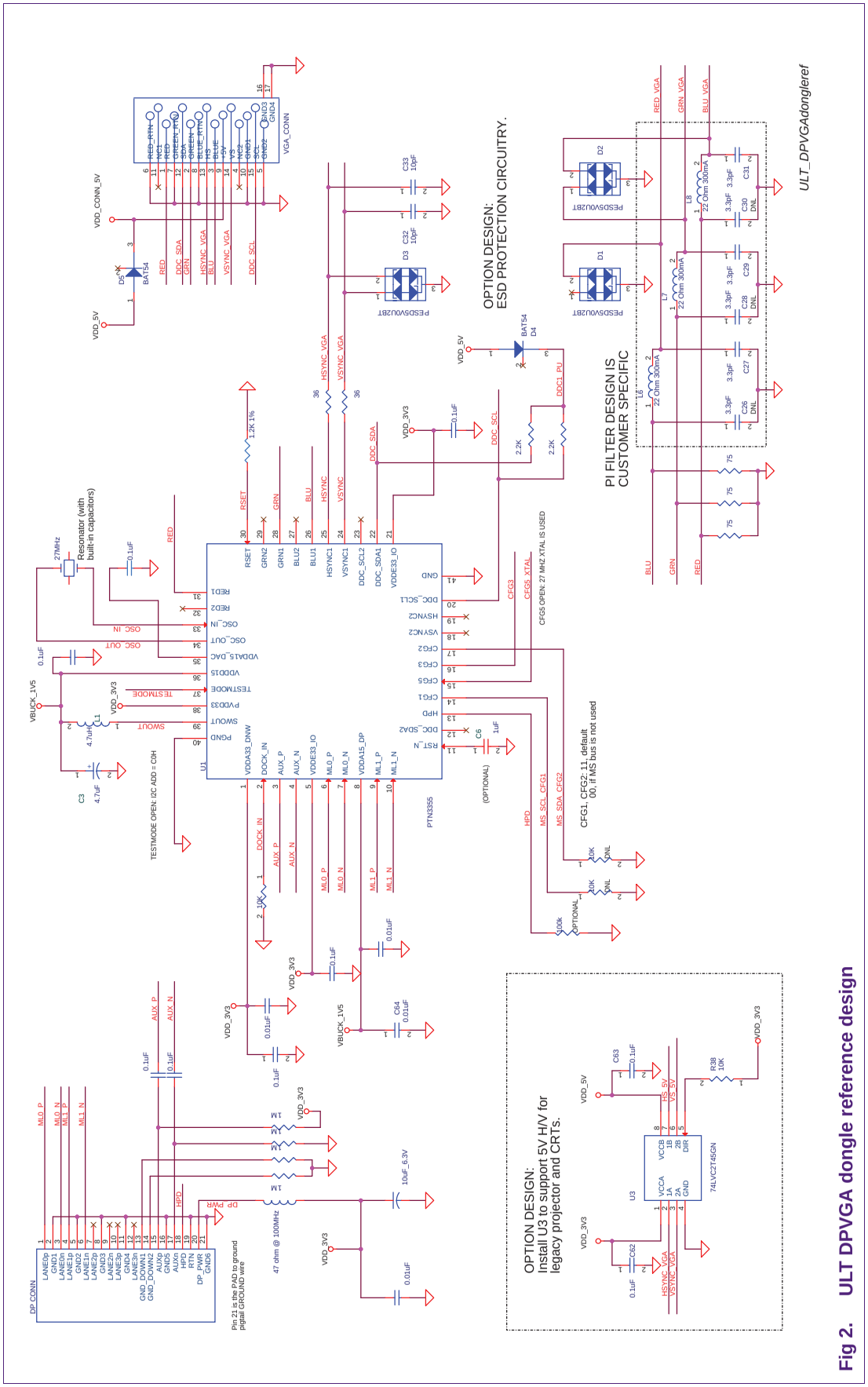


Fig 2. ULT DPVGA dongle reference design

2.3 Minimum BOM design

For cost conscious application, PTN3355 needs only a handful of components to function.

Below is a minimum BOM design for embedded or dongle design.

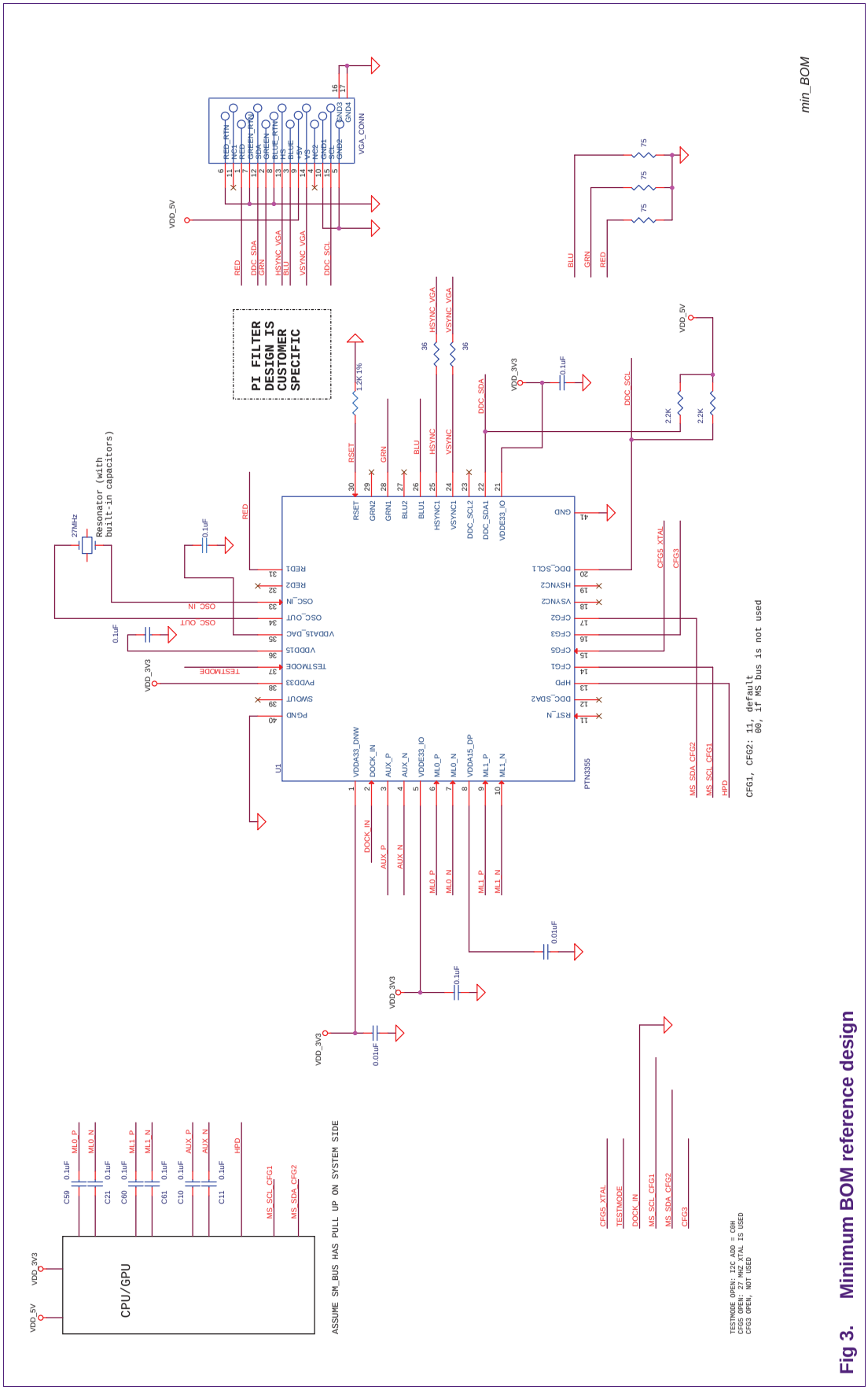


Fig 3. Minimum BOM reference design

3. Buck converter

3.1 Buck converter layout guideline

PTN3355 utilizes a switch mode power supply to deliver the power needed with high efficiency. Switch mode power supplies require careful attention to the PC board layout.

There are two switching high-current loops formed by the switching action of the buck converter. One loop is formed by the current that flows from the input capacitor through the PVDD pin of the part, through the internal PMOS High-side switch, out the SW pin, through the inductor and the load capacitor to the analog ground, and through the ground plane back to the ground connection of the input capacitor. A second switching high current loop is formed when the low-side NMOS switch is on. The current flows from the PGND pin of the part through the internal NMOS switch, out the SW pin, through the inductor and the load capacitor, to the analog ground, and through the ground plane back to the PGND pin of the part.

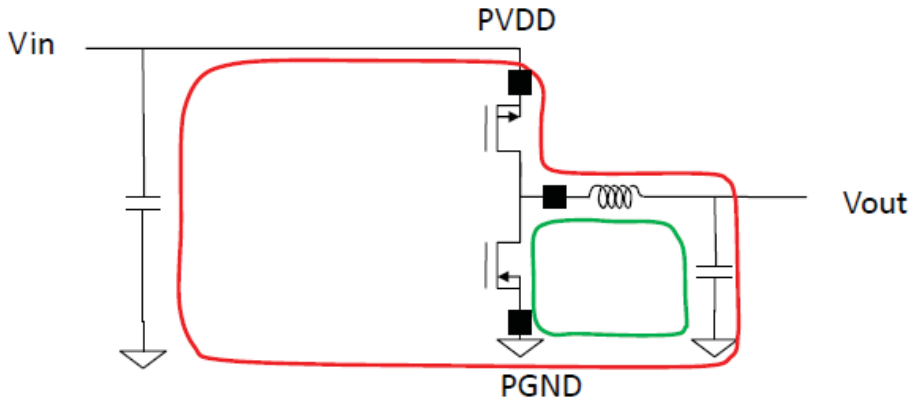


Fig 4. Switching High-current Loop1: PVDD - LC - PMOS -- GND

To minimize electromagnetic interference (EMI), it is essential to minimize the length and area of the switching high current loops. It is also critical that the two switching current paths are matched as closely as possible.

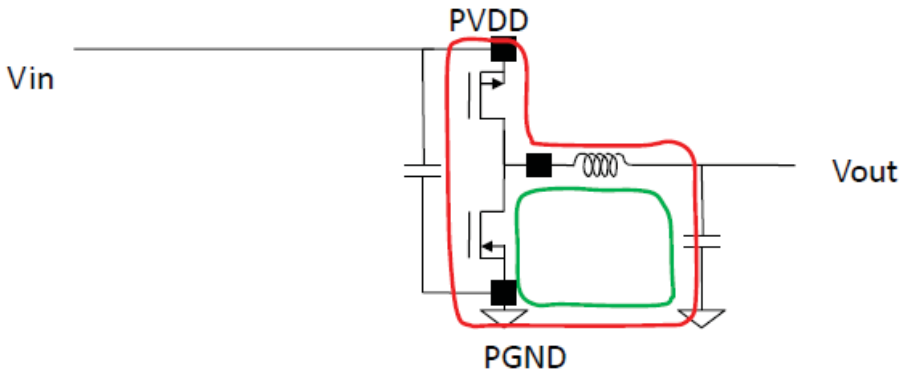


Fig 5. Switching high-current loop2 : PGND - NMOS - SW - LC - GND

Here are some guidelines for PC board design:

- Connect the exposed paddle of the IC to the PC board ground plane.
- Place the input capacitor as close to the PVDD pin as possible.
- Place the inductor and the load capacitor as close to the SW pin as possible.
- Keep the traces for the input capacitor, inductor and the output capacitor, short, direct and wide.
- Do not connect the PGND pin directly to the ground plane, instead, connect the PGND pin and the input capacitor's ground pin to the ground plane at the same point.
- Minimize the distance between the input capacitor's ground and the ground of the load capacitor.
- Keep the trace for the FB (Vout to VDD1V5) away from the switching high current paths.

The following is a proposed PC board layout scheme for the PTN3355 which minimizes the area of the two switching current loops and matches the current flow paths for the two loops as closely as possible.

Note the smaller capacitors are 0.1 uF caps that must be place as close to the pin as possible.

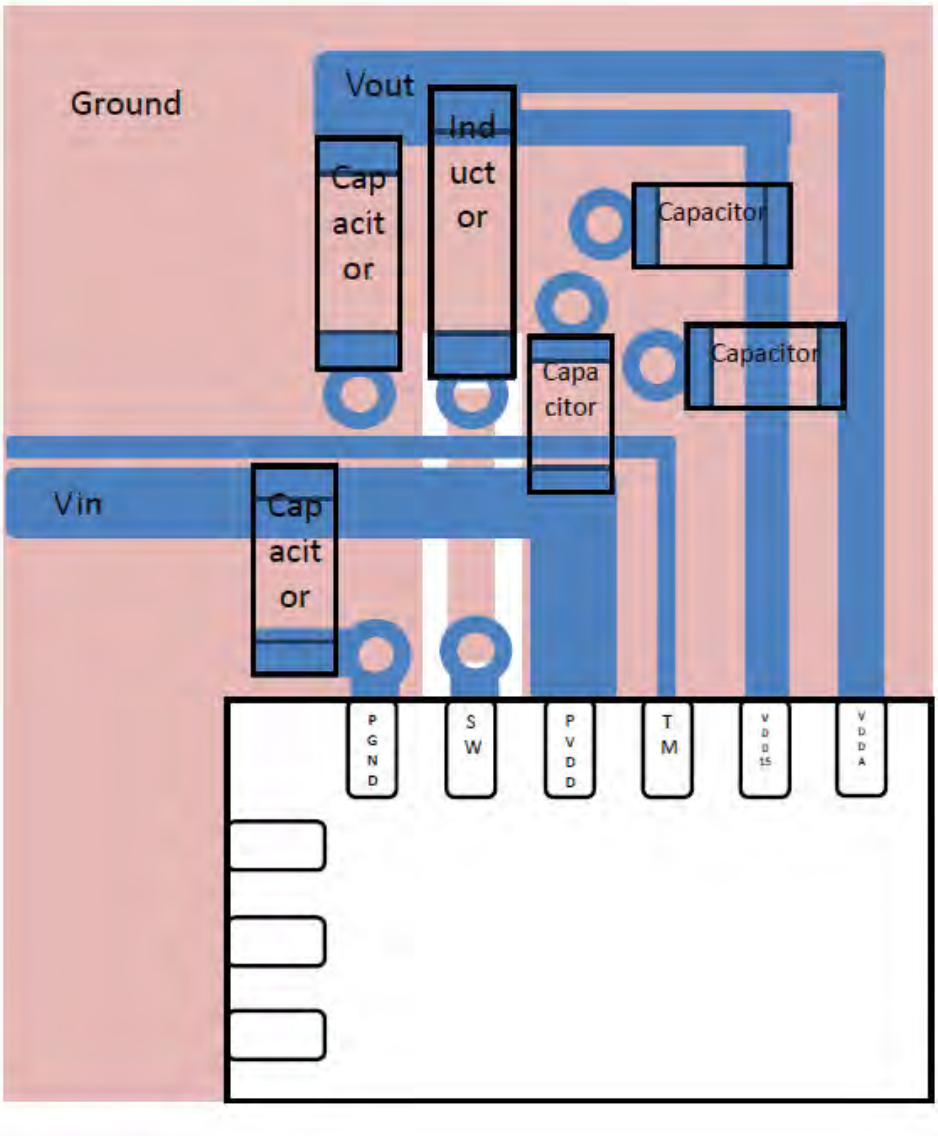


Fig 6. Buck converter component placement

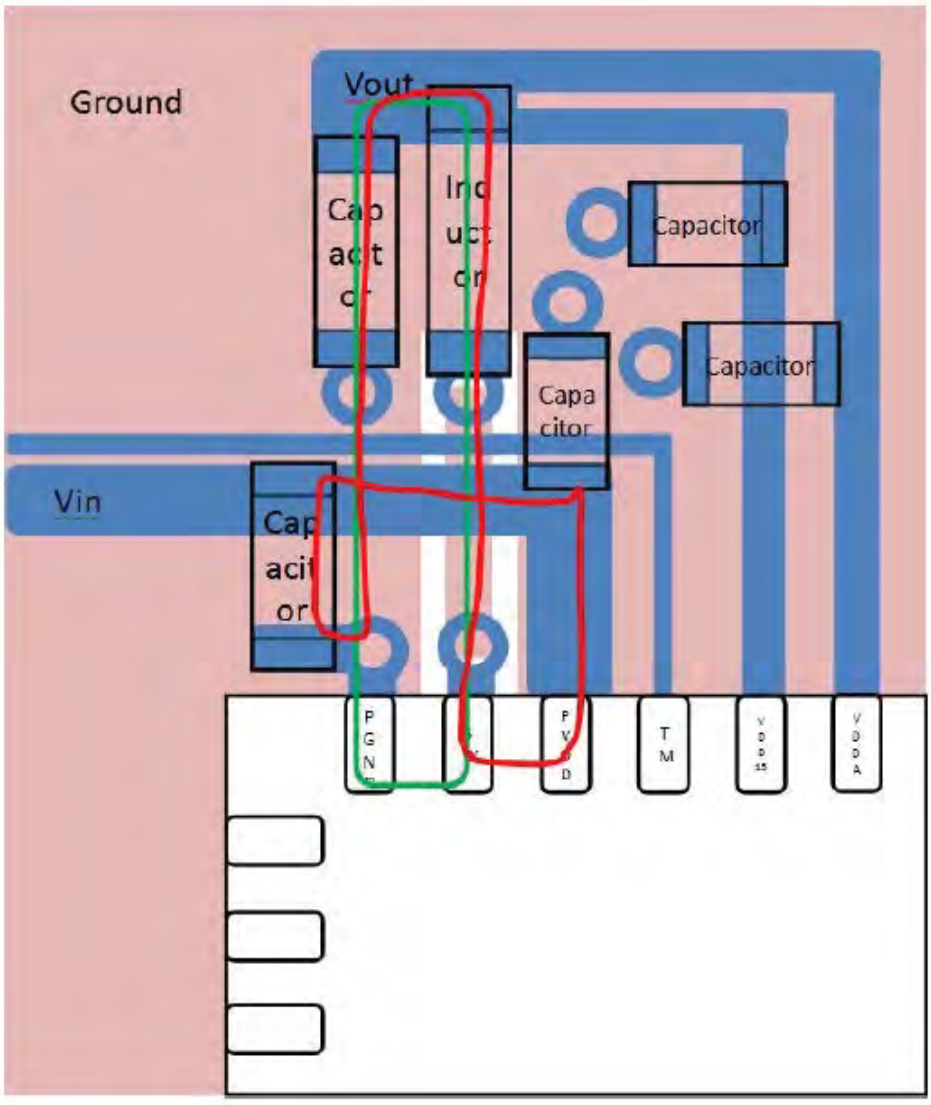


Fig 7. Buck converter switching current loops

3.2 Buck converter schematic

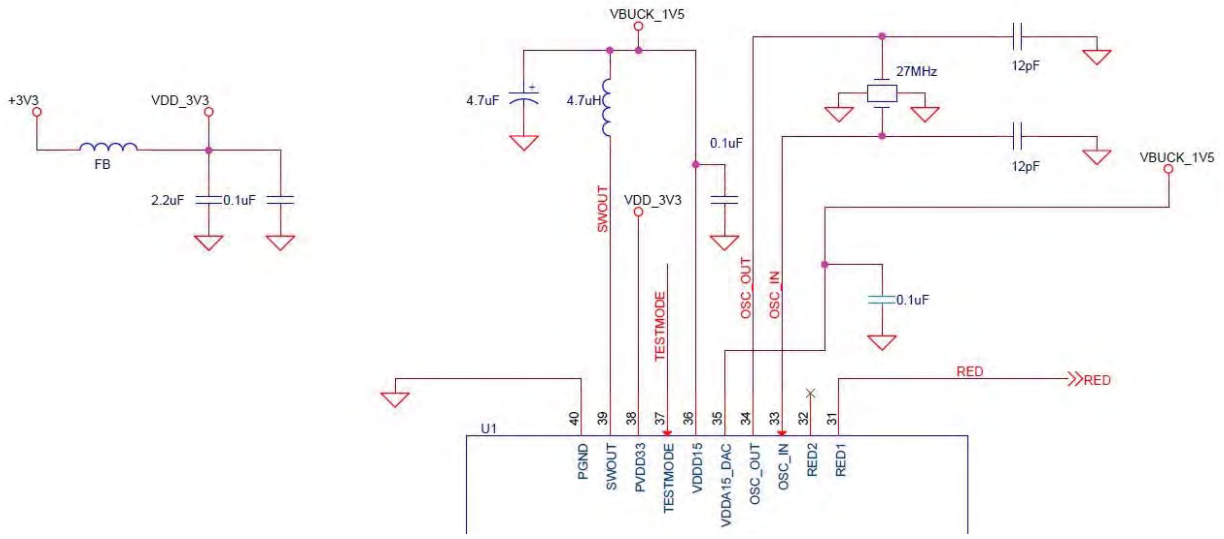


Fig 8. Buck converter schematics

4. DP receiver interface

Main differential pairs and AUX channel are routed with 100 Ohm impedance. The important parameters to calculate the impedance are:.

- PCB thickness
- Distance to ground plane
- Trace width
- Trace spacing
- PCB permittivity

Guard grounds are used to isolate the pair. This helps to eliminate cross talk between traces. Trace lengths are matched on the same pair to 0.01”. Inter pair match to 1”.

AC caps for DP lanes and AUX pair should be placed close to the DP interface.

When signals change plane, the ground plane need to move along to keep constant trace impedance. On DPVGA a ground island is inserted on the VCC plane for this purpose.

5. VGA interface

Table 1. Design guidelines for VGA connector, PWB to cable junction

Design guideline number	Design guideline description	Approximate impact on EMI decrease
1	Define the 2nd PWB layer as ground plane	
2	Connect the ground chassis pins of the VGA PWB-connector	25 dB
3	Use an upper ground plane around VGA connector pins. This design guideline makes no sense when it is not combined with design guideline 4.	
4	Use enough vias to connect the upper ground plane with main ground plane in 2nd PWB layer. Enough means around every 3 mm (stitching)	20 dB
5	Ensure proper connection between PWB-connector chassis and upper ground plane by using contact springs (at least 3 contact points). Emission improvement when either 1 or 3 contacts were used was 10 dB!	10 dB
6	Apply ferrite bead around VGA cable (is already very common for typical cables available from the market)	3 dB

Following the recommended guidelines, all RGB traces on DPVGA board are routed with 75 Ohm impedance from PTN3355 to VGA connector. Ground fills are used to isolate these traces. Ground fills are connected to ground plane with vias.

6. PCB stack up

4-layer FR4 PCB is sufficient for PTN3355 DP-VGA layout. Suggested layers:

1. Signal layer 1 for DPs, with ground cover the entire buck converter area plus power islands or thick traces for Vin and Vout for buck converter.
2. Ground layer
3. Power layer with VDD_3V3 island to cover entire PTN3355, except pin 39, 36, 35 and pin 8.
4. Signal layer 2

Table 2. PCB stack up

PCB stack up		**Impedance**			
Thickness (mil)					
Solder mask	**0.50 mils**	**Single**		**Diff**	
copper + plating	0.70 mils	9.45 mils, 50Ω ± 10 % 3.55 mils, 75Ω ± 10 %	53.09Ω	5.9/5.5/5.9 mils, 100Ω ± 10 %	101.26Ω
Prepreg	4.70 mils				
copper	1.40 mils				
core	47.20 mils				
copper	1.40 mils				
Prepreg	4.70 mils				
copper + plating	0.70 mils	9.45 mils, 50Ω ± 10 % 3.55 mils, 75Ω ± 10 %	53.09Ω	5.9/5.5/5.9 mils, 100Ω ± 10 %	101.26Ω
Solder mask	0.50 mils				
TOTAL	61.80 mils				
	1.57 mm				

7. PTN3355 on notebook BOM

PTN3355 DPVGA Reference Design Revised: Tuesday, September 24, 2013

Revision: 0.13

NXP Semiconductors

Bill Of Materials September 24,2013 17:30:29

Item	QTY	Reference	Value	PCB Footprint	Feature	Manufacturer	Manufacturer Number	Vendor N.	Load Option
1	2	C1,C4	12pF	rc0402	CAP CER 12PF 50V 5% NP0 0402	Murata	GRM1555C1H120JZ01D	Digikey, 490-1279-2-ND	LOAD
2	13	C2,C8,C10,C11,C13,C19,C20,C21,C23,C58,C59,C60,C61	0.1uF	rc0201	CAP CER 0.1UF 10V 10% X5R 0201	TDK Corporation	C0603X5R1A104K	Digikey, 445-7318-2-ND	LOAD
3	1	C3	4.7uF	rc1206	CAP CER 4.7UF 16V 10% X7R 1206	TDK	C3216X7R1C475K/1.60	Digikey, 445-1385-2-ND	LOAD
4	1	C5	2.2uF	rc0603	CAP CER 2.2UF 10V 10% X5R 0603	Taiyo Yuden	LMK107BJ225KA-T	Digikey, 587-1253-2-ND	LOAD
6	2	C14,C24	0.01uF	rc0201	CAP CER 10000PF 10V 10% X5R 0201	TDK Corporation	C0603X5R1A103K	Digikey, 445-1793-2-ND	LOAD
8	3	C27,C29,C31	3.3pF	rc0402	CAP CER 3.3PF 50V NP0 0402	Murata	GRM1555C1H3R3CZ01D	Digikey, 490-1270-2-ND	LOAD
9	2	C32,C33	10pF	rc0402	CAP CER 10PF 50V 5% NP0 0402	Yageo	CC0402JRNP09BN100	Digikey, 311-1014-2-ND	LOAD
11	3	D1,D2,D3	PESD5V0U2BT	SOT-23	DIODE ULOW ESD PROTECTION SOT-23	NXP	PESD5V0U2BT,215	Digikey, 568-4296-2-ND	LOAD
12	1	D4	BAT54	SOT23	DIODE SCHOTTKY 30V 200MA SOT23-3	Diode	BAT54TA	Digikey, BAT54TR-ND	LOAD
13	1	D5	BAT54	SOD80C	DIODE SS SWITCH 60V 250MA SOD80	Vishay	BAV100-GS08	Digikey, BAV100-GS08TR-ND	LOAD
14	1	J1	VGA_CONN	DB-15_HD	CONN D-SUB RCPT 15POS HD R/A	EDAC	634-015-274-992	Digikey, 151-1125-ND	LOAD
16	1	L1	4.7uH	rc1210	IND 4.7uH, 1210, 20%	Panasonic	ELJ-PA4R7MF2	Digikey, PCD2336TR-ND	LOAD
17	1	L2	FB	rc1206	FERRITE 3A 100 OHM 1206 SMD	Laird-Signal	HI1206N101R-10	Digikey, 240-2408-2-ND	LOAD
18	3	L6,L7,L8	47nH	rc0402	INDUCTOR 47NH 200MA 0402	Murata	LQG15HS47NJ02D	Digikey, 490-2631-2-ND	LOAD
19	1	R16	1.2K 1%	rc0402	RES 1.20K OHM 1/10W 1% 0402 SMD	Pansonic	ERJ-2RKF1201X	Digikey, P1.20KLTR-ND	LOAD
20	2	R29,R30	36	rc0402	RES 36 OHM 1/16W .5% 0402 SMD	Pansonic	ERA-2AKD360X	Digikey, P36DDTR-ND	LOAD
21	3	R31,R32,R33	75	rc0402	RES 75.0 OHM 1/10W 1% 0402 SMD	Pansonic	ERJ-2RKF75R0X	Digikey, P75.0LTR-ND	LOAD
22	2	R34,R35	1.2K	rc0603	RES 1.2K OHM 1/10W 5% 0603 SMD	Yageo	RC0603JR-071K2L	Digikey, 311-1.2KGRTR-ND	LOAD
25	4	R44,R45,R54,R59	10K	rc0201	RES 10K OHM 1/20W 5% 0201 SMD	Pansonic	ERJ-1GEJ103C	Digikey, P10KAGTR-ND	LOAD
26	1	U1	PTN3355	HVQFN40	IC PTN3355 HVQFN40	NXP	PTN3355BS	NXP_ptn3355BS	LOAD
28	1	Y1	27MHz	3mm2x2mm5	CRYSTAL HYBRID 27.000MHZ 3225	ECS	ECS-270-20-33-CKM-TR	Digikey, XC1818TR-ND	LOAD
5	1	C6	1uF	rc0603	CAP CER 1UF 10V 10% X5R 0603	Murata	GRM188R61A105KA61D	Digikey, 490-1543-2-ND	NO LOAD
7	3	C26,C28,C30	3.3pF	rc0402	CAP CER 3.3PF 50V NP0 0402	Murata	GRM1555C1H3R3CZ01D	Digikey, 490-1270-2-ND	NO LOAD
10	2	C62,C63	0.1uF	rc0201	CAP CER 0.1UF 10V 10% X5R 0201	TDK Corporation	C0603X5R1A104K	Digikey, 445-7318-2-ND	NO LOAD
15	1	J5	HEADER 4	hdr_4x1	CONN HEADER .100 SINGL STR 4POS	Sullins	PBC04SAAN	Digikey, S1011E-04-ND	NO LOAD
23	1	R36	100K	rc0402	RES 100K OHM 1/10W 5% 0402 SMD	Pansonic	ERJ-2GEJ104X	P100KJTR-ND	NO LOAD
24	8	R38,R48,R51,R52,R53,R55,R58,R60	10K	rc0201	RES 10K OHM 1/20W 5% 0201 SMD	Pansonic	ERJ-1GEJ103C	Digikey, P10KAGTR-ND	NO LOAD
27	1	U3	74LVC2T45GN	sot1116	Dual Tranceiver	NXP	74LVC2T45GN	NXP, 74LVC2T45GN	NO LOAD

Fig 9. Notebook BOM

8. HVQFN exposed center pad solder lands

PTN3355 uses HVQFN package.

The HVQFN package exposed center pad must be soldered to a corresponding solder land on the board for enhanced thermal, as well as electrical ground, performance.

During reflow soldering, solder paste melts and gas or trapped air is released, causing splattering or solder balling. Solder balling and splatter can be minimized if the solder paste is printed as a number of individual dots, instead of one large deposit, and if the solder paste is kept at a sufficient distance from the edge of the solder land.

The solder paste pattern area should cover 35 % of the solder land area. When printing solder paste on the exposed die pad solder land, the solder paste dot area should cover no more than 20 % of this solder land area. Furthermore, the paste should be printed away from the solder land edges. This is illustrated in 01; the solder paste pattern area lies within the boundary indicated by the red line and it is divided by the entire solder land area.

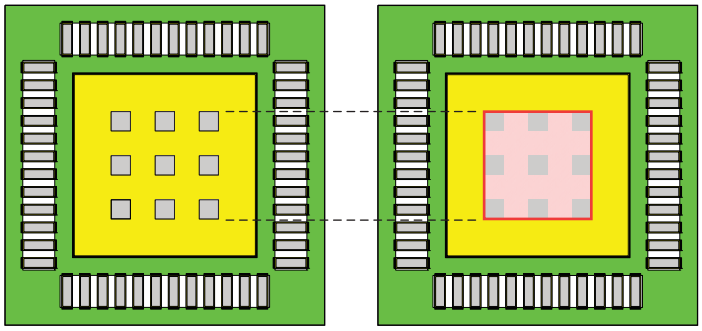


Fig 10. Solder paste dot area (left) and paste pattern area (right)

9. References

[1] PTN3355 datasheet, 14 July 2014

[2] PTN3355 Reference Design Schematics, rev 0.15

[3] AN10873.pdf, PTN3392 application design reference manual

[4] AN10798, DisplayPort PCB Layout Guidelines

[5] Intel Huron River Design Guide, Rev. 0.9, March 2010

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