# AN11267

## EMC and system level ESD design guidelines for LCD drivers

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### Document information

| Info | Content |
|---|---|
| **Keywords** | LCD, LCD driver, COG, Chip-On-Glass, EMC, EMI, ESD, Electro Magnetic Compatibility, Electro Magnetic Interference, Electrostatic Discharge, guidelines, HBM |
| **Abstract** | This application note aims to assist a designer who uses Liquid Crystal Displays (LCD) in a product, to implement design measures in order to optimize EMI and ESD robustness of LCDs and LCD drivers. The difference between system level ESD and device level ESD is explained as well as norms, test procedures and design guidelines to improve system performance. |

### Revision history

| Rev | Date | Description |
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| 1 | 20130211 | new application note, initial release |

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# 1. Introduction

ElectroMagnetic Compatibility (EMC) and ElectroStatic Discharge (ESD) immunity must be considered in the early design phase of a system. This is also true for the application of liquid crystal displays and the accompanying drivers. If ignored, problems encountered later during testing or in the field will become very difficult and expensive to fix, whereas in the early development stage, measures to improve EM and ESD immunity can be implemented at low cost or often even for free. Therefore, an hour or two spent on an early EMC review may well pay off later on in the project. Correct component placement, partitioning of different functions, and having preparations in the layout and mechanics to add a shielding bezel to just name some examples, can save a lot of engineering time and money later on in the project. Ideally this application note would be read before starting a design. Chances are however that you are reading this now, because you have encountered problems in passing EMC-compliance or ESD tests.

This document deals with both EMC and ESD. Sometimes it is not easy to draw a clear line between them. First a clear definition of what is meant by electromagnetic compatibility must be given:

EMC is defined as the ability of a device, an equipment or system to function satisfactorily in its intended electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment.

As systems shrink in size and become more interconnected, EMC is of huge concern to overall system performance. If there is no disturbance problem the situation of electromagnetic compatibility has been achieved. EMC can be divided into two cases:

1. The device, equipment or system is disturbing other devices/systems in its environment. This is called Electro Magnetic Emission (EME)
2. The device, equipment or system is itself disturbed in its environment and therefore it is susceptible. This is called Electro Magnetic Susceptibility (EMS)

In the case of LCD drivers, the focus will be on susceptibility. The power and frequencies used to drive passive LCDs are relatively low and therefore an LCD driver will rarely disturb other components in the application via emissions, let alone other products in the vicinity of the product with the LCD. However, external disturbances, RF fields and electrostatic discharges can affect the operation and reliability of an LCD. In this context the term ‘LCD’ must be interpreted as the liquid crystal display with accompanying driver. The driver can be placed on the glass in a Chip-On-Glass application but it can also be an application with standalone display and a packaged LCD driver.

This application note covers the NXP family of monochrome LCD drivers. This family consists of the following categories:

- Segment drivers: Low multiplex rates (depending on the driver up to 4, 8 or 9), optimized to drive Twisted Nematic (TN), Super Twisted Nematic (STN) and Vertical Alignment (VA) displays. The maximum number of segments that can be controlled using one LCD driver IC is in the order of 1000.
- Character drivers: These drivers are equipped with a display ROM which contains a character set. Just addressing the desired character results in the character being displayed. It is a special form of a dot-matrix display. For every character 5 x 8 dots are reserved. The multiplex rates are up to 18 and the drivers are optimized to drive STN and VA displays.

- Dot matrix drivers: These drivers allow complete freedom to display any kind of graphic within the available display area. Multiplex rates are higher here, up to 80.

Before going into the specifics of the LCD drivers and the design guidelines, first some of the various, relevant, EMC and ESD standards are described in short, along with a description of the test methods. Section 3 gives an introduction to the various EMC standards. In section 4 ESD standards and test methods are discussed, in particular the differences between system level and device level standards and testing.

Sections 3 and 4 have mainly been included for the sake of completeness and only give an introduction into these subjects. For those, who are familiar with the EMC and ESD standards or are mainly interested in a practical solution, it is ok to jump directly to the sections where design guidelines are given, starting at section 5.

## 2. LCD drivers

A Liquid Crystal Display is an electro-optical transducer with analogue signals as electrical driving signals. In order to display information on an LCD, driving electronics is necessary to supply the required signals to the LCD. Usually a design engineer only wants to supply a few data and control signals. Consequently care has to be taken of the specific LCD driver signals. These are coming from dedicated driver ICs, which are in general placed as close as possible to the display. For smaller displays the LCD driver can be placed somewhere on the PCB with all driving signals running over the PCB to the LCD. For larger displays this would result in an unpractical number of connections on the PCB, taking up a large area. In such cases usually an LCD module is used. Here the actual LCD and the driver are integrated onto one unit. This can be either a Chip-on-Board (COB) module where a conventional LCD is mounted on a PCB, or a Chip-on-Glass (COG) module. With a COB module, on the same PCB an LCD and an LCD driver die is mounted, with the contacts facing up. The connections from the die to the PCB are made using wire bonding, followed by a complete epoxy encapsulation for a hermetic seal. Since no conventional IC-package is required this reduces cost, but the wire bonding step is a complication in production.

A second and more common form of an LCD module is the Chip-on-Glass (COG) module. Here the die is placed directly on the LCD glass with the contacts facing down towards the glass. Connections to the ITO tracks are made using gold bumps. This way of creating LCD modules results in the most compact and most cost effective modules. It is a mature and robust technology which has been used for over twenty years, with NXP in a pioneering role, in applications ranging from consumer, industrial to automotive.

There are several display types and also several different driving methods, which implicitly means that there is a need for many different LCD drivers. Many of them are available on the market.

Summarizing these, three different architectures can be distinguished:

- Discrete: Standalone LCD driver in a package driving an LCD
- COB: A module with the unpackaged driver IC die mounted on a PCB which carries the LCD too
- COG: A module with the driver IC die mounted directly on the display glass

Microcontrollers with integrated LCD driver are not considered here, but from an application point of view they are most similar to the first architecture listed above.

## 2.1 Typical application

The information to be displayed is usually prepared in a microcontroller. Via the interface (serial, like $I^2C$ or SPI, or parallel) this information along with configuration settings is transmitted to the LCD driver. The LCD driver then generates the necessary analog signals to drive the LCD.

Electromagnetic disturbances can couple in at almost any part of the circuit:

- At the supply lines
- Via the bus interface
- Directly at the LCD and working its way back into the LCD driver
- At the microcontroller, which may be affected and therefore will not transmit the correct information to the LCD driver

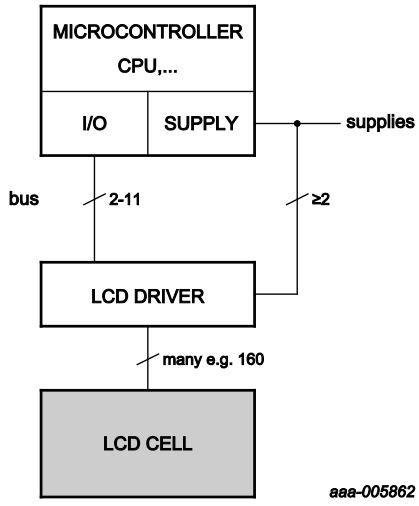



**Fig 1. Typical LCD application**

This will be handled in more detail in later sections.

# 3. Introduction to EMC/ESD standards

Several organizations exist which define standards important for the electronics industry. One of them is the IEC: the International Electrotechnical Commission. It is the leading global organization that prepares and publishes International Standards for all electrical, electronic and related technologies. In addition it promotes international cooperation on all questions of electro-technical standardization and related matters in the fields of

electricity, electronics and related technologies. Having international standards saves cost by harmonizing test methods worldwide. The IEC is made up of National Committees representing the electro-technical interests of their respective countries. The IEC has also defined standards relating to EMC and ESD.

There are two main IEC committees dealing with EMC. One is the International Special Committee on Radio Interference which operates by its French acronym CISPR (Comité International Spécial des Perturbations Radioélectriques). Its principal task is at the higher end of the frequency range, from 9 kHz upwards. CISPR prepares standards which offer protection of radio and TV reception from various interference sources and it covers the measurement of radiated and conducted interference. CISPR's organization is divided into six subcommittees, each responsible for a different area:

- A – Measurement of radio interference and statistical methods
- B – Measurement of interference regarding industrial, scientific or medical (ISM) equipment, high voltage equipment, power lines and traction devices
- D – Interference in motor vehicles, both gasoline and electric
- F – Interference in household appliances, tools and lighting equipment
- H – Limitations to protect radio frequencies
- I – Electromagnetic compatibility of information technology (IT) equipment, multimedia / hi-fi equipment and radio receivers.

The second committee, B, is called TC 77 and its main task is to prepare **basic** and **generic** EMC publications specifying electromagnetic environments, emissions, immunity, test procedures, measurement techniques etc. TC 77 has three subcommittees: SC 77A, SC77B and SC77C. SC 77A deals with-low frequency phenomena up to 9 kHz. SC 77B deals with high-frequency continuous and transient phenomena including electrostatic discharges. SC 77C covers high-power transients. An important part is the description and classification of the EM environment which can be used by product committees to create specifications for the particular products they are standardizing.

Three classes of standards exist:

- Basic standards

  These standards provide general and fundamental rules in order to achieve EMC, which can be applied to all products, systems and networks. Basic standards serve as a reference and are not applicable to specific products. They provide general information about the way the EM disturbance is taking place and provide limits which must be adhered to. The basic standards are contained in the IEC 61000 or CISPR 16 series of publications.

- Generic standards

  Generic EMC standards are for products operating in a particular EMC environment for which no specific EMC standards exist yet. The standard then provides essential requirements and test procedures which must be applied to any product operating in this environment. The standard also provides limits and test procedures. These standards fill the gap until a product standard exists.

- Product standards

  These are standards that apply to specific products or families of products and provide test procedures and limits for these products.

## 3.1 Structure of IEC 61000

The IEC 61000 series (basic standards) will eventually consist of nine parts. Currently the titles of Parts 7 and 8 are still open, therefore now seven parts exist. The structure of this series reflects the subjects dealt with by basic EMC requirements (although Part 3 does not contain basic EMC publications). The parts in the series include terminology, descriptions of EM phenomena and the EM environment, measurement and testing techniques and guidelines on installation and mitigation.

Part 1: General

- General considerations like introduction, definitions, terminology, function requirements (what the function does)
- Safety integrity requirements; the likelihood of a safety function being performed satisfactorily.

Part 2: Environment

- Description of the environment
- Classification of the environment
- Compatibility levels

Part 3: Limits

- Emission limits
- Immunity limits (unless product committees have dealt with these already)

Part 4: Testing and measurement techniques

- Measurement techniques
- Testing techniques

Part 5: Installation and mitigation guidelines

- Installation guidelines
- Mitigation methods and devices

Part 6: Generic standards

Part 9: Miscellaneous

The part most relevant to the LCD applications this manual is about, is IEC 61000-4.

# 4. ESD standards and test methods

ESD is an abrupt discharge of static electricity between objects at different electrical potentials and is therefore all but a static phenomenon. In order to generate static electricity, for example due to friction between two different materials, at least one of those needs to be non-conducting.

The high voltages that cause ESD are caused by tribo-charging, the natural process by which electrons get transferred from one material to another material of a different type when they are rubbed together or separated from each other. This happens because the two materials being in contact with each other are exchanging electrons (see Fig 2) to equalize their electrochemical potential (ECP). This is a thermodynamic measure combining the concepts of energy stored in the form of electrostatics and in the form of chemical potential.

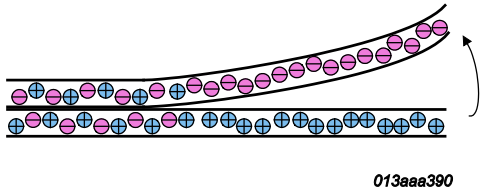



**Fig 2. Tribo-electric effect**

When separated, some materials tend to give electrons away whereas others tend to keep extra electrons. This will not be dealt with in detail here, but the result is that both materials are at different electrical potentials after being separated. This is also what happens when the protective tape is removed from an LCD, and the buildup of static electricity is visible on the display (random segments being on). Friction increases the possibility to exchange electrons because it enhances the contact surface of the two materials.

Materials which are often very ‘suitable’ for tribo-charging are man-made fabrics and plastic materials. At the same time process structures in the semiconductor industry become smaller and smaller so ESD problems become more and more common. ESD is a very fast phenomenon, and a very intense one while it lasts. The duration is usually just a few tens of nanoseconds overall.

Several types of ESD exist and also several types of ESD specifications and ESD tests. In order to avoid confusion it is important to make a clear separation between ESD specs as listed in datasheets (device level) and ESD specs for an end product (system level).

## 4.1 Device level ESD specs

In most datasheets there is a section containing ESD specifications. The ESD specifications in the datasheet are related to the electrostatic handling voltage of the device. For ESD evaluations standardized test procedures have been developed along with standardized ESD pulses for the following three models:

- HBM: A person discharges to an IC
- MM: A machine or tool discharges to an IC
- CDM: A charged IC discharges to its environment

All three models (HBM, MM and CDM) are (semiconductor) device level specifications and are used to qualify ICs. They guarantee the ESD levels that a device can withstand when the discharge is directly to or from the pins of the IC. These specifications are intended for customer assembly production lines. In general they say nothing about the ESD immunity of the system in which these semiconductors are used. Once the IC has been mounted on the board, most of the pins will never see the outside world again. Only some inputs and outputs will be exposed to the outside world and on system level, care needs to be taken that these pins are properly protected for the system to fulfill its ESD requirements.

LCD drivers are a bit special in this respect because here most pins will still see the outside world via the display. Most pins will be driver outputs driving the LCD and an ESD to the display will work its way back to the driver.

### 4.1.1 Human body ESD

Human body ESD is caused by people becoming tribo-charged, usually by walking around, wearing certain fabrics, combing dry hair with a plastic comb or by moving on or ascending from a seat. Walking on plastic floor coverings, synthetic carpets etc. can easily result in this kind of charging. The Human Body Model (HBM) is a model created in order to have a well defined model against which to test for this kind of ESD. The Human Body Model is commonly used for characterizing the susceptibility of an electronic device to damage from ESD. It is a simulation of the discharge which might occur when a human touches an electronic device. Several HBM definitions and test methods exist, for example according EIA/JEDEC JESD-A114, the US military standard MIL-STD-883, the JEDEC standard JS-001 and AEC-Q100-002. In these models the human body is modeled by a 100 pF capacitor and a 1500 Ω discharging resistor. During testing the fully charged capacitor is discharged through the resistor connected in series to the EUT, see Fig 4.

### 4.1.2 Machinery ESD

Machinery ESD occurs when isolated metal parts rub against insulating materials, or have a flow of insulating liquids or gases over them. The metal parts are tribo-charging until they can discharge with a spark into something nearby which was not previously charged, equalizing their potentials. Sparks created in this way by machinery can be very intense, especially when the metal part being charged is large and so has a large capacitance, which can store a large amount of charge. The Machine Model (MM) has been created in order to have a defined model against which to test this kind of ESD immunity. It contains a capacitance of 200 pF and an inductance of 0.75 µH.

### 4.1.3 Charged Device Model

A Charged Device Model (CDM) is used to define the ESD a device can withstand when the device itself has an electrostatic charge and discharges due to metal contact. This discharge type is the most common type of ESD in electronic devices and causes most of the ESD damages in manufacturing. CDM discharge depends mainly on parasitic parameters of the discharge and is strongly depending on size and type of component package.

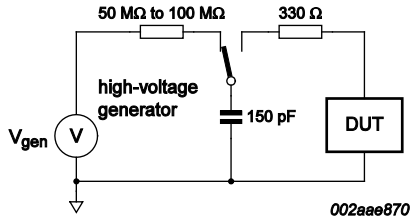



Fig 3. System level ESD testing according to IEC61000-4-2

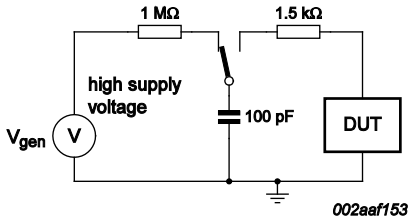



Fig 4. HBM test circuit (device level)

## 4.2 System level ESD specs

Device level ESD pulses and system level ESD pulses (according IEC 61000-4-2) should be considered with separate test acceptance criteria. There is a disconnection in the EMC world between system manufacturers, who test systems for upset (that is, the system may be disturbed), and device manufacturers testing devices for failure of the device. There is no relation at all between device level ESD specifications and system level ESD specifications. A complete system consists of many more components, which are connected together using one or more PCBs. All these components, the PCB layout and system software have an influence on system level ESD robustness. The fact that a device may not suffer any damage due to an ESD event does not mean that it continuous to function undisturbed in a system. If a bit in a register changes, its behavior will change but no damage was done. Similarly changing RAM content will result in unwanted or lacking information on the display. A reset, power cycle or rewriting the registers and display RAM would correct this. Despite this fact some system level manufacturers are pushing device manufacturers to test semiconductor devices using system-level compliance standards, specifically IEC61000-4-2, for ESD. Product manufacturers would like to believe that if devices are qualified to IEC standards, end products will likewise be qualified. Unfortunately there is a fundamental difference between system-level and device-level testing. Table 1 shows a comparison between the peak current of HBM versus IEC61000-4-2 standards.

Table 1. Peak current of HBM versus IEC61000-4-2 ESD standards

| Applied voltage [kV] | Peak Current [A] Human Body Model (IC-level) | Peak Current [A] IEC61000-4-2 (system level) |
|---|---|---|
| 2 | 1.33 | 7.5 |
| 4 | 2.67 | 15.0 |
| 6 | 4.00 | 22.5 |
| 8 | 5.33 | 30.0 |
| 10 | 6.67 | 37.5 |

The “*human body model*” as defined in IEC 61000-4-2 is not meant to test on device level, but it serves to verify the ESD robustness of an apparatus or equipment. The ESD simulator used for testing according to IEC 61000-4-2 is based upon the 150 pF/330 Ω human model. The typical test circuit is shown in Fig 3 and the characteristics of the pulse are shown in Fig 5. It is unfortunate that this model is also often referred to as human body model because this creates confusion with the HBM as specified in datasheets. In the remainder of this document the term “human body model” is only used for device level specifications. When ESD testing or specifications on system level are meant always IEC 61000-4-2 (a basic standard) is referred to, and the term “human body model” is avoided.

The ESD simulator used for testing according to IEC 61000-4-2 generates a waveform with a rise time of between 700 ps and 1 ns to reach a peak of several kV, which then decays to about 50 % in 50 ns. At a voltage of 8 kV the peak current into a 50 Ω load is almost 20 A. The frequency spectrum of such an ESD waveform is flat to around 300 MHz and then begins to roll off. Therefore it contains significant energy at 1 GHz and above.

Some older test standards exist, which use a model with a much longer rise time of 5 ns. Its spectrum already starts to roll off at 60 MHz and is therefore much less aggressive than IEC 61000-4-2. However, even this norm may not even be aggressive enough as it appears that real ESD events can have rise times even faster than 700 ps.

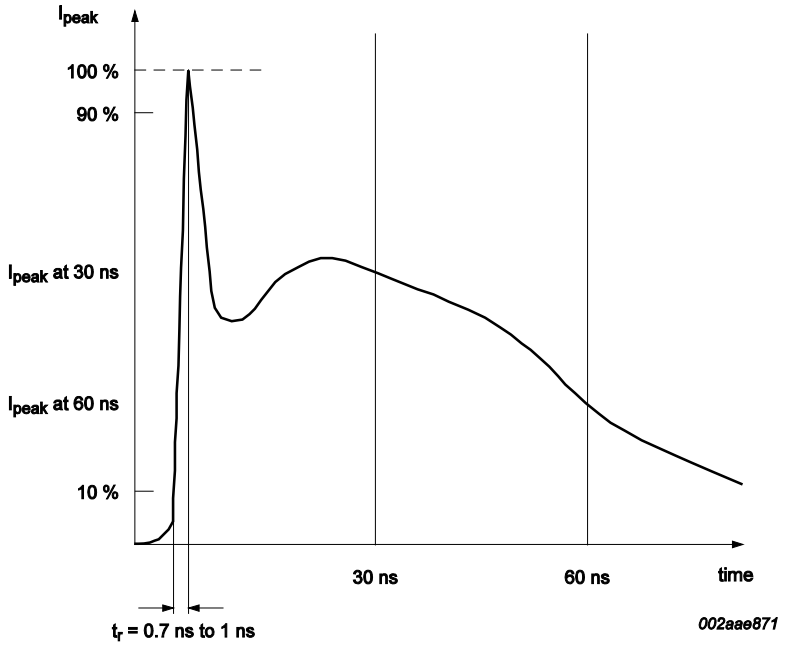



**Fig 5. ESD surge charge according to IEC 61000-4-2**

This manual deals with effects due to discharge of the human body at system level, that is of an end product using semiconductors, and about increasing the system robustness w.r.t. ESD and EMC. Therefore the relevant ESD pulse is the one defined in:

IEC61000-4-2; “Testing and measurement techniques – Electrostatic discharge immunity test”.

IEC 61000-4-2 is about the immunity requirements and test methods for electronic equipment subjected to static electricity discharges, directly from operators. It also defines various ranges (classes) of test levels representing different environmental and installation conditions. The standard defines the typical waveform of the discharge current (Fig 5) with a range of test levels (see Table 2), the test setup, procedure and equipment.

The human body has the ability to charge and store energy that can result in a voltage of several thousands of volts (8 kV to 15 kV is not uncommon) and a discharge current with peak currents from 1 A up to several tens of ampere. The timing in which this charge is delivered varies as follows:

Rise time $t_r$: 200 ps to 20 ns

Spike time $t_{spike}$: 0.5 ns to 10 ns

Total time $t_{tot}$: 100 ns to 2 µs

The ESD waveform of the IEC specification has similar characteristics; however the amount of energy delivered is far greater than a HBM pulse (for device testing).

An end product must have high immunity against users who may have been charged up to a high voltage. “Immunity” here will often mean that the product continues working without disturbance. At device level (IC level) “immunity” means that no damage occurs. These are clearly two different things.

System level ESD performance depends also on much more than just the devices that are used in the system. It is related for example to the entire application circuit and PCB layout. Given these principal differences it is clear that the ESD robustness of an application cannot be deduced from the ESD robustness of the IC.

## 4.3 Human ESD

Now that the difference between device level ESD and system level ESD is clear, it is interesting to look more detailed into an ESD event between a real human and a product with an LCD. As the hand or fingertip of a charged person approaches a metallic or conductive surface of an Equipment Under Test (EUT), and prior to the discharge, an electrostatic field exists. The field strength increases with decreasing distance and no or very little current is flowing. Therefore also no magnetic field is present.

Once the discharge starts, the electrostatic field in the gap between the hand and the EUT collapses to a voltage of about 25 V to 40 V within the short duration of 50 ps to 5 ns.

Simultaneously a current starts flowing. Fig 5 is the standardized IEC discharge current, which attempts to realistically model the current as it appears in real. While the current continues to expand on the EUT and arm, it experiences reflections and losses due to radiation and resistance. This leads to a very complex pattern of current densities.

The highest frequency components of the current will be attenuated quickly, mainly due to radiation. Then the current becomes smoother and at the end a new electrostatic equilibrium between body and EUT is reached. However, there may be a remaining charge on the body. The hand is still approaching the EUT and a second discharge may occur at a lower voltage. This can lead to a series of discharges. Consecutive discharges

will be at a lower voltage and each one having a faster rise time. This leads to changing charge densities and changing currents result in radiated fields. One can distinguish between the near field and the far field. In close proximity to the arc (the near field) the field is dominated by the current and charge directly. The far field conditions are reached at about 10 cm from the arc. Here the current and charge time derivatives determine the fields.

These fields can disturb the electronics system without destroying it. Also disturbing systems due to an ESD is not allowed in many applications, as this will affect the user experience.

## 4.4 ESD testing

### 4.4.1 Air discharge test

For the ESD test a test gun is used. See Fig 6 for tip shapes. The air discharge attempts to simulate the circumstances of a real human touch as described in section 4.3 “Human ESD” as realistically as possible. During the air discharge test the charged electrode of the test generator is moved towards the DUT/EUT until it touches the DUT (Device Under Test). Often the discharge occurs before the test generator touches the DUT, once the distance became small enough to trigger the discharge. Using air discharge the following effects are simulated:

- The electrostatic field which exists before the discharge occurs
- The pre-discharge resulting from the corona
- The dynamic electric and magnetic field of the (repeating) spark discharge
- The current injection

However, the properties of all these effects are dependent on some parameters which can’t always be well controlled such as the speed of approach of the discharge tip, local humidity, shape of the discharge tip, and construction of the ESD generator. These variables lead to variations in pulse rise time and magnitude of the discharge current.

### 4.4.2 Contact discharge test

Given the variables when using air discharges during testing, contact discharge is the preferred test method since this is the best defined and reproducible method. Air discharges can be used when a contact discharge can’t be applied or as an additional test, but the result is influenced by the parameters mentioned above.

During the contact discharge test the electrode of the test generator is moved into position such, that it contacts the intended test point of the DUT. Then the discharge is actuated by flipping the discharge switch within the generator, see Fig 3.

The test levels for the various classes - contact discharge and air discharge - are given in Table 2.

IEC 61000-4-2 also specifies compliance levels, with a Class 4 being the most severe and representing an 8 kV contact discharge or a 15 kV air discharge onto the EUT.

Table 2. IEC 61000-4-2 ESD surge classification

| Contact discharge | | | Air discharge | |
|---|---|---|---|---|
| **Class** | **Test voltage [kV]** | **Maximum current [A]** | **Class** | **Test voltage [kV]** |
| 1 | 2 | 7.5 | 1 | 2 |
| 2 | 4 | 15 | 2 | 4 |
| 3 | 6 | 22.5 | 3 | 8 |
| 4 | 8 | 30 | 4 | 15 |
| x | special | special | x | special |

Here “x” can be any level, above, below or in between the other levels.

If a device would have to withstand these discharges directly at its pins without damage, huge ESD structures would be required, which would increase cost price a lot. And still, no guarantee could be given that the system would not be disturbed.

The test generator must meet the specifications given in Table 2 and Table 3.

Table 3. General specifications of a test generator

| Parameters | Values |
|---|---|
| Output voltage, open circuit, contact discharge mode | At least 1 kV to 8 kV |
| Output voltage, open circuit, air discharge mode | At least 2 kV to 15 kV (unless application does not need to be tested up to 15 kV) |
| Tolerance of output voltage | ± 5 % |
| Polarity of output voltage | Both positive and negative |
| Holding time (interval within which the decrease of test voltage due to leakage prior to discharge is < 10 %) | ≥ 5 s |
| Discharge mode of operation | Single discharges, repetition rate of at least 20 times per second |

The discharge electrodes shall conform to the shapes and dimensions shown in Fig 6. Insulating coating of the electrodes is permitted as long as the discharge current waveform specifications are met.

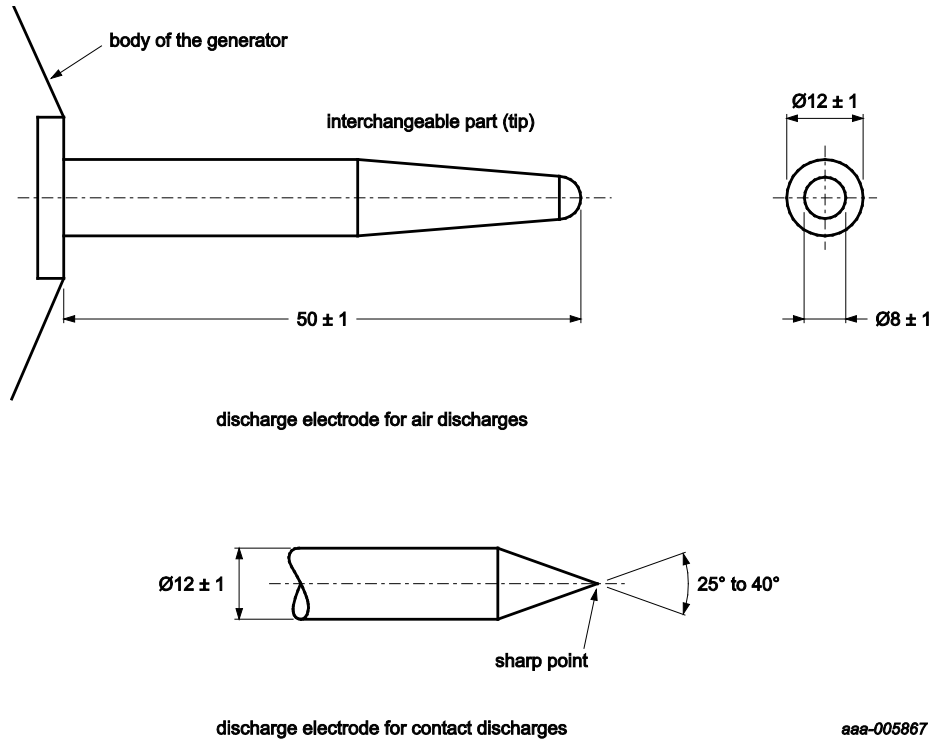



**Fig 6. Discharge electrode shapes and dimensions**

## 4.5 ESD test setup

The ESD test setup is illustrated in Fig 7 and includes

- The ESD generator
- The discharge return cables
- The two 470 kΩ bleeder resistors
- The ground reference plane
- All connections that form the discharge path

The ground reference plane (GRP) is lying on the floor of the test room. It is a metallic sheet. If copper or aluminum is used, the minimum thickness is 0.25 mm. If other metallic materials are used the thickness must be at least 0.65 mm. The dimensions of the ground reference plane must be such that it projects beyond the EUT by at least 0.5 m on all sides. It must be connected to the earth protective grounding system of the building. The EUT must be at least 0.8 m away from the walls of the test room or any other metallic structure.

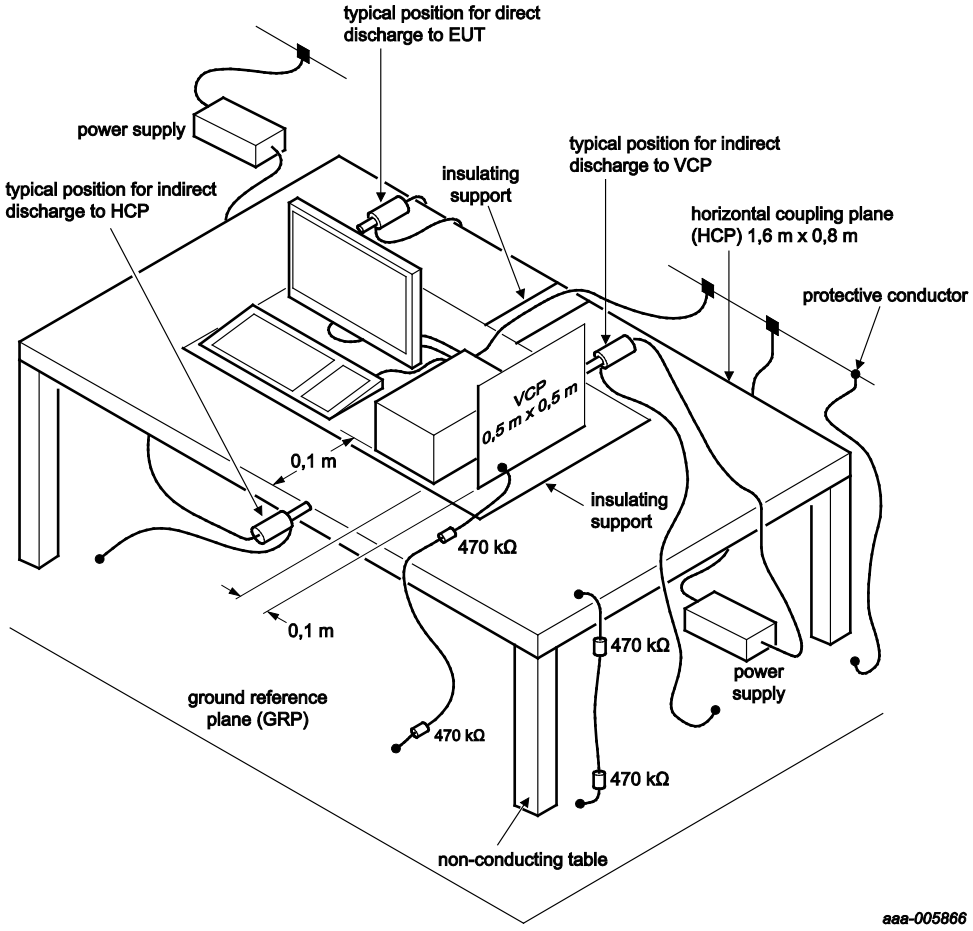



**Fig 7. ESD test setup according to IEC 61000-4-2**

The 470 kΩ resistors which are inserted in the grounding cables serve to prevent the charge applied to the planes disappearing instantly after the discharge of the ESD generator to the plane. This increases the impact of the ESD to the EUT. Obviously these resistors must be capable of withstanding the maximum discharge voltage used during the tests. Splitting them in two eases the requirements for the individual resistor.

In addition to the ground reference plane (GRP) there is a horizontal coupling plane (HCP) with dimensions of 1.6 m x 0.8 m. The HCP is placed on the table. The table must be non-conductive and is usually made of wood. The EUT and its cables must be isolated from the coupling plane by an insulating support of at least 0.5 mm thickness.

The electrostatic discharges shall be applied only to those points and surfaces of the EUT which are accessible to persons during normal use. In many applications, the LCD surface can be touched by the user and in this case discharges shall be applied directly to the LCD surface as well. In many other applications the LCD is behind a plastic or glass window, for example a display in a car's instrument cluster. In such a case the user can't touch the display directly.

Testing to IEC 61000-4-2 involves the following:

- Air discharges are applied to everything non-metallic which is normally accessible by the operator
- Contact discharges are applied to operator accessible metal or conductive parts, and also to nearby vertical and horizontal metal plates.

Test voltages are increased gradually from low values in steps of for example 1 kV, up to 100% of the test voltage. This is because ESD failures or setups are sometimes seen on lower voltages but not on the maximum test level. The highest level is not necessarily the one most likely to cause a failure. An LCD enclosed with a metal bezel for example, will see ESD at lower voltage levels go directly to the display glass, thus affecting the display where the ESD at higher levels may be to the metal bezel.

When a discharge into equipment occurs, the discharge current will flow through the equipment via different paths. The high frequency components will flow radially, whereas the low frequency components will seek the path of least resistance to ground. This current flow will excite any existing antennas (as formed in the application) in their path. The efficiency (gain) of these antennas is primarily dependent on their size. Since a ¼ wavelength antenna is very efficient, it can easily have a dimension of 1.5 cm to 150 m. For ESD events, even a $^{1}/_{20}$ wavelength antenna may conduct a significant amount of energy.

In dealing with ESD there are three steps:

1. Avoid the discharge. This is not always possible;
2. Drain the discharge to GND;
3. Immunize the electronics. This is the subject of the next chapters.

# 5. Hardware design measures to improve ESD and EMC behavior

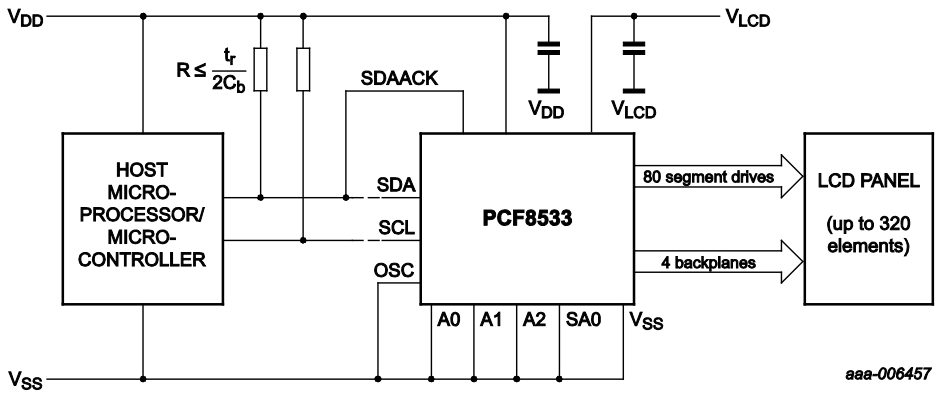
In order to achieve an application with optimal ESD and EMC behavior, the first step is to apply well known basic design guidelines which are generally valid and not just for LCD drivers. Most EMC design rules are also valid for ESD immunity improvement. The power supply must be stable and clean, also under the influence of ESD or EMI. Steps like adequate decoupling and good layout can be implemented at low cost. If shielding is required this will usually be relatively expensive.

## 5.1 Power supply decoupling

Power supply decoupling (or actually filtering of supply disturbances) must function from low up to very high frequencies and must have no resonances. Therefore the aim is a minimum impedance between driver and decoupling and a maximum impedance between decoupling component and power supply, whereby the DC is not hindered.

In many practical situations the optimal design practices are not implemented due to cost reasons. This is not necessarily a problem, as long as legal and functional requirements are fulfilled.

The NXP LCD drivers typically have two different power supplies. One is for the logic in the driver ($V_{DD}$); the other is for the display ($V_{LCD}$). Both require their own decoupling.

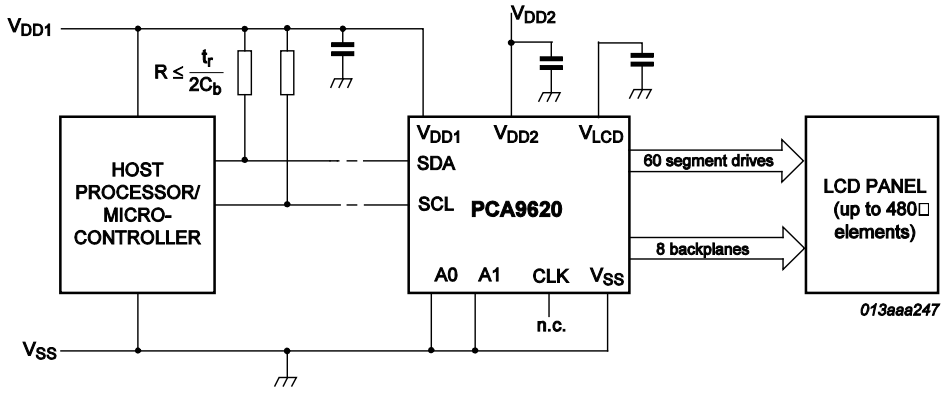



(1) PCF8533 is a COG driver. That is why instead of just SDA there is SDA and SDAACK.

**Fig 8. Typical application of LCD driver without integrated charge pump**

Fig 8 gives a typical application of an LCD driver without integrated charge pump, where $V_{DD}$ and $V_{LCD}$ use different voltages and where both have their own decoupling. Use a ceramic capacitor of 100 nF for $V_{DD}$ and a ceramic capacitor of 470 nF to 1 µF for $V_{LCD}$, depending on the display size. It is also important to make the tracks from power pin to the capacitor and from the capacitor back to the $V_{SS}$ pin as short as possible. By keeping the tracks short, the decoupling loop area will be kept as small as possible. Using packaged devices it is easy to follow these guidelines. Ceramic capacitors tend to have low inductance because of their flat plate construction. Most other types of capacitors are wound and thus inductive. Nowadays SMD capacitors are dominant in small signal applications. The lack of connecting leads has a positive effect on decoupling properties.

X7R is a reasonably stable high-permittivity dielectric which allows capacitance values up to 1 µF into a reasonable package. The available range is in the order from 100 pF to 22 µF in SMD; even larger values are available in leaded packages. The capacitance of X7R type varies under the influence of electrical operating conditions such as voltage and frequency. This rules out many applications, but they are very suitable for decoupling purposes. The leakage current is sufficiently low. Fig 9 shows a typical application of an LCD driver with integrated charge pump. Also here, there are two supply voltages but $V_{LCD}$ can be generated internally in the chip and only one supply voltage needs to be supplied to the LCD driver. $V_{LCD}$ still needs its own capacitor.




(1) For capacitor values, see text

**Fig 9. Typical application of LCD driver with integrated charge pump**

### 5.1.1 Power supply decoupling in COG applications

In COG applications the power supply is often divided in more separate connections (bumps) for functions as the various logic circuits, the charge pump and the bias voltage generation. Therefore these LCD drivers have $V_{DD1}$, $V_{DD2}$, $V_{DD3}$, $V_{LCD1}$, $V_{LCD2}$ and also various $V_{SS}$ supply rails. This allows the module maker to connect these supply circuits using separate ITO tracks. In this way the common (shared) part of the ITO track is minimized or eliminated. This reduces the amount of common-mode electrical noise.

An example is given in Fig 10. Multiple power supply pins with equal function can be grouped and can be decoupled from that central point. As stated before, it is also best to keep the tracks from supply pins to decoupling capacitor and from the capacitor back to $V_{SS}$ as short as possible. With COG applications the foil connector may be several cm long which also increases the distance between decoupling capacitor and LCD driver. If required it is possible to place the decoupling capacitor on the foil.

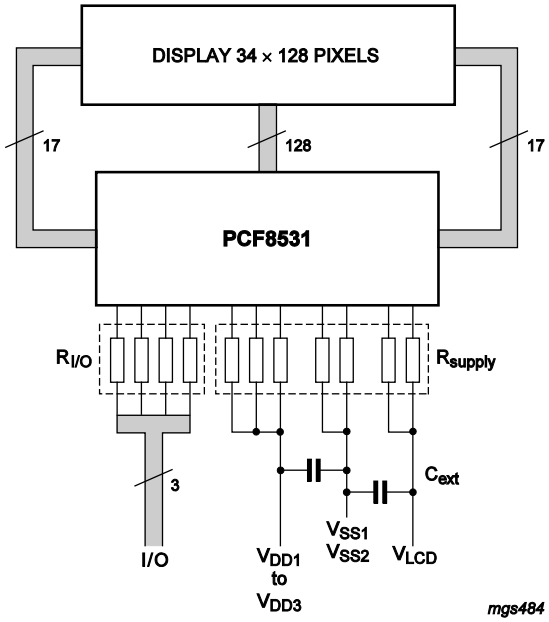



**Fig 10. Typical chip-on-glass application**

Fig 11 and Fig 12 represent the ITO and glass-to-PCB connection paths in two typical configurations. Suggested maximum resistance values of the power supply for a typical small display application (character drivers and dot matrix drivers, pixel size approximately 0.25 mm x 0.25 mm) are given in Table 4. These limits depend on the display load and need to be revised for each particular application. Excessive track resistance, especially common track and connection resistance will result in:

- A deterioration of the display quality
- Increased power consumption
- Incorrect operation

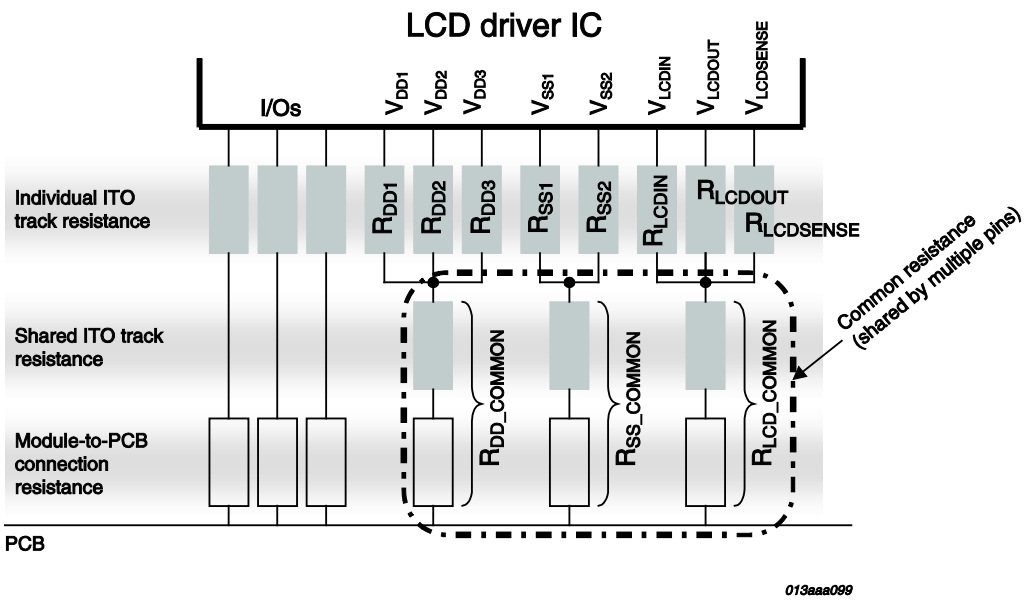



**Fig 11. $V_{DD1} = V_{DD2} = V_{DD3}$**

The $V_{SS}$ line is most critical. Therefore the ITO track resistance has to be kept as low as possible.

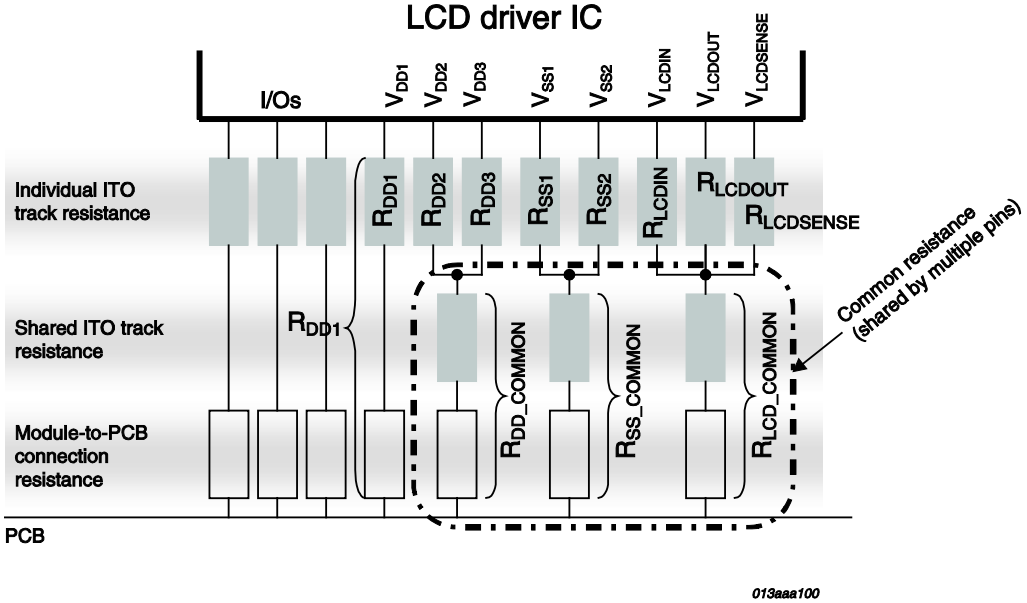



**Fig 12. $V_{DD1}$ # $V_{DD2} = V_{DD3}$**

**Table 4. Maximum ITO track resistance for display drivers with integrated charge pump**

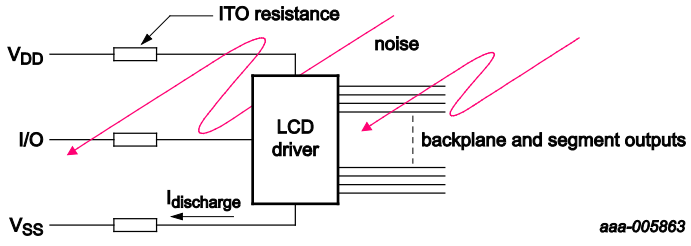
*Recommended maximum ITO track resistances*

| Resistance path | Description | Maximum resistance [Ω] |
|---|---|---|
| $R_{DD\_COMMON}$ | Common $V_{DD}$ track, including connector | 40 |
| $R_{DD1}$ | Positive logic supply | 500 |
| $R_{DD2}$ | Positive charge pump supply | 200 |
| $R_{DD3}$ | Positive analogue supply | 2000 |
| $R_{SS\_COMMON}$ | Common $V_{SS}$ track, including connector | 40 |
| $R_{SS1}$ | Negative supply (excluding charge pump) | 80 |
| $R_{SS2}$ | Negative charge pump supply | 200 |
| $R_{LCD\_COMMON}$ | Common $V_{LCD}$ track, including connector | 60 |
| $R_{LCDOUT}$ | Generated $V_{LCD}$ output | 100 |
| $R_{LCDIN}$ | $V_{LCD}$ input to chip | 500 |
| $R_{LCDSENSE}$ | $V_{LCD}$ sense input | 2000 |

More information about designing COG modules can be found in AN10170, section 8, references.

All guidelines given above serve already to guarantee proper operation without taking EMI or ESD into account. Adding these aspects for consideration shows why it is important to keep ITO track resistances as low as practically possible.

Fig 13. indicates how an external field can affect the LCD driver via the backplane and segment outputs and how the current flows on the display module via the various ITO tracks.




1. $I_{discharge}$ is limited by ITO resistance, and creates voltages across $R_{ITO}$

**Fig 13. External field or ESD event affecting the LCD driver via its outputs**

The discharge current will also flow via the $V_{DD}$ lines and I/O lines, but it is likely that most of the discharge current will flow via the $V_{SS}$ line. It is important to minimize the ITO track resistance, especially of the $V_{SS}$ line, in order to minimize the voltage step that results from these currents. These discharge currents will affect the supply voltage that the LCD driver sees, and the sudden change may affect the operation.

## 5.2 $I^2C$ pull up resistor values

The SDA and SCL lines in $I^2C$ devices are open-drain outputs and therefore an external pull-up resistor is required on each of the two lines. Besides the normal considerations regarding rise time and fulfilling timing requirements (a smaller resistor value reduces the rise time) and current flow during the LOW state of the line, LCD COG-modules require even more attention when a pull-up resistor value is chosen. The ITO track resistance, $R_{ITO}$, together with the pull-up resistor $R_{PULL-UP}$, forms a voltage divider. Because of this there is a danger that the other devices on the $I^2C$ bus will not see a valid logic LOW when the LCD driver pulls the SDA line LOW e.g. during the Acknowledge cycle or read back (only some drivers provide this feature) from the IC. For more details see AN10170, also listed in the references, section 8.

Taking all these considerations into account, leads to a range of suitable resistor values. It is advised to use one of the lower values in the range, because this will make the circuit less susceptible to EMI.

## 5.3 Layout considerations

Keep the display driver as close as possible to the LCD. In case of a COG module this is achieved by integrating the drive on the module. In principle it is also best to keep the length of communication bus tracks between microcontroller and display driver short, but often it is difficult to optimize (read, minimize) both distance between LCD driver and LCD, and also between LCD driver and microcontroller. In this case it has priority to keep the length of traces between LCD driver and display as short as possible. One reason for this is that there are many more traces between the LCD driver and the display than between the LCD driver and the microcontroller.

## 5.4 Choice of oscillator (internal or external)

NXP LCD drivers contain an integrated oscillator which drives the logic and determines the LCD frame frequency. In addition the LCD drivers offer the possibility to use an external oscillator instead of the internal oscillator. This makes it possible to use a very well controlled oscillator which then results in a well defined frame frequency. Many of NXP's state of the art LCD drivers offer the option to program the LCD frequency with small tolerances.

Experience has shown that using the internal oscillator results in the highest robustness against EMC and ESD. If an external oscillator signal is used, there is a track running from the oscillator to the LCD driver and this signal may be susceptible to EMI and ESD as well.

## 5.5 Sync signal

In order to achieve synchronous operation between cascaded chips, a sync pin has been provided. The only time that SYNC is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments, or by the definition of a multiplex mode when segment drivers with different $I^2C$ addresses are cascaded). The sync pin is organized as an input/output, the output selection being realized as an open-drain driver. It is not a tri-state pin. It is either output or input. A sense circuit (input) is

connected to this pin as well as an open drain output circuit. If the open drain output transistor is conducting, the SYNC pin will be LOW. If the open drain output transistor is not conducting the SYNC pin acts as an input and the segment driver is monitoring this pin. The sync pin is only actively driven LOW but never driven actively HIGH. Its HIGH level is via an internal pull-up resistor. The value of this internal pull-up resistor is large and therefore the SYNC pin as output is not able to drive a significant load. Under the influence of a strong external noise signal, the SYNC line may be affected. This is also true in a non cascaded application, where only one segment driver is used. If a disturbance is seen on the display while doing EMC compliance testing, it is worthwhile to try connecting an external pull-up resistor between $V_{DD}$ and SYNC. A good starting value is 100 kΩ and one can go down to 10 kΩ. Note that this will increase power consumption of the application.

Only with a continuously applied external noise signal, the sync pin can give a clearly visible disturbance. With a single discharge as with ESD or a single interference the display would be disturbed for maximal one frame. At worst a brief flicker would be seen on the display.

If adding the external pull-up resistor has no influence, the SYNC pin is not the cause of the problem and the resistor can be removed again.

## 5.6 Choice of $V_{LCD}$

The optimal choice for $V_{LCD}$ depends on the LCD, in particular on the liquid properties. The bias voltages are fractions of $V_{LCD}$ and are obtained from an internal voltage divider between $V_{LCD}$ and $V_{SS}$, followed by buffers.

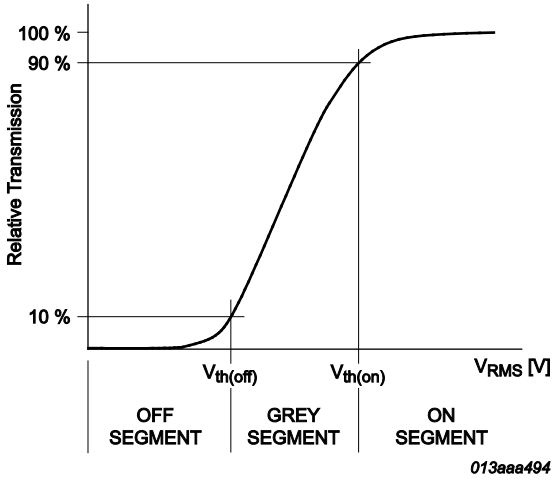



**Fig 14. Electro-optical characteristic: relative transmission curve of the liquid**

In Fig 14 the relative transmission as a function of the RMS voltage across a display element is indicated. Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. For any given liquid there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see Fig 14. For a good contrast the following rules must be observed:

- $V_{on(RMS)} \geq V_{th(on)}$
- $V_{off(RMS)} \leq V_{th(off)}$

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module maker. $V_{th(off)}$ is sometimes just named $V_{th}$. $V_{th(on)}$ is sometimes named saturation voltage $V_{sat}$.

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by a few parameters (refer also to the datasheet of the driver used), one of which is $V_{LCD}$.

The effect of external HF fields on the LCD driver is sometimes a reduction in the voltages that are available on the segment and backplane (or column and row) outputs. As a result, the generated $V_{on(RMS)}$ is no longer larger than $V_{th(on)}$ and therefore the display element does not properly switch on. Since the generated $V_{on(RMS)}$ is directly proportional to $V_{LCD}$ this effect can be counteracted by increasing $V_{LCD}$. Of course also $V_{off(RMS)}$ will increase if $V_{LCD}$ is increased, but as long as it stays below $V_{th(off)}$ it will not have an optical effect. Therefore choosing $V_{LCD}$ in the upper end of the allowed range, probably a bit higher than the specified operating voltage, can result in creating some extra reserve. It will require some experimenting to find the optimum value for $V_{LCD}$.

### 5.6.1 Difference between TN/STN and VA technology

In addition to the conventional TN and STN technology, great progress has been made by a new display technology, VA, which stands for Vertical Alignment. VA displays have deep blacks in off state and good transmissivity in the on state, and therefore a much higher contrast than (S)TN displays. One of the differences between TN and VA is in the liquid which is being used. Module makers use various commercial names for this technology in which the term black nematic is often seen. It seems that smaller reductions in the generated $V_{on(RMS)}$ are already visible on the display if the VA technology is used. This means that in practice, display applications with this technology will have reduced electromagnetic immunity.

In addition to reduced immunity, using VA technology will result in higher radiated emission levels. There are a few reasons for this. First, the operating voltage is higher than for TN displays. Secondly, the required frame frequency is higher than for TN displays. In addition, frame inversion mode (driving scheme B) is less suitable for VA displays. Therefore line inversion mode (driving scheme A) must be used. In line inversion mode the DC offset of the voltage across the LCD is compensated over one line as compared to frame-wise for frame inversion mode, which is another contributing factor to higher frequencies of the driving signals.

## 5.7 Metal parts

Do not have metal parts floating, but connect them to ground. If metal parts are floating, a substantial increase in the amount of capacitive coupling results. Metal parts can be for example heat sinks, and more related to LCD applications a metal bezel. Such a bezel is used to keep the LCD in place, and is an example of a metal part that should be grounded.

## 5.8 Dummy pads (COG layout)

Some LCD drivers have dummy pads (test or reserve pads). These should not be connected to ITO tracks, unless the datasheet states otherwise. Often dummy pads do not have ESD protection elements and in this case connecting dummy pads may compromise the ESD protection of the LCD module.

## 5.9 External ESD protection

The previous design measures were all basically free of charge and involved only common, good engineering practice. Sometimes however, increasing robustness involves adding material or components which results in increased cost price. An example is adding external ESD protection.

Adding external ESD protection can be a countermeasure in cases where a display driver fails to meet severe ESD requirements, e.g. it suffers permanent damage. This is not common and therefore external ESD protection won't be necessary in most applications.

NXP LCD drivers are provided with internal ESD protection structures. An example is given in Fig 15. These internal structures ensure that the device withstands discharges as specified under the HBM, CDM and MM specs in the datasheet.

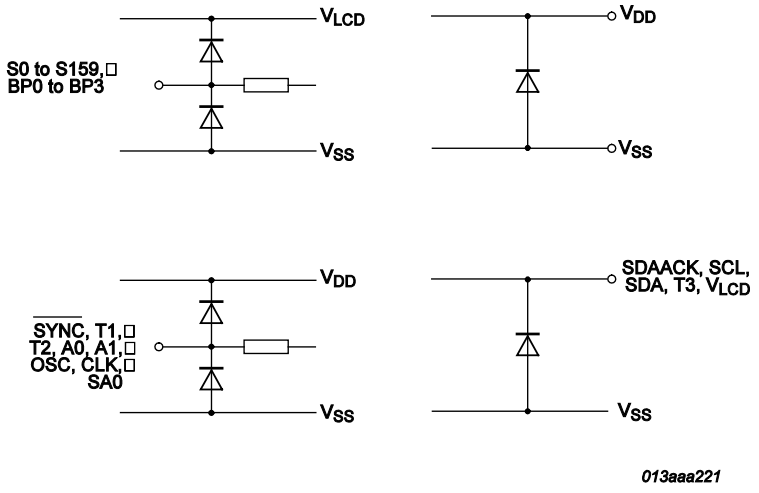



**Fig 15. Example of a device protection diagram**

This diagram shows clearly that the segment and backplane outputs are clamped between $V_{SS}$ and $V_{LCD}$. At first sight this limits the voltage excursions on the outputs to roughly ($V_{SS}$ – 0.7 V) and ($V_{LCD}$ + 0.7 V). However, during an ESD event, the rise time is that fast, that inductance of PCB tracks plays an important role. The inductance of a PCB track is given by the following equation

$$L_{track} = 200l \cdot \ln\left(\frac{2\pi h}{w} + 1\right) \quad [nH]$$

Here; l = length [m], h = height (thickness) [m], w = track width [m]

A single PCB track easily has an inductance L = 10 nH/cm. The voltage across an inductance is given by

$$U_L = L\frac{dI}{dt}$$

Assuming:

- A track length of 1 cm, resulting in L ≈ 10 nH.
- An IEC 61000-4-2 Class 2 pulse, 4 kV.
- ITO track resistance will be something in the order of 150 Ω + backplane / segment line ($R_{LCD\_COMON}$ + $R_{LCDOUT}$ + $R_{BP/SEG}$).
- ITO track resistance of 1 kΩ for the line from display element to LCD driver.

Now the resulting peak currents can be up to ca. 4 A, combined with a rise time of 1 ns. In this case the voltage over the 1 cm track can be as much as 40 V.

In Fig 16 an output of the LCD driver is depicted together with the internal clamping diodes and decoupling capacitor $C_{DECOUP}$. All inductances are parasitic due to PCB tracks and component leads (no component leads if SMDs are used). Without the external clamping, diodes $D_1$ and $D_2$ are not present and neither are $L_4$, $L_5$, $L_6$ and $R_{EXT}$. A positive discharge current arriving from the display (refer Fig 13) will enter the IC at its output pin(s) and leave the IC via the upper internal clamping diode via pin $V_{LCD}$. The current will further flow via $L_1$ (track), $C_{DECOUP}$, $L_3$ and $L_2$ to GND. The decoupling capacitor will absorb the charge and for a normal value of 100 nF to 1 µH, the voltage change on the capacitor will be very small. However, the voltage excursion during the ESD event can be much higher due to the parasitic inductance. The larger are the values of these parasitic inductances, the larger is the voltage excursion on the LCD driver output. This increases the risk of damage and this also explains why the decoupling capacitors must be placed as close to the supply pins as possible, with short connecting traces.

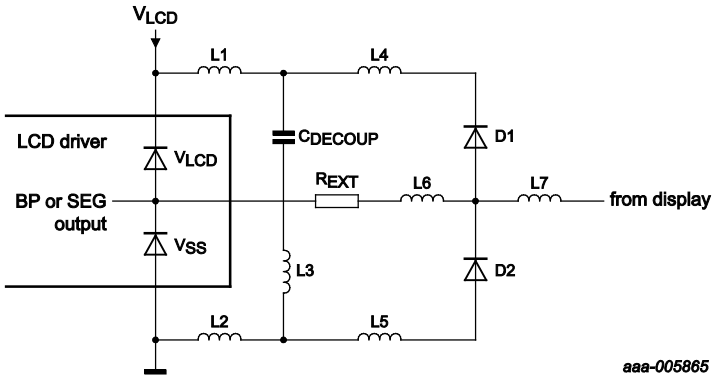



**Fig 16. Display driver output protection with external clamping diodes**

If a device is damaged due to ESD, adding external ESD diodes like indicated ($D_1$ and $D_2$ along with an external resistor $R_{EXT}$) will help to avoid this. Now the ESD current will flow via $D_1$ and $L_4$ to the decoupling capacitor for a positive pulse and via $D_2$ and $L_5$ for a negative pulse. The same considerations as before are still valid, so $L_4$ and $L_5$ must be kept as low as possible which translates to short tracks. Adding an external resistor, $R_{EXT}$, will help to make the current flow via the external clamping network. $L_6$ is parasitic and at this position a larger value is better. Adding an inductive bead instead of a resistor is an option. The higher the value of $R_{EXT}$, the more it may impact the display quality. This depends on the value of the display capacitance. For a larger display capacitance, the driving resistance must be smaller.

In most cases no external ESD protection is required, but for applications where users can touch the display directly and may be charged to high voltages, external ESD protection will help if the tests are not fulfilled with only the internal protection. The value of $L_7$ is not relevant for the ESD protection.

## 5.10 Adding output filters

Immunity for EM fields can sometimes be improved by adding filters in the outputs. This can also improve ESD robustness, but here the focus is on EMI. When injecting noise in both a segment and a backplane the segment optical performance has been seen to improve when an RC filter is connected to the affected backplane. For COG displays this is hard to do but for applications with the display driver on the PCB this can be easily realized.

In order to arrive at this recommendation, some experiments were carried out on the following segment drivers: PCF8562, PCF8576C, PCF8576D and PCF8533. Observations are also valid for derivatives of these parts. A pulse generator was used to generate noise at about 10 – 20 MHz which was injected via capacitive coupling into the system. The following observations were made:

- Noise in one segment is slightly coupled into other segments or backplanes. Amplitude however, is reduced by roughly a factor 5
- Noise and disturbances in backplanes hardly affect the optical contrast of the display. The effect of noise in segments is clearly visible in loss of contrast.
- The effect of noise coupled into just one segment or backplane is also an increased power consumption. The intermediate bias levels start to decrease. This decrease of bias levels is seen in all segments and backplanes, not only in the one that the noise was coupled into. This means that the output buffers are affected and with them all segments and backplanes.
- Decoupling to ground (filtering) on the segment lines where noise is applied, solves the problem but this would imply adding filters to all segment outputs, which results in increased cost and requires more PCB space.
- A positive effect has been seen when decoupling through a different backplane or segment than the one where the noise is injected. Therefore, adding a filter in the backplane outputs also improves immunity and this limits the number of filters to four or eight. It could be less too, depending on the multiplex rate that is used.
- From this also follows, that placing the display further away from the driver reduces the immunity. The longer the tracks, the easier it picks up an external field.

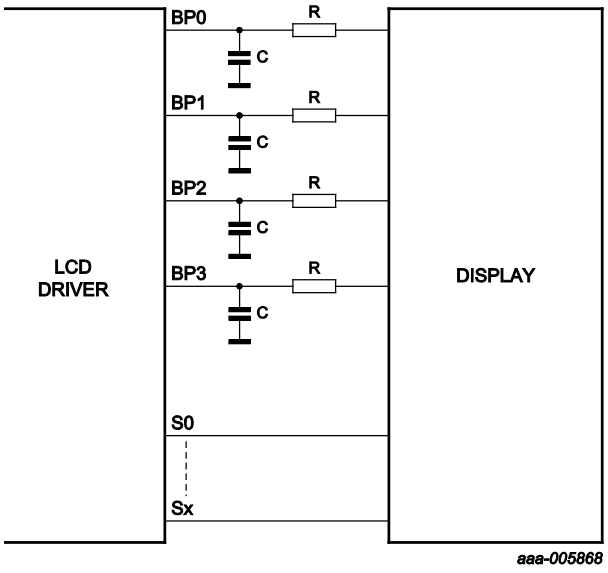



**Fig 17. Adding filters to the backplane outputs**

The capacitor and resistor values must be experimentally determined. As a first indication, C can be in the range from 1 nF to 1.8 nF and R in the order of 1 kΩ. The effect on the display under normal circumstances must be verified as well. The capacitors must be placed close to the IC with short connections to $V_{SS}$. Proper decoupling of $V_{DD}$ and $V_{LCD}$ is a prerequisite.

A ground plane under the LCD driver to which the decoupling can be done is advantageous.

## 5.11 Shielding

Shielding attempts to divert the EM-fields or ESD currents away from the internal circuitry. However, it still exposes the external conductive connections and the internal circuits as well to indirect ESD injection via ground lift. The latter is especially true with COG modules as the ITO track resistances can't be ignored.

In general it can be stated that COG applications are less immune. However, also with COG-modules good immunity can be achieved, but from the start it is usually better with a separate LCD and the display driver in a package. One reason for this is the increased resistances in the Vss line. Another reason is, that a metal bezel is often omitted in COG applications because it is not required for mechanical reasons. Therefore it is omitted in order to reduce cost. A conventional LCD, where the connections between the LCD and the PCB are made using zebra connectors, is firmly held in place with a metal bezel enclosing the display, see Fig 18.

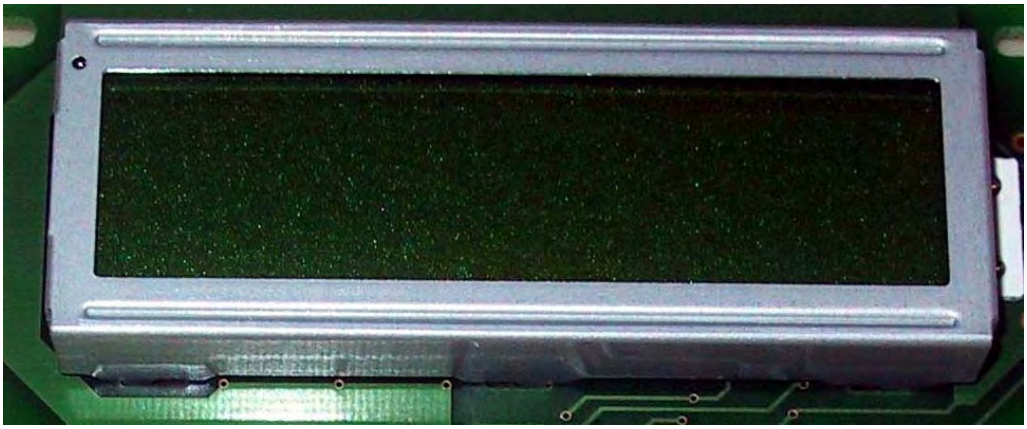


Fig 18. LCD with metal bezel

The metal bezel, which is used in LCD applications with the driver somewhere on the board, provides also shielding for EMI and ESD, provided that it is connected to GND.

Adding a similar shielding to a COG-module results in considerable improvements in immunity. It depends on the end application whether this is necessary.

With regards to EMC, COG-modules have the advantage that connections between the active display area and the display driver are short. Short connections result in less pickup by the segment and backplane lines, and this has a positive impact on immunity. Therefore the statement “COG displays are less immune” is not entirely true. It is the fact that often a bezel is omitted which may create the problem. When the bezel or a similar shielding is added, very good immunity can be achieved. A further advantage is the reduction in interconnections which results in improved reliability.

Experience has shown that just shielding the LCD driver only gives small improvements in immunity. If shielding is implemented the most effective is to surround the entire display and connect the ring to PCB ground. The picture in Fig 19 shows an experimental shielding with copper foil added such, that the display is covered on top and bottom with the shield extending over the edges of the display. In a practical realization this can be achieved with a U-shaped metal profile which fits nicely around the display, covering top and bottom, and which then is folded such that the entire display is enclosed. Important is to provide short connections to PCB ground from this ring. Obviously this shielding ring takes up some space. Therefore it should be taken into account when designing the plastic holder for display and backlight. Also it may cover part of the active area of the display. This can be avoided by increasing glass dimensions such that the active area is not covered by the metal shielding.

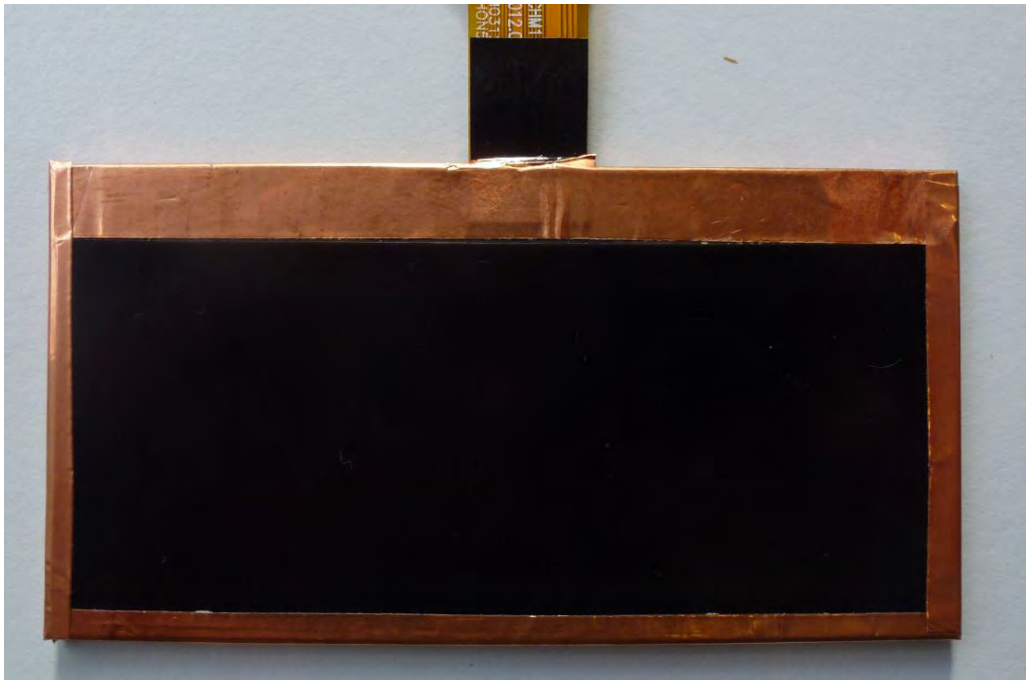


Fig 19. COG module with shielding around the module

In certain demanding applications like automotive, experience learns that often additional shielding like this ring is necessary in order to pass all tests. When the design is made with the shielding ring from the start, the additional cost is just the ring. If only in a late stage of development, the need for additional shielding is identified, this will not only lead to problems in keeping the time schedule, but also to additional cost for redesign of the plastic holder and even new manufacturing tools.

The connection between COG module and PCB is made using a Flexible Printed Circuit (FPC). It is advisable to keep the length of this foil connector short, no longer than necessary. Adding a second grounded layer on the other side of the FPC hardly brings an improvement. Therefore it also can be concluded that the FPC is not the weak link. The biggest contribution in improving the immunity for both EMI and ESD is the shielding ground ring as discussed before.

### 5.11.1 LCD Emissions

Most problems encountered with passive LCDs are immunity problems, but sometimes also emissions can create problems. With added functionality in the LCD driver, like integrated charge pumps to generate $V_{LCD}$, also the risk of exceeding emission limits increases. Often the problem can be traced back to the flex cable between the circuit board and the LCD-module, see Fig 20. The currents going up to the LCD do not all return via the same cable. A small fraction remains as a common mode current, exciting from the LCD.

Some steps can be taken in this case. First, the currents need to be returned to the source (the PCB) with a loop area as small as possible. This can be achieved by adding direct shunts from the LCD back to the PCB. The metal bezel or metal shield as discussed above does just this. Its effectiveness increases if the connections can be made at all four corners instead of just at one place. A ground plane under the LCD, to which the metal shield can be connected, is very useful in reducing emissions coming directly from the LCD.

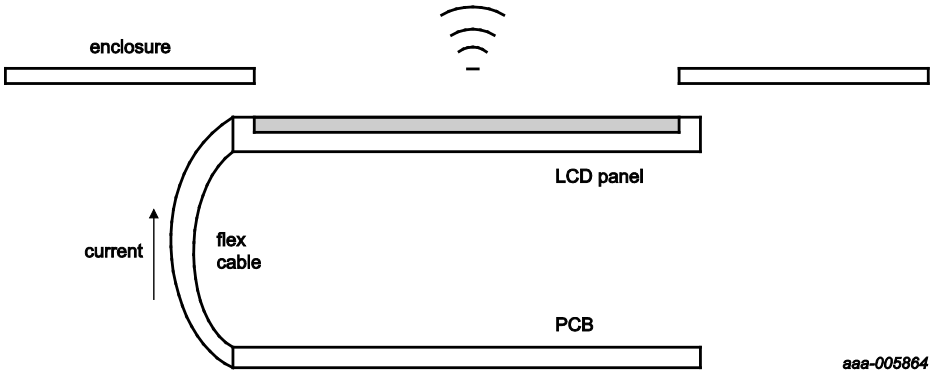



**Fig 20. Emissions from LCD**

# 6. Software design measures

Besides hardware measures which often result in increased Bill Of Material (BOM) cost, it is possible to implement measures to deal with EMI and ESD in software. Software or firmware can be an efficient way to recover from non-destructive ESD events and EMI. As with hardware measures also software measures have their associated costs, e.g. increased development time and possibly increased memory requirements. However, the software measures that can be taken to make an LCD application more robust come at virtually no extra cost. The internal state of a display driver can be changed when exposed to external noise, whether this is due to strong HF fields or an ESD, which also contains high frequency components, as discussed before. Some measures that can be taken in the software will be discussed below.

## 6.1 Refreshing

Do not just write the configuration registers and display RAM once, but refresh them periodically in an endless loop. Determining the optimal refresh rate involves a compromise between fast corrections in case that RAM content or register settings are accidentally changed, and the statistical chance that the communication between the microcontroller and the LCD driver gets corrupted due to disturbance. The more often configuration settings and data are refreshed, the more likely that (at some point) the

communication is affected by external noise or an ESD event. This could be for example by incorrectly interpreting a 1/0 level, by adding another clock or by creating a false START or STOP condition. At the same time, when this happens, the effect will also last less long, if the next refresh comes quickly. As a starting point once every 100 ms could be used, but the actual refresh frequency chosen is determined by other tasks the software has to execute and depending on the application. Several factors have to be considered in this case.

## 6.2 Write to all configuration registers

Write and refresh all configuration registers, also those whose default state after reset is as desired in the application. This could be treated as excessive, but it isn't, because one of these registers can be affected as well. Therefore it is recommended to also initialize and refresh these configuration registers.

## 6.3 Use the Acknowledge bit and act if a NACK is received

Many NXP LCD-drivers communicate with the microcontroller via the $I^2C$-bus. Don't ignore the ACK (Acknowledge) and NACK (Non Acknowledge) during $I^2C$ communication.
Some features of the $I^2C$-bus are:

- Only two bus lines are required; a serial data line (SDA) and a serial clock line (SCL).
- All devices connected to the bus must use open drain or open collector outputs, thus performing the Wired OR function. Never use push-pulls as this could lead to conflicts and short circuits on the bus.
- Each device connected to the bus is software addressable by a unique address and simple master/slave relationships exist at all times. Masters can operate as master-transmitters or as master-receivers.
- Serial, 8-bit oriented, bidirectional data transfers can be made at up to 100 kbit/s in the Standard-mode, up to 400 kbits/s in the Fast-mode, up to 1 Mbit/s in Fast-mode Plus, or up to 3.4 Mbit/s in the High-speed mode.
- On-chip filtering rejects spikes on the bus lines to preserve data integrity.

All transactions begin with a START (S) and can be terminated with a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. The START and STOP conditions are the only occasions where the SDA line is allowed to change while SCL is HIGH. The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight data bits is followed by an acknowledge cycle. Therefore nine clock cycles are used to transmit a data byte.

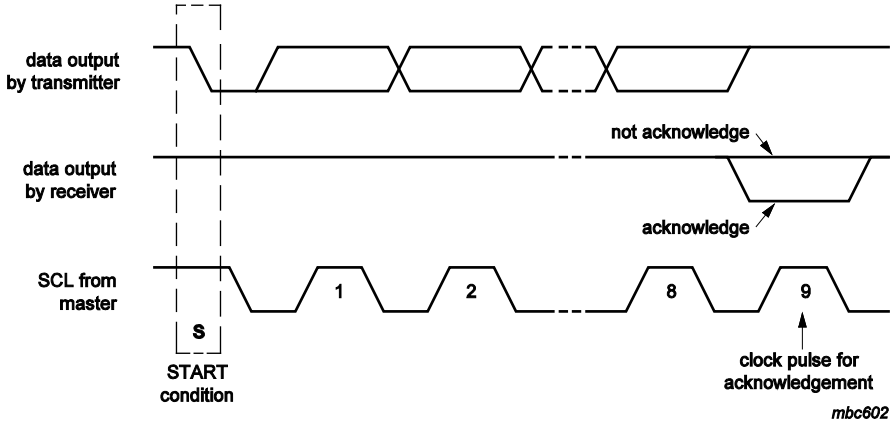



**Fig 21. START condition and ACK / NACK**

The Acknowledgement takes place after every byte. The Acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses including the 9$^{th}$ clock pulse are generated by the master.

The Acknowledge signal is defined as follows: The transmitter releases the SDA line during the acknowledge clock pulse so the receiver (the LCD driver) can pull the SDA line LOW and it remains stable LOW during the HIGH period of the clock pulse. This is visualized in Fig 21. When SDA remains HIGH during this 9$^{th}$ clock pulse, this is defined as the Not Acknowledge signal (NACK). There are five conditions that lead to the generation of a NACK:

1. No receiver is present on the bus with the transmitted address so there is no device to respond with an Acknowledge.
2. The receiver is unable to receive or transmit because it is performing some real-time function and is not ready to start communication with the master.
3. During the transfer the receiver gets data or commands that it does not understand. This could happen due to an ESD event or due to disturbance caused by EMI.
4. During the transfer, the receiver cannot receive any more data bytes.
5. A master-receiver needs to signal the end of the transfer to the slave transmitter.

In the context of this application note, condition 3 is important. In a well designed application, communication between the microcontroller and LCD driver will operate without generating a NACK under normal conditions. Disturbance due to EMI or ESD could lead to the generation of a NACK. A NACK is simple to explain in terms of the interface state machines failing or receiving extra clocks. It could easily be, that the ACK phase coming from the LCD driver is one clock too early in the eyes of the microcontroller, i.e. the chip has received an extra clock due to the ESD event. The microcontroller only 'knows' the clocks it is sending, but a disturbance due to an ESD event got interpreted by the driver as an extra clock, and therefore the driver sent an acknowledge before the microcontroller expected it. The microcontroller then does not see it. This is more likely than that the chip is changing state, i.e. the state machine jumping to a different state (flip flops changing state as a result of a strike).

When a NACK is received, the software can ignore this and continue communication as if nothing had happened. Much better would be, if a NACK leads to the master generating a STOP condition to abort the transfer, or a repeated START (R) to start a new transfer.

The best way to deal with a NACK in order to have the display recover as quickly as possible is:

1. Upon receiving a NACK, send a repeated START condition.
2. Assume that any configuration bit or data bit could be corrupted. Therefore refresh all configuration registers and the Display RAM (DRAM).
3. After this, the normal refresh cycle, as discussed before, will take over again.

The ACK cycle is part of the $I^2C$ protocol. Some of NXP's LCD drivers communicate via the SPI bus. It is more difficult to detect a communication error with it, but some recently introduced LCD drivers have a 'status read function' which assists in detecting abnormal or unintended states of the LCD driver.

Not only the LCD driver can be affected by an ESD event. It could as well be the microcontroller which controls the LCD driver. Therefore it is important to also verify proper functionality of the microcontroller under all circumstances.

# 7. Abbreviations

A glossary of used terms is given below.

**Table 5. Abbreviations**

| Acronym | Description |
|---|---|
| AEC | Automotive Electronics Council |
| CDM | Charged Device Model |
| CE | Conducted Emissions |
| COB | Chip-On-Board |
| COG | Chip-On-Glass |
| DUT | Device Under Test |
| EFT | Electrical Fast Transient |
| EMC | ElectroMagnetic Compatibility |
| EME | ElectroMagnetic Emission |
| EMI | ElectroMagnetic Interference |
| EMS | ElectroMagnetic Susceptibility |
| ESD | ElectroStatic Discharge |
| EUT | Equipment Under Test |
| FPC | Flexible Printed Circuit |
| HBM | Human Body Model |
| HCP | Horizontal Coupling Plane |
| I/O | Input/Output |
| ITO | Indium Tin Oxide |
| IC | Integrated Circuit |
| $I^2C$ | Inter-Integrated Circuit |
| LCD | Liquid Crystal Display |
| LSB | Least Significant Bit |
| MM | Machine Model |
| MSB | Most Significant Bit |
| PCB | Printed Circuit Board |
| POR | Power On Reset |
| RAM | Random Access Memory |
| RE | Radiated Emissions |
| RF | Radio Frequency |
| SCL | Serial CLock line |
| SDA | Serial DAta line |
| SMD | Surface Mount Device |
| SMT | Surface Mount Technology |
| STN | Super Twisted Nematic |
| TN | Twisted Nematic |
| VA | Vertical Alignment |

## 8. References

The references below provide further useful information. The first three are white papers from the “Industry Council on ESD Target Levels” which is made up of several semiconductor manufacturers and OEMs. The white papers can be easily found on the internet using a suitable search engine.

[1] **White Paper 1: A Case for Lowering Component Level HBM/MM ESD Specifications and Requirements**, Industry Council on ESD Target Levels.

[2] **White Paper 2: A Case for Lowering Component Level CDM ESD Specifications and Requirements**, Industry Council on ESD Target Levels.

[3] **White Paper 3: System Level ESD. Part I: Common Misconceptions and Recommended Basic Approaches**, Industry Council on ESD Target Levels.

[4] **IEC 61000-4-2:** Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge.

[5] **IEC 61000-4-4:** Electromagnetic compatibility (EMC) – Part 4-4: Testing and measurement techniques – Electrical fast transient/burst immunity test.

[6] **IEC 61000-4-6:** Electromagnetic compatibility (EMC) – Part 4-6: Testing and measurement techniques – Immunity to conducted disturbances, induced by radio-frequency fields.

[7] **AN10897**: A guide to designing for ESD and EMC.

[8] **AN10853**: ESD and EMC sensitivity of IC.

[9] **AN10170**: Design guidelines for COG modules with NXP monochrome LCD drivers

[10] **UM10204**: $I^2C$-bus specification and user manual.

[11] **AN10706**: Handling bare die

[12] **R_10015**: Chip-On-Glass (COG) – a cost-effective and reliable technology for LCD displays

[13] **Electromagnetic Compatibility Engineering**, Henry W. Ott, Wiley, August 24, 2009.

[14] **Electromagnetic Compatibility**, J.J. Goedbloed, Prentice Hall, February 1993.

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