AN11001

CBTL02042A switching application for mSATA and PCI Express Mini-Card

Rev. 1 — 7 March 2011

Application note

Revision history

Rev	Date	Description
v.1	20110307	application note; initial release

Contact information

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1. Introduction

NXP's CBTL02042A (shown in Figure 1) is a 3.3 V, 2-to-1 multiplexer/de-multiplexer specially designed for switching between PCIe Gen 2 (up to 5 Gbit/s) and SATA Gen 2 (up to 3 Gbit/s) signals, with features such as low insertion loss (−1.2 dB at 2.5 GHz), low crosstalk (−30 dB at 2.5 GHz), and low operating power consumption (< 1 mA). A motherboard manufacturer can use CBTL02042A for multiplexing between PCIe Gen 2 and SATA signals connecting to an mSATA/Mini-Card socket. This document discusses system level design guidelines and considerations while using CBTL02042A in a Mini-Card/mSATA sub-system.

Fig 1.   CBTL02042A functional block diagram
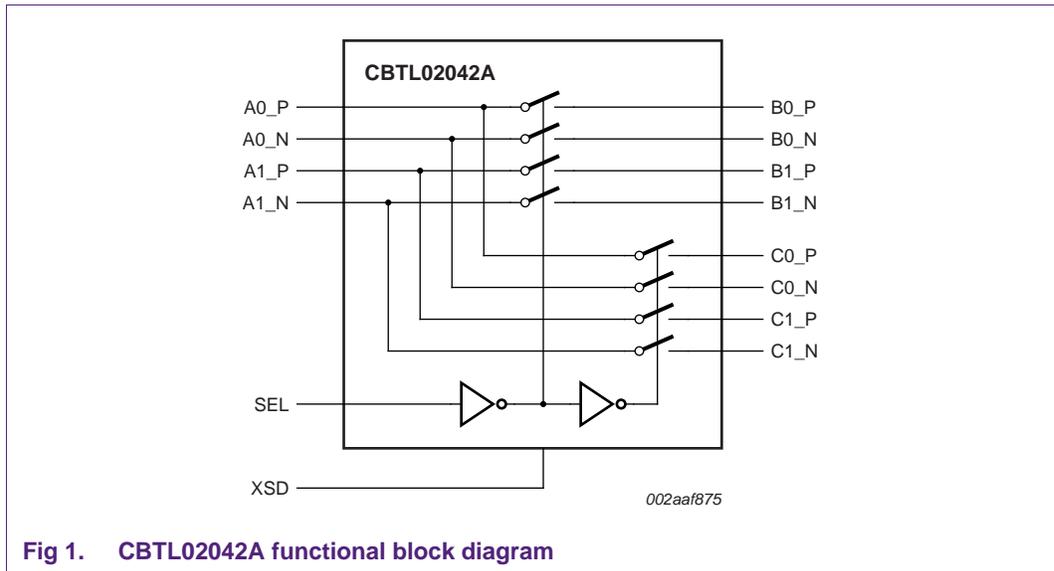
2. Mini-Card and mSATA applications

Both mSATA (from SATA-IO) and Mini-Card (from PCI SIG) share the same form-factor and similar electrical pinout assignments on their connectors. Mini-Cards are PCI Express (or PCIe)-based devices, and PCIe interface signals are accessible on the connectors. An mSATA device's connector replaces PCIe interface signals with SATA interface, but with power and ground signals assigned to the same connector pins as Mini-Card's. There was no clear mechanism to distinguish if a mSATA drive or a Mini-Card device is plugged into the socket until recently that SATA-IO issued an ECN change (ECN #45) to re-define pin 43 on mSATA connector as 'no connect' instead of 'return current path' (or GND).

Table 1.   mSATA and Mini-Card pin assignments

Pin	mSATA	Description	Mini-Card
P1	reserved	no connect	WAKE#
P2	+3.3 V	3.3 V source	+3.3 V$_{aux}$
P3	reserved	no connect	COEX1
P4	GND	return current path	GND
P5	reserved	no connect	COEX2
P6	+1.5 V	1.5 V source	+1.5 V
P7	reserved	no connect	CLKREQ#

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Table 1. **mSATA and Mini-Card pin assignments** *...continued*

Pin	mSATA	Description	Mini-Card
P8	reserved	no connect	UIM_PWR
P9	GND	return current path	GND
P10	reserved	no connect	UIM_DATA
P11	reserved	no connect	REFCLK−
P12	reserved	no connect	UIM_CLK
P13	reserved	no connect	REFCLK+
P14	reserved	no connect	UIM_RESET
P15	GND	return current path	GND
P16	reserved	no connect	UIM_VPP
P17	reserved	no connect	reserved (UIM_C8)
P18	GND	return current path	GND
P19	reserved	no connect	reserved (UIM_C4)
P20	reserved	no connect	W_DISABLE#
P21	GND	return current path	GND
P22	reserved	no connect	PERST#
P23	+B	host receiver differential signal pair	PERn0
P24	+3.3 V	3.3 V source	+3.3 V$_{aux}$
P25	−B	host receiver differential signal pair	PERp0
P26	GND	return current path	GND
P27	GND	return current path	GND
P28	+1.5 V	1.5 V source	+1.5 V
P29	GND	return current path	GND
P30	Two Wire Interface	two-wire interface clock	SMB_CLK
P31	−A	host transmitter differential signal pair	PETn0
P32	Two Wire Interface	two-wire interface data	SMB_DATA
P33	+A	host transmitter differential signal pair	PETp0
P34	GND	return current path	GND
P35	GND	return current path	GND
P36	reserved	no connect	USB_D−
P37	GND	return current path	GND
P38	reserved	no connect	USB_D+
P39	+3.3 V	3.3 V source	+3.3 V$_{aux}$
P40	GND	return current path	GND
P41	+3.3 V	3.3 V source	+3.3 V$_{aux}$
P42	reserved	no connect	LED_WWAN#
P43	no connect	no connect indicates mSATA use	GND
P44	reserved	no connect	LED_WLAN#
P45	Vendor	vendor specific / manufacturing pin	reserved
P46	reserved	no connect	LED_WPAN#
P47	Vendor	vendor specific / manufacturing pin	reserved
P48	+1.5 V	1.5 V source	+1.5 V

Table 1. **mSATA and Mini-Card pin assignments** *…continued*

Pin	mSATA	Description	Mini-Card
P49	DA/DSS	Device Activity signal / Disable Staggered Spin-up	reserved
P50	GND	return current path	GND
P51	Presence Detection	shall be pulled to GND by device	reserved
P52	+3.3 V	3.3 V source	+3.3 V$_{aux}$

This ECN change enables a card-type detection mechanism by adding a pull-up resistor on pin 43 on the socket. When an mSATA drive is inserted, its pin 43 is 'no connect', and the respective pin on the socket is being pulled-up to logic 1. When a Mini-Card device is inserted, its pin 43 forces the respective pin on the socket to ground, or logic 0. The host processor (or CPU) can utilize this information to enable either a SATA or a PCIe host controller on a notebook motherboard. Figure 2 illustrates a typical block diagram of Mini-Card/mSATA sub-system implementation using CBTL02042A.

Table 2. **Pin 43 statuses while different devices inserted**

Device inserted	PCIe Mini-Card	mSATA drive
Pin 43 status	logic 0	logic 1

019aaa989
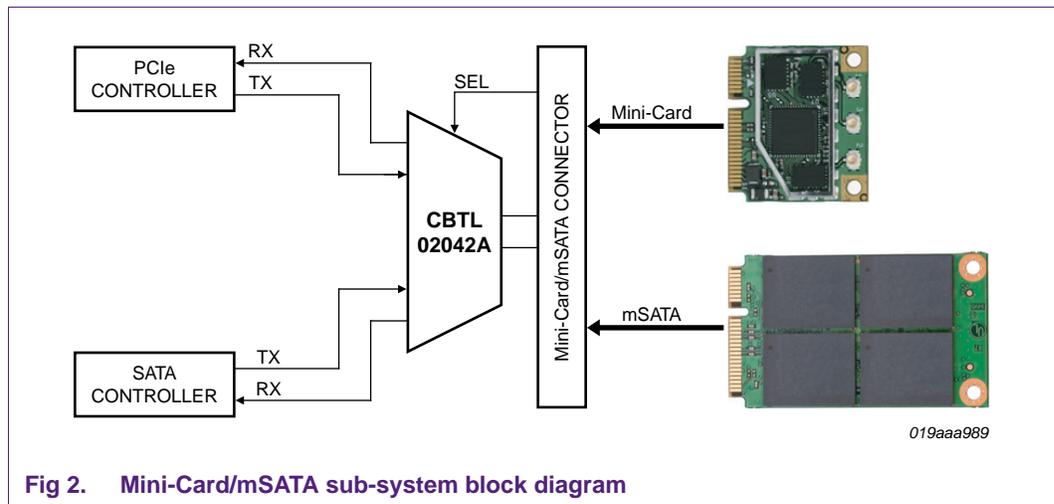
Fig 2. **Mini-Card/mSATA sub-system block diagram**

3. Switching circuit schematic

Figure 3 illustrates circuit schematics of Mini-Card/mSATA connector socket, CBTL02042A, and connections to PCIe and SATA host controllers (shown as transmitter and receiver symbols). Pins 3, 4, 7, and 8 (connector-side port) of CBTL02042A are differential pair signals connecting to the connector socket. Based on the logic level of the SEL signal, the port on the connector side will connect either to pins 19, 18, 17, and 16 (SEL_0_Port) when SEL = 0, or to pins 15, 14, 13, and 12 (SEL_1_Port) when SEL = 1. Information in Table 2 institutes the circuit diagram such that SEL_0_Port should be connected to a PCIe host controller, and SEL_1_Port should be connected to a SATA host controller.
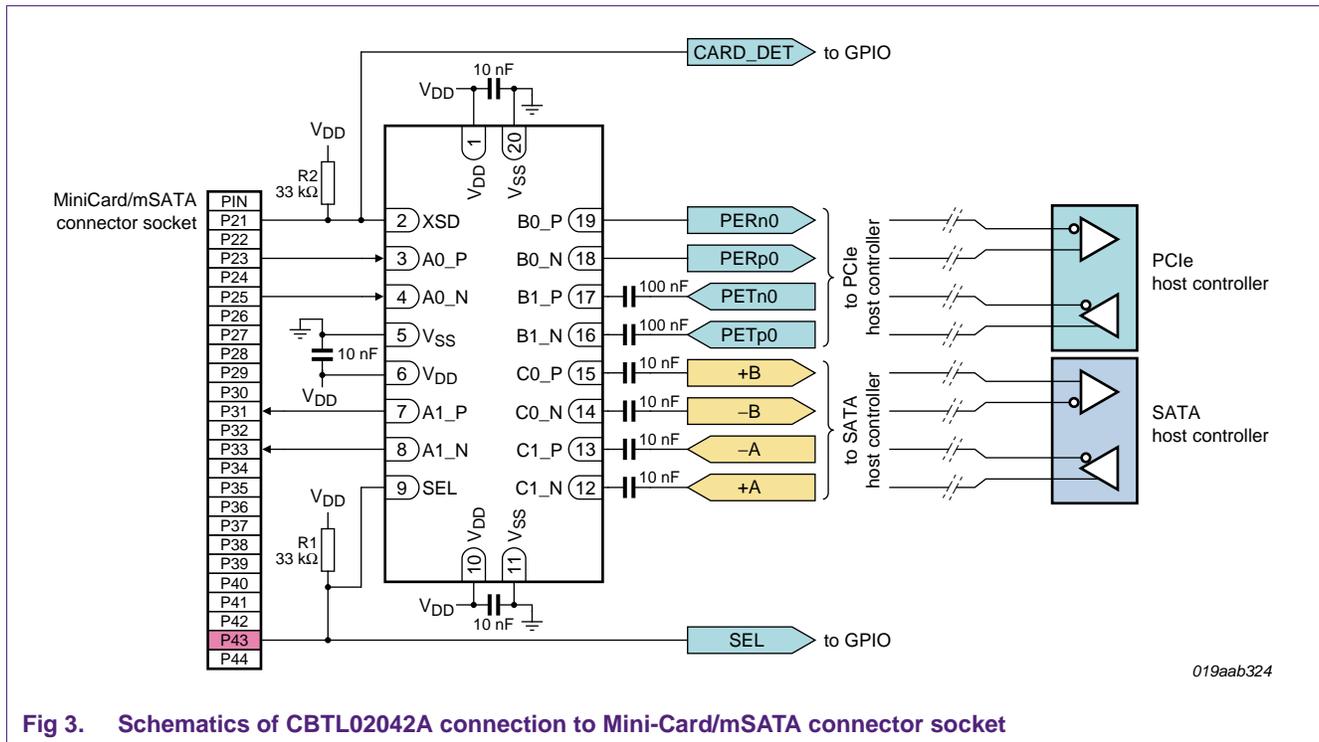

Fig 3. Schematics of CBTL02042A connection to Mini-Card/mSATA connector socket

In Figure 3 above, the XSD pin (pin 2) of CBTL02042A is connected to pin 21 of the connector with a 33 kΩ pull-up resistor. The purpose of this pin is to detect if there is a Mini-Card or an mSATA device inserted to the connector, similar to a card detect signal found in most card-based sub-systems. Pin 21 is chosen such that this pin is grounded on the device side. When there is no device inserted in the connector socket, the state of XSD pin (and 'CARD_DET' signal) is HIGH. This signal can be used to notify the chip set that no device is inserted, PCIe and mSATA functions for this Mini-Card/mSATA sub-system can be disabled, and CBTL02042A is placed under Shutdown mode to conserve power. On the contrary, when a device is inserted, 'CARD_DET' signal is being grounded by the device, and logic level of zero forces CBTL02042A to resume in normal operating mode. The schematics might be modified to connect 'CARD_DET' signal to any other pin that is being assigned as ground on the connector.

4. Mini-Card/mSATA routing guidelines (summary)

High-speed signals on Mini-Card and mSATA devices are listed in Table 3. PCB design must follow general guidelines of these high-speed signals as suggested by the chip set manufacturer. This section briefly discusses these guidelines.

Table 3.   Mini-Card/mSATA high speed signals

Card type	Signal name	Description
Mini-Card	PETp0, PETn0	PCI Express Tx differential pair
	PERp0, PERn0	PCI Express Rx differential pair
mSATA	+A, −A	SATA Tx differential pair
	+B, −B	SATA Rx differential pair

4.1 PCI Express routing guideline (without multiplexer in topology)

The Mini-Card topology supports up to four vias for each transmit or receive differential signal, with maximum of 10 inches (25.4 cm) of trace length from chip set pin to the Mini-Card connector. Maximum trace length includes all routing sections, including breakout region from the chip set, main route, and breakout region to the connector. Length mismatch within the differential pair should not exceed 5 mils. If signals can be routed without switching to a different layer, less vias will be used, and impedance change of the differential pairs can be avoided as well.

Figure 4 illustrates the required routing for PCI Express differential signals from chip set to a Mini-Card connector. The PCIe interface is an x1 link and can be routed to different devices at varied locations of the board, it is practical to route TX signals and RX signals of each link next to each other on the same PCB layer.

- Total trace length from chip set pin to Mini-Card connector should not exceed 10 inches (25.4 cm). If at all possible, it is recommended to route the signals on the top layer with no vias.

- Maximum main route length should not exceed 8 inches (20.32 cm), and should include maximum of one via in the main route region for each signal. Route the main route signals on the PCB top layer if possible so that the trace can be connected to AC coupling capacitors (also located on the top layer) directly.

- Trace length in the breakout area near chip set side and connector side should be limited to be less than 0.5 inch (1.27 cm). Similar to main route, maximum of one via in each breakout region is allowed.

- AC coupling capacitors with values of between 75 nF and 200 nF for the transmit signals should be located near the connector side. RX signals on the motherboard sides do not require AC coupling capacitors since those capacitors are located on the device side.
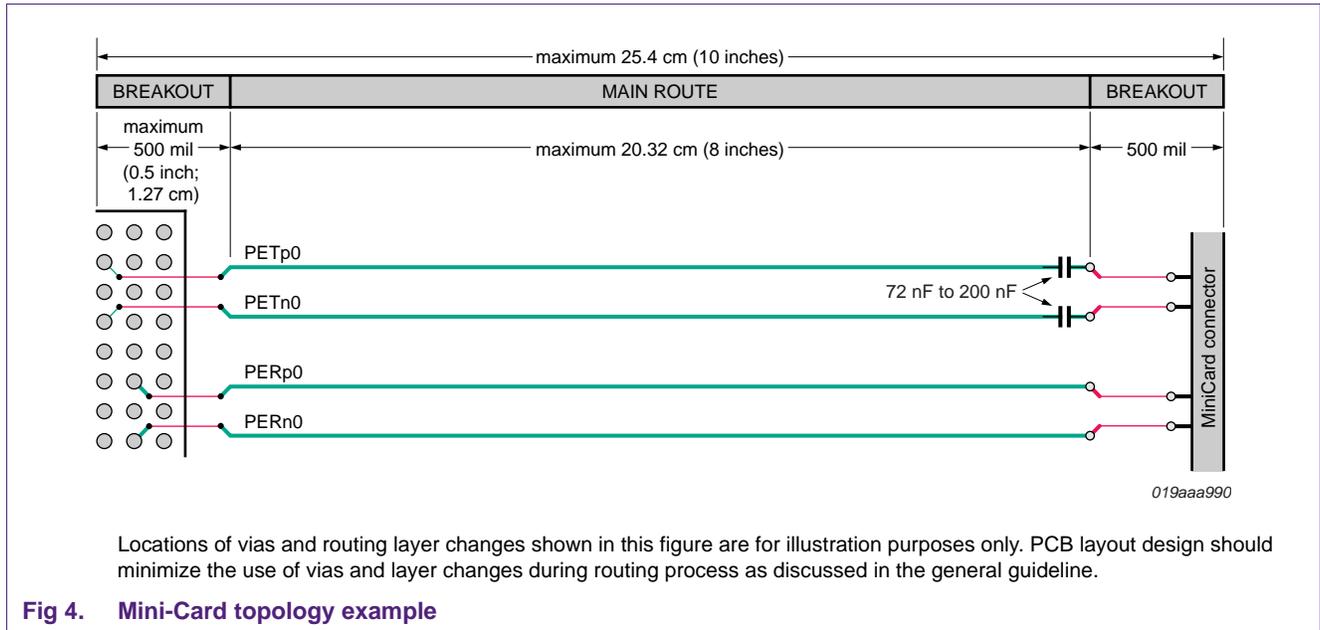
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Locations of vias and routing layer changes shown in this figure are for illustration purposes only. PCB layout design should minimize the use of vias and layer changes during routing process as discussed in the general guideline.

Fig 4.   Mini-Card topology example

4.2 SATA routing guideline (without multiplexer in topology)

General routing and placement guidelines for SATA signals are:

- SATA signals should be referenced to internal ground plane. If it is necessary to change reference to power plane (such that SATA signals are routed on the bottom layer, which is referenced to power or V_{CC} plane on PCB), capacitors with low ESR values should be placed at locations where the SATA signals are changing layers, and between power and ground planes to minimize the negative impact of EMI and signal integrity performance caused by reference plane change. These capacitors provide a high frequency current return path between different reference planes, and minimize the impedance discontinuity and current loop area that crossing different reference planes created.

- Route differential traces over a continuous ground planes with no interruptions. Routing across a split ground plane (which contains anti-etch) should be avoided.

- If a layer change is absolutely necessary, make sure the trace matching for either transmit or receive pair occurs within the same layer. It is also recommended to not to use vias whenever possible. A maximum of four vias are allowed on the path, inclusive of the though-hole via of the external connector.

- Route TX and RX pairs close to each other and on the same PCB layer with minimum mismatch of trace length within the pair. Trace length matching should be within the differential pair for each segment between points of discontinuity. Points of discontinuity could be vias, capacitor pads, or connector pins. Total length mismatch should not exceed 20 mils. It is not necessary to match the trace length of TX and RX pairs since they operate independently.

- Do not route SATA traces under power connectors, other interface connectors, crystals, oscillators, clock synthesizers, or magnetic devices that use and/or duplicate clocks.

- Route SATA signal traces away from etching areas, including pads, vias, and other signal traces. Keep minimum keep-out distance of 20 mils whenever possible.

- AC coupling capacitors should be placed close to the connector for optimal signal quality. Capacitors must be of type X7R with values of 10 nF $\pm$ 15 % and body size 0402.

- Maximum of 6 inches (15.24 cm) trace length from host controller to SATA connector is strongly suggested.

4.3 Topology with CBTL02042A as a switch for Mini-Card/mSATA

CBTL02042A, like other high-speed switches, introduces certain amount of signal loss at different frequencies. Without any switch on a PCB trace, the PCB trace itself introduces some loss as well. Although the CBTL02042A can operate up to 7 Gbit/s, this particular application mandates the operating speed of mSATA up to 3 Gbit/s (SATA Gen 2), and PCIe on the Mini-Card up to 2.7 Gbit/s (PCIe Gen1). Hence, the critical signal frequency we will be focusing on is 1.5 GHz. Typically, a signal loss of 0.25 dB exists for every 1 inch (2.54 cm) of PCB trace on FR4 material at frequency of 1.5 GHz. At this frequency, CBTL02042A exhibits signal loss of less than 1 dB, or translating to 3 inches (7.62 cm) to 4 inches (10.16 cm) of PCB trace. Keep this in mind, traces length of PCIe and SATA signals will need to be reduced by 3 inches (7.62 cm) to 4 inches (10.16 cm) when CBTL02042A is used to select either PCIe or SATA signals. Effectively, with CBTL02042A, the maximum trace length reduces from 10 inches (25.4 cm) to 7 inches (17.78 cm) for PCIe signals, and from 6 inches (15.24 cm) to 3 inches (7.62 cm) for SATA signals.

The topology of PCIe and SATA signals going to Mini-Card/mSATA connector is shown in Figure 5. Note that the CBTL02042A should be placed close to the Mini-Card/mSATA connector, with AC coupling capacitors placed on the side that is close to the host controllers, but adjacent to CBTL02042A. PCIe's RX signals (PERp0, PERn0) to the host controller do not require AC coupling capacitors on the motherboard because they are placed on the Mini-Card.
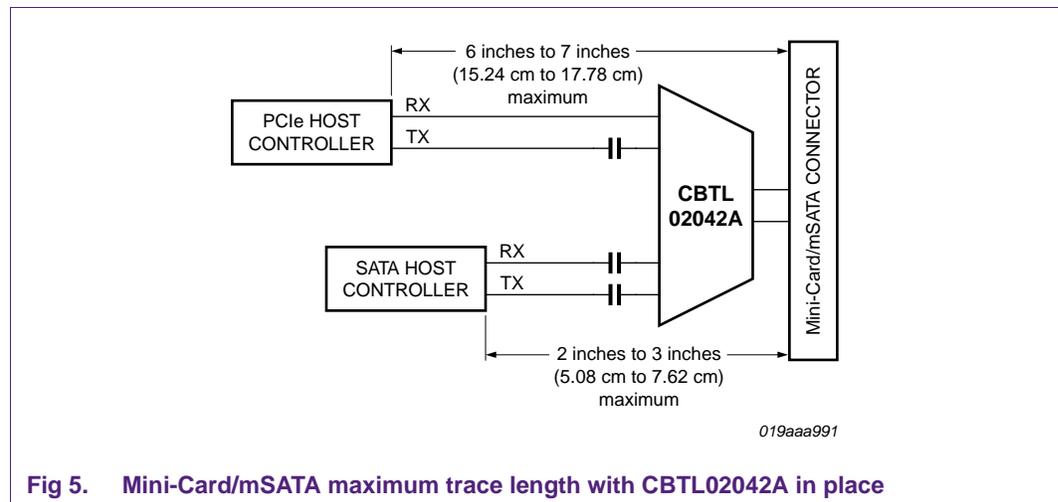

Fig 5. **Mini-Card/mSATA maximum trace length with CBTL02042A in place**

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It is recommended to minimize the use of vias and avoid impedance mismatch between traces. Also, the signal traces between the AC-coupling capacitors and the Mini-Card/mSATA connector, including those signals going through CBTL02042A, should be routed on the top layer only. Figure 6 and Figure 7 show the cross section view of the PCBs with signal path connecting from PCIe/SATA host controller to the connector. Note that the main route trace is placed on the inner signal layer in Figure 7, however it is strongly suggested for a PCB designer to route the main route on the top layer (as shown in Figure 6) by moving the second via (which is close to the AC-coupling capacitor) to the break-out region near the host controller.
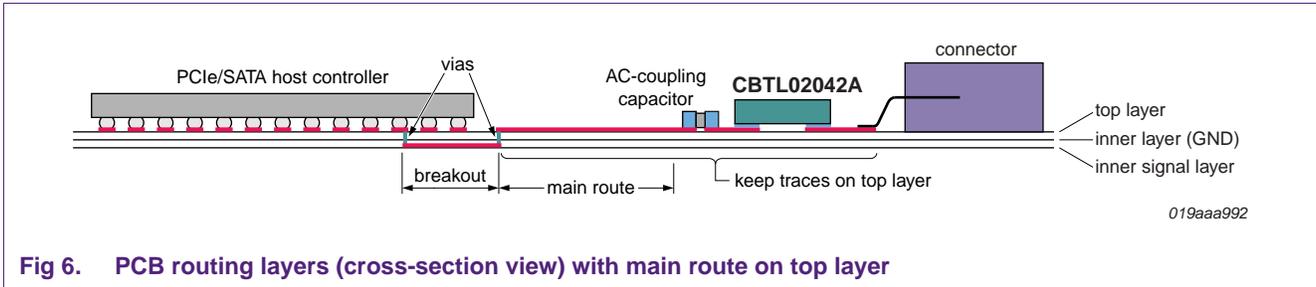
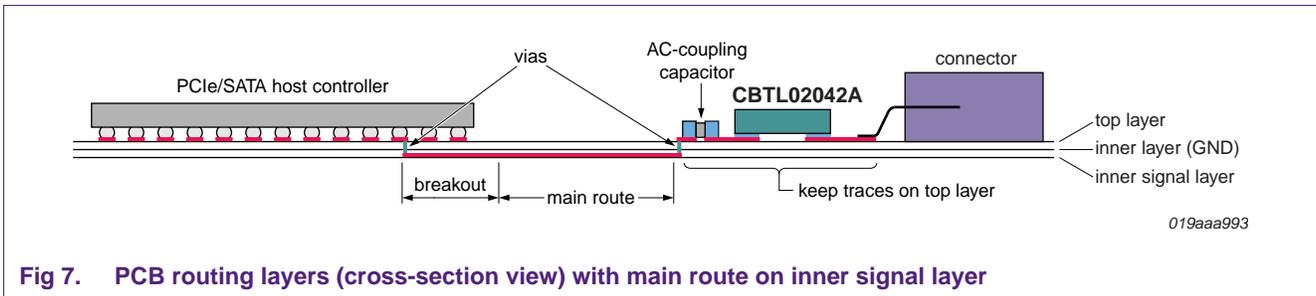**Fig 6.** **PCB routing layers (cross-section view) with main route on top layer**

Fig 7. **PCB routing layers (cross-section view) with main route on inner signal layer**

Beside the trace length changes and routing layer recommendations, a PCB designer should also follow all other layout guidelines mentioned in the previous PCIe and SATA guideline sections.

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5. Alternative design using CBTL02042A or CBTL04082A

In the design example above, only one interface is active at a time. For example, when a Mini-Card is inserted into the Mini-Card/mSATA connector socket, the PCI Express interface is selected, and the SATA interface is inactive. Instead of leaving SATA interface inactive in this configuration, a motherboard design may reclaim the SATA interface for a form-factor hard disk drive. A conceptual application diagram is shown in Figure 8 below, and it can be realized using either two CBTL02042As or one CBTL04082A/CBTL04083A.
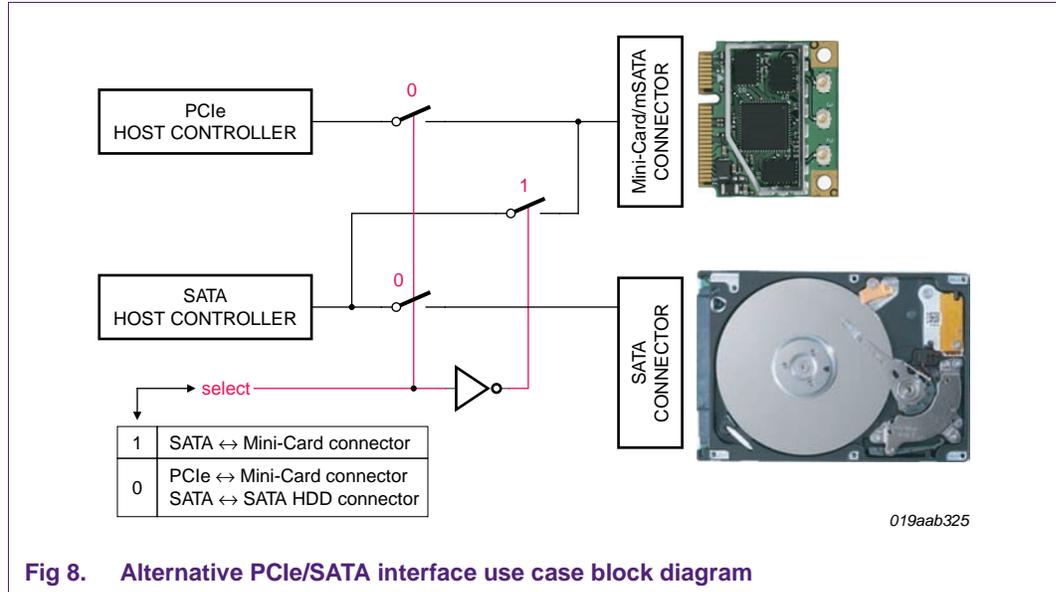
Fig 8. **Alternative PCIe/SATA interface use case block diagram**

The following paragraphs discuss the design implementation in detail. While using either topology, a designer should pay special attention to the insertion loss caused by the multiplexers, and adjust the trace length accordingly. The SATA interface signals to Mini-Card/mSATA connector go through the multiplexer twice, thus insertion loss caused by the multiplexers would need to be accounted for twice as well. From the trace length calculation discussed in Section 4.3 "Topology with CBTL02042A as a switch for Mini-Card/mSATA", a typical SATA trace length of 7 inches (17.78 cm) will need to deduct 5 inches (12.7 cm) to 6 inches (15.24 cm) to compensate the loss from the multiplexers. This only leaves 1 inch (2.54 cm) to 2 inches (5.08 cm) of SATA signal traces to route between the controller and the Mini-Card/mSATA connector. Depending on locations of the controllers and connectors on motherboards, routing such short SATA signal traces can be very difficult.
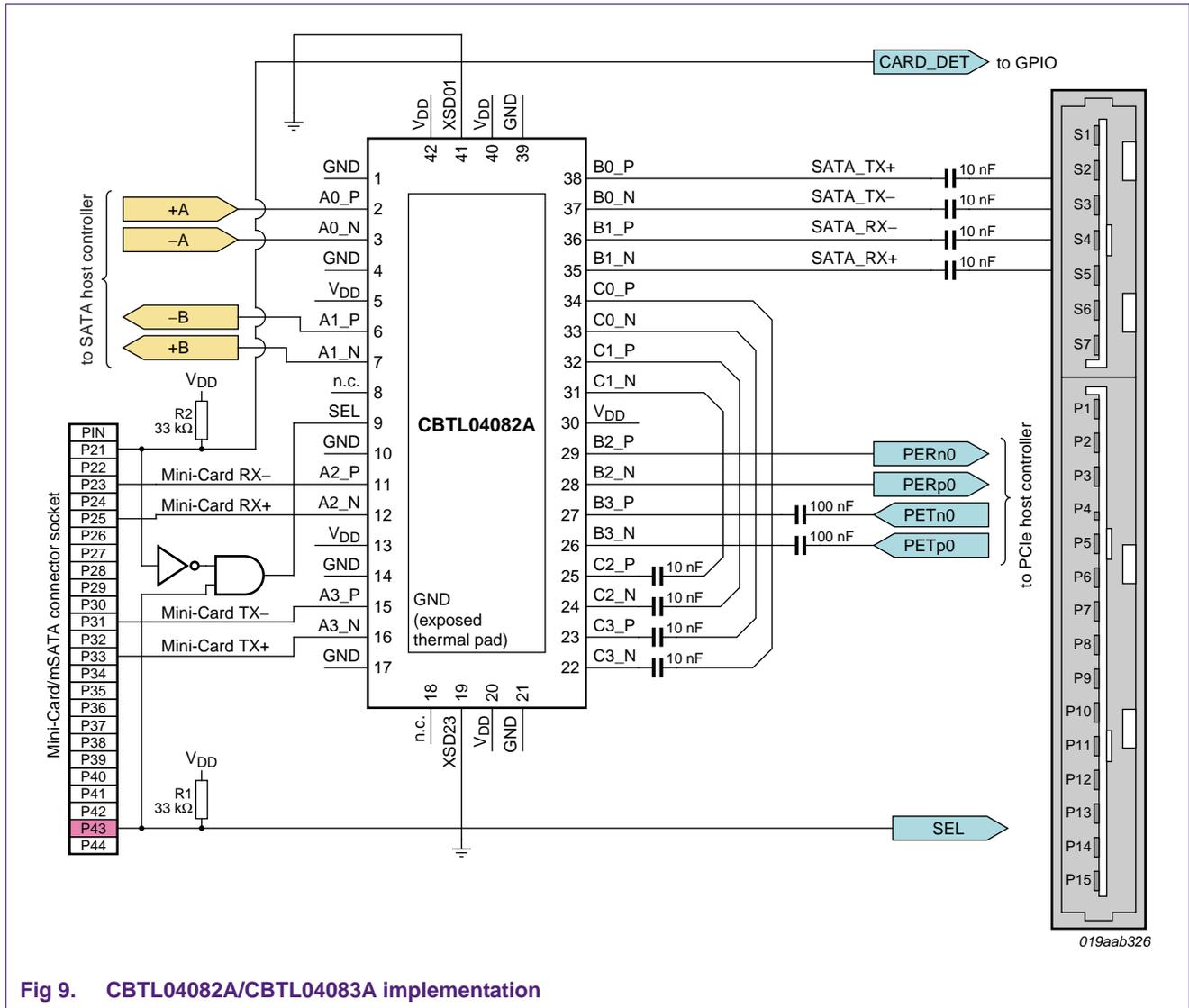
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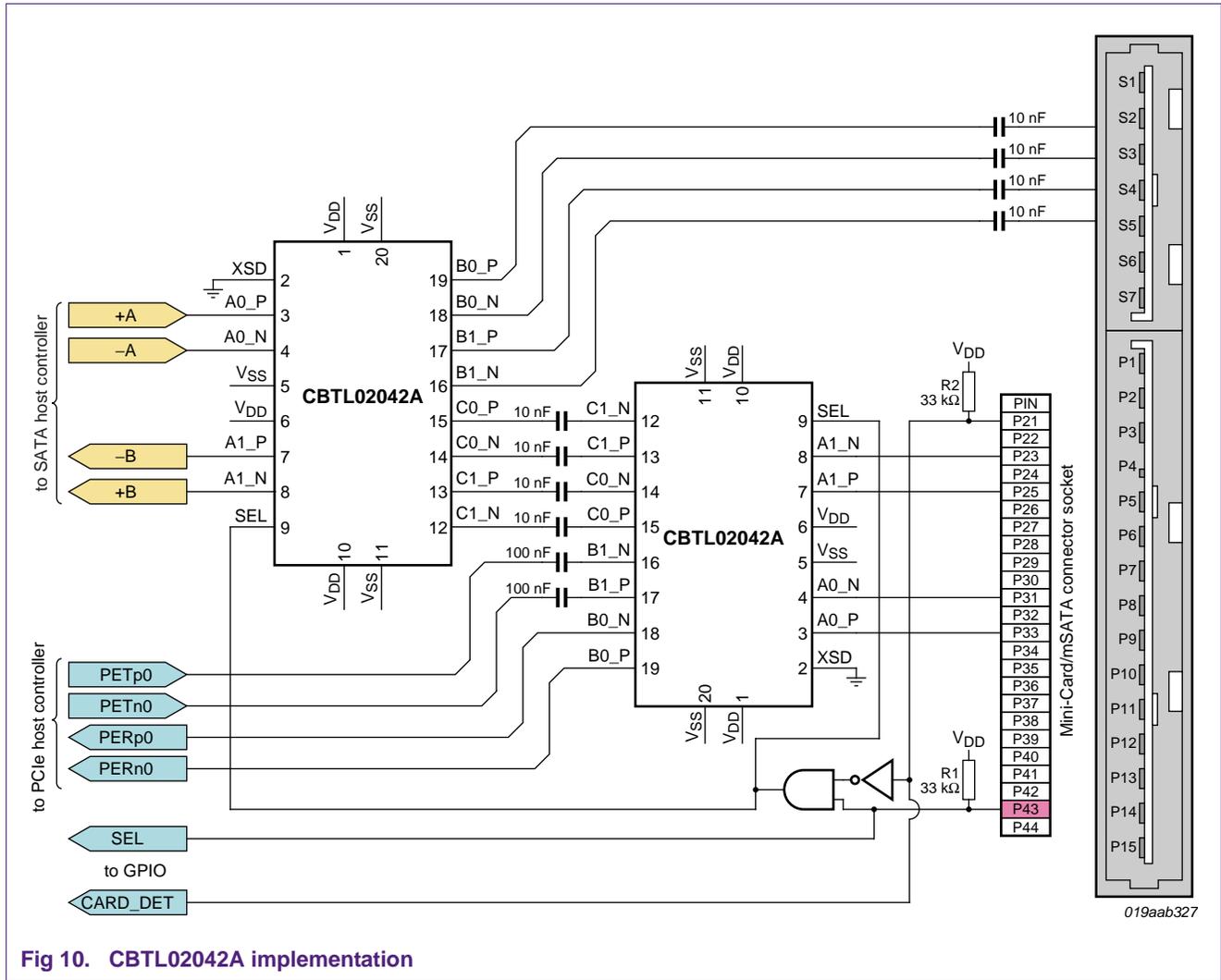**Fig 9.   CBTL04082A/CBTL04083A implementation**

Fig 10. CBTL02042A implementation

Note that PCB routing using a CBTL04082A/CBTL04083A is more difficult to implement than using two CBTL02042As. Signals from a PCI Express controller are connected to pin 26 to pin 29 of CBTL04082A/CBTL04083A, but these pins are encapsulated by SATA signals connecting between pins 22 to 25 and pins 31 to 34. Multiple vias are necessary to route PCI Express signals in this case, and using additional vias usually implies that extra insertion loss needs to be accounted for. PCB routing using two CBTL02042As topology will have a smoother high-speed signal flow without using any via. In addition, SATA and PCI Express signals are typically coming from the same Platform Controller Hub (PCH) located in the middle of the motherboard, and connectors are located on the board edge. The configuration shown in Figure 10 keeps signals to the controllers and to the connectors on the opposite sides of the multiplexers and fits this layout profile perfectly.

When an mSATA device is not inserted in the Mini-Card/mSATA connector, SATA signals should be re-directed to the SATA HDD connector, regardless if a Mini-Card device is present or not. Table 4 summarizes all possible combinations of devices inserted in the Mini-Card/mSATA and SATA HDD connectors.

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Table 4.   Mini-Card/mSATA and SATA HDD device possible insertion combination

		SATA HDD connector	
		None	SATA HDD
Mini-Card/mSATA connector	None	possible	possible
	Mini-Card	possible	possible
	mSATA	possible	impossible (mSATA active)

Circuits in Figure 9 and Figure 10 show automatic hardware selecting the SEL pins on the multiplexers utilizing an AND gate and an inverter, or a single 74LVC1G98. Logic is based on pin 43 and pin 21 on the Mini-Card/mSATA connector. This detection logic can also be implemented using a GPIO output from a processor based on the CARD_DET and SEL signal status. However, this is beyond the scope of this design guideline, and will not be discussed here.

Table 5.   Multiplexer SEL pin logic table

CARD_DET signal state (pin 21)		SEL signal state (pin 43)		SEL pin on multiplexers	
0	card inserted	0	Mini-Card	0	PCIe ↔ Mini-Card
	inverted → 1				SATA ↔ HDD
0	card inserted	1	mSATA	1	PCIe ↔ X
	inverted → 1				SATA ↔ Mini-Card
1	card absent	X (1)	card absent	0	PCIe ↔ X
	inverted → 0				SATA ↔ HDD
1	card absent	X (1)	card absent	0	PCIe ↔ X
	inverted → 0				SATA ↔ HDD

To simplify the circuit diagrams, XSD pins on the multiplexers are also permanently tied to ground disabling device shutdown function. One can utilize pin 21 on Mini-Card connector and S1 or S7 pin on the SATA HDD connector to implement this shutdown feature on the multiplexers as shown below.
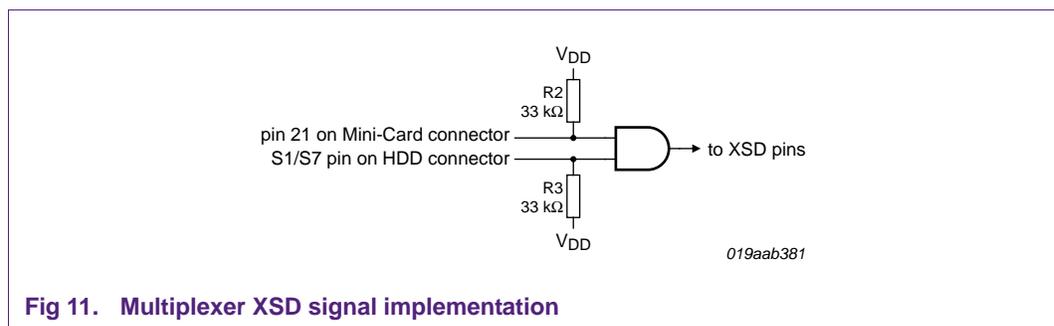
Fig 11.   Multiplexer XSD signal implementation

6. Conclusion

mSATA and PCI Express Mini-Card are sharing the same physical connector type with minor pin definition modification. Automatic card detection and signal multiplexing function between SATA interface and PCI Express interface can be implemented using CBTL02042A. PCB design should account for the insertion loss by the multiplexer, and reduce the trace length accordingly.

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7. Abbreviations

Table 6. **Abbreviations**

Acronym	Description
CPU	Central Processing Unit
ECN	Engineering Change Notice
EMI	ElectroMagnetic Interference
ESR	Equivalent Series Resistance
HDD	Hard Disk Drive
mSATA	mini SATA
PCB	Printed-Circuit Board
PCH	Platform Controller Hub
PCI	Peripheral Component Interconnect
PCIe	PCI Express
SATA	Serial Advanced Technology Attachment

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