AN10998

BGX7221 evaluation board application note

Rev. 1.0 — 17 August 2012 Application note

Document information

Info	Content
Keywords	BGX7221, down-mixer, EVB, IP3, CP1, NF, PCB
Abstract	This application note describes the BGX7221 evaluation board (EVB) design and its performances. BGX7221 is a dual down-conversion mixer designed for base station applications. This EVB includes the required IF transformer in order for differential to single ended impedance transformation, and ease of evaluation with 50Ohm standard SMA connectors.

Revision history

Rev	Date	Description
1.0	20120817	initial version

Contact information

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1. Introduction

Evaluation of BGX7221 is done on the evaluation board A723 v1 (EVB) described in this document.

This document provides the EVB circuit schematic, the bill of materials of the board, the information about PCB technology and its artwork, list of equipments for a typical test set-up required to evaluate the device, and finally the typical test results expected to be obtained.

2. Product Description

The BGX7221 device combines a pair of HIGH performance, HIGH linearity down-mixers for use in receivers having a common local oscillator, for instance having main and diversity paths. The device covers the frequency range from 1700 MHz to 2700 MHz. Each mixer provides an 1 dB input compression point (ICP_{1dB}) above 13 dBm, with an input third-order intercept point (IIP3) of 26 dBm. The small-signal Noise Figure (NF) is below 10 dB whereas under large signal blocking conditions the NF is degraded to 19 dB. Isolation between mixers is at least 40 dB.

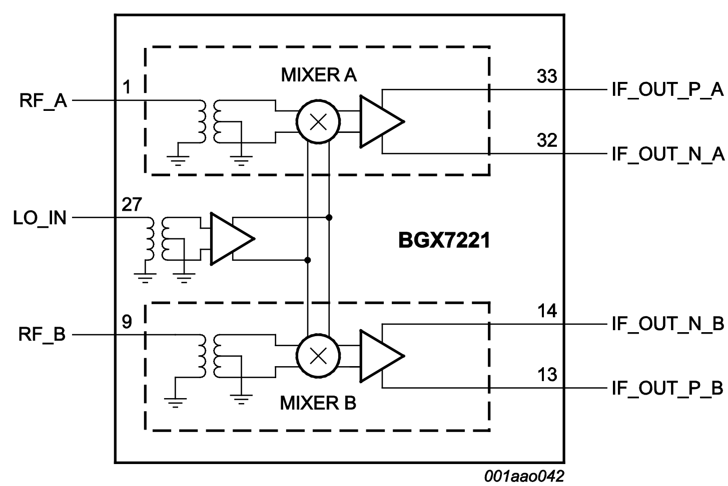

Fig 1. Pin description

Each mixer, A and B employs a transformer to convert the single-ended RF input into a differential signal to drive the passive MOS mixer. The MOS mixer directly drives the IF amplifier. Its open-collector outputs deliver the differential signal into an external transformer load, referenced to the 5 V supply for maximum signal swing. Each mixer can be independently powered-off by a combination of POFF_1 and POFF_2.

The dual paths allow diversity operation with a common LO path. A transformer at the LO input converts the single-ended RF into a differential signal to drive the LO buffer.

3. EVB Circuit Description

The evaluation board is illustrated in Fig 2 associated with its schematic in Fig 3.

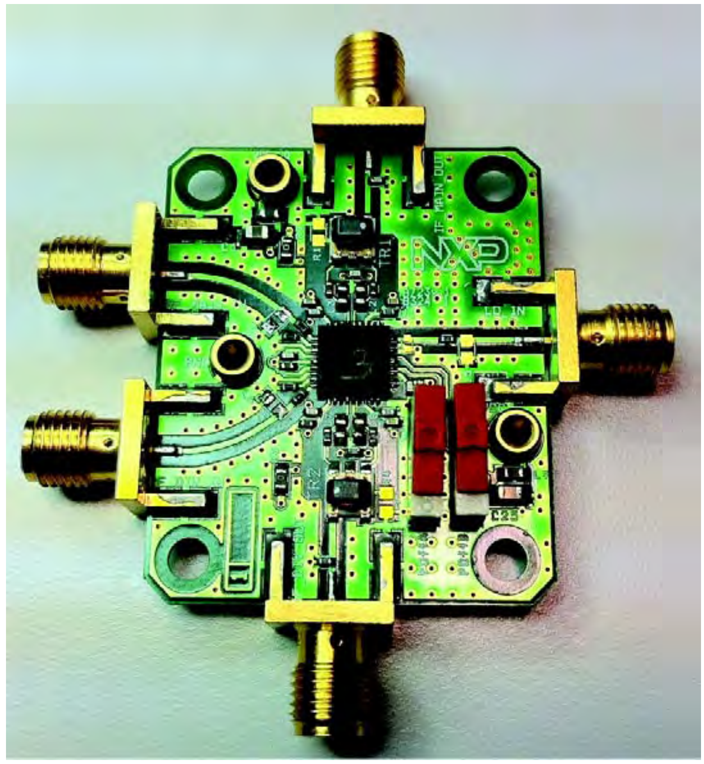

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Fig 2. Evaluation board

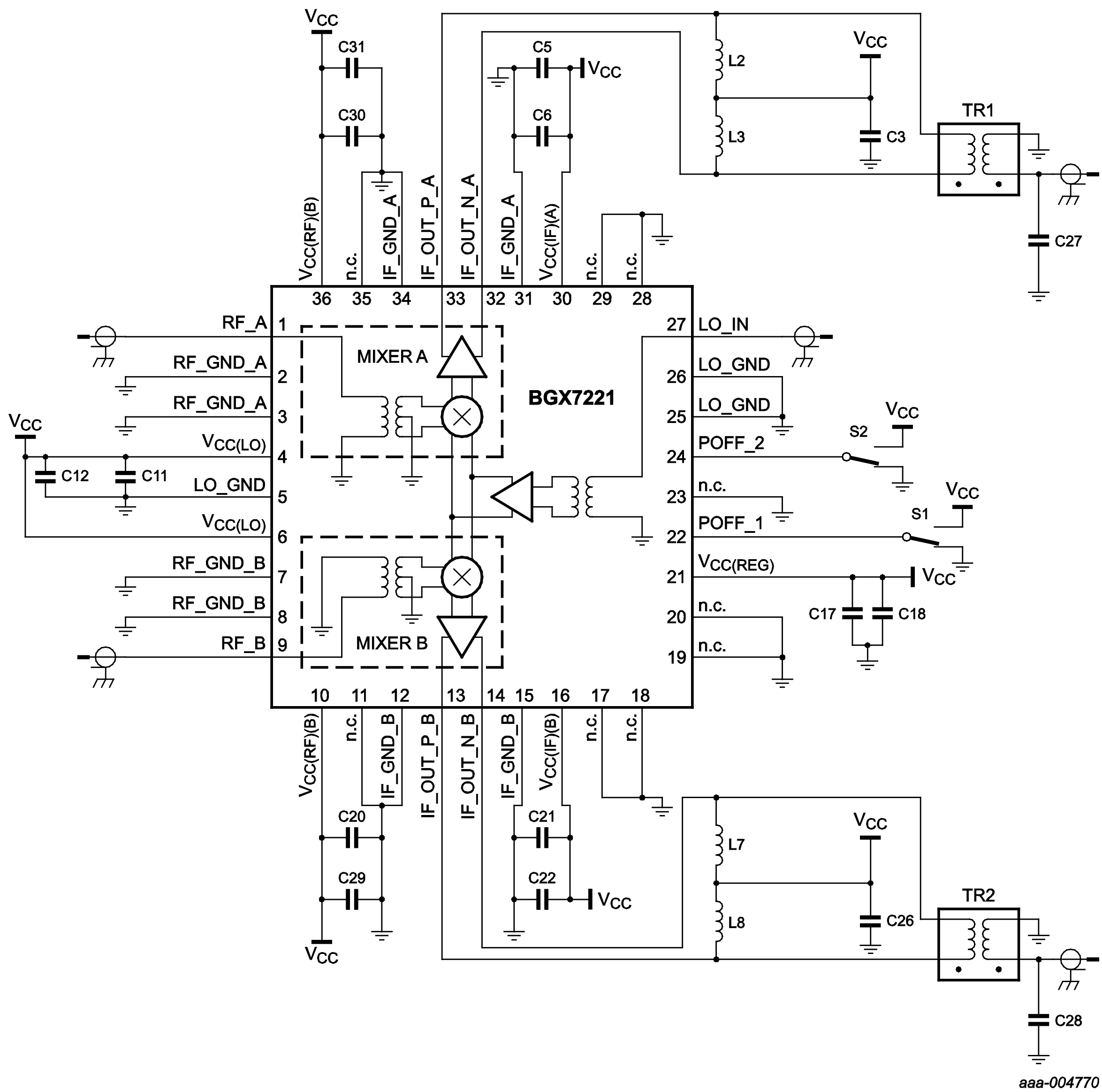

Fig 3. Evaluation board schematic

Table 1. Bill Of Material (BOM) of BGX7221 EVB, IF matching at 200 MHz

Reference	Part	Values	Description	Package	Vendors	Qty
C1, C25	Cc 4.7 µF/16 V	4.7 µF/16 V	capacitor	0805	Murata	2
S1, S2	SECME 1K2		change over switch		Eao	2
T1, T2, T3	2 mm 200-52 Banana Plug		supply connector		Multicontact	3
RX1, RX2, RX3, RX4, RX5	142-0701-851		SMA connector, 50 Ohm		Emerson/Johnson	5
L1, L9	BLM18SG700TN1D		ferrite bead	0603	Murata	2
C3, C26, C6, C21	GRM1555	150 pF	capacitor	0402	Murata	4
C5, C22	GRM1555	1 nF	capacitor	0402	Murata	2
C12, C17, C20, C30	GRM1555	18 pF	capacitor	0402	Murata	4
C11, C18, C29, C31	GRM1555	100 nF	capacitor	0402	Murata	4
C9, C10, C14, C16		0 Ω	resistor	0402	Rohm	4
C27, C28	GRM1555	15 pF	capacitor	0402	Murata	2
L2, L3, L7, L8	BLM18AG102SN1D		ferrite bead	0603	Murata	4
L4, L5, L6		NC		0603		
R1, R4		NC		0402		
L10		NC		0402		
R2, R3, C2, C4, C13, C23, C24		0 Ω	resistor	0402	Rohm	7
TR1, TR2	TC4-1W-G2		IF transformer	AT224-3	Mini-circuits	2
U1	BGX7221		Dual mixer	HVQFN36	NXP	1

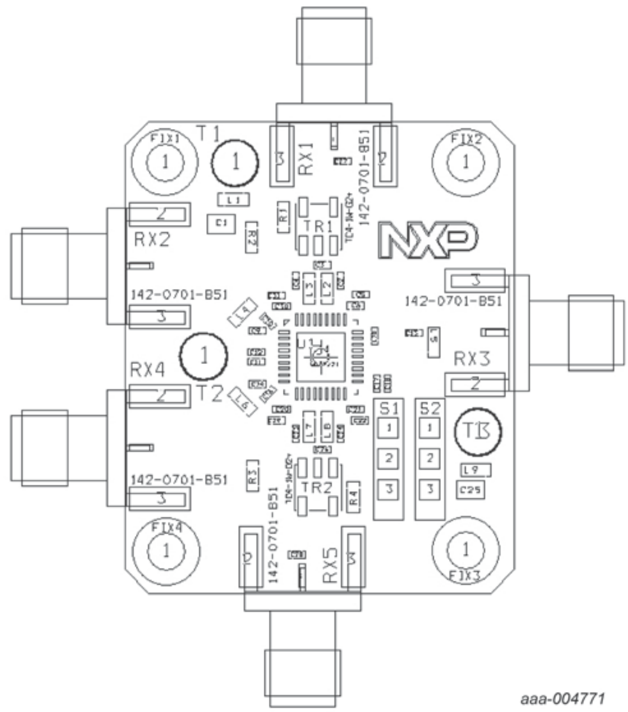

Fig 4. Evaluation board component placement

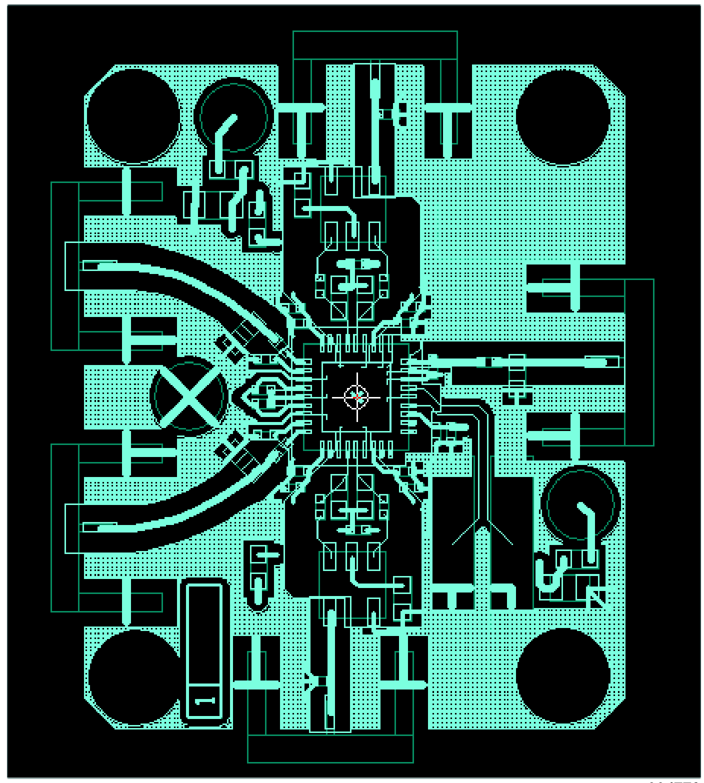

Fig 5. Evaluation board top layer PCB layout

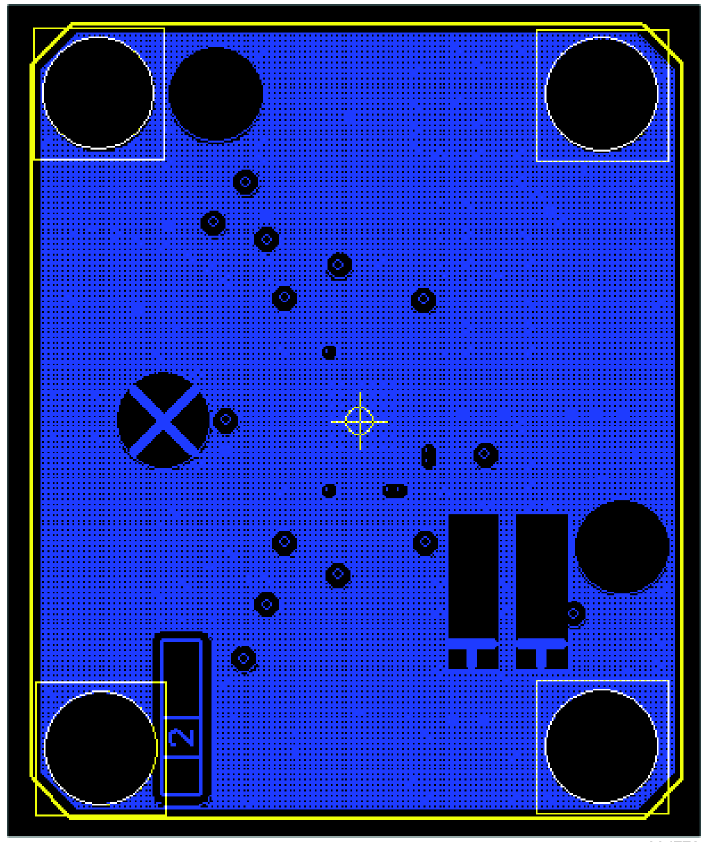

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Fig 6. Evaluation board inner layer_1 PCB layout

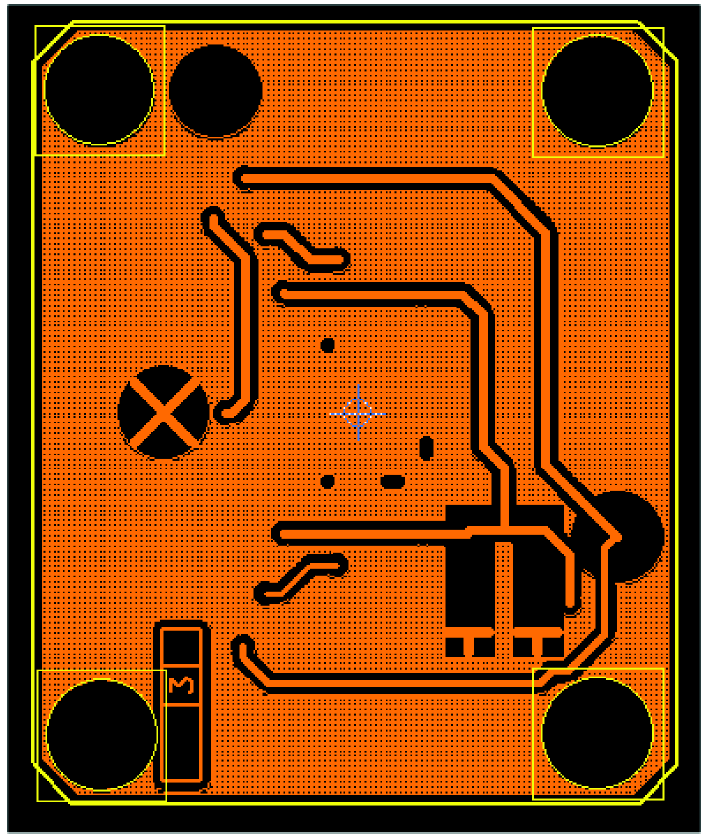

Fig 7. Evaluation board inner layer_2 PCB layout

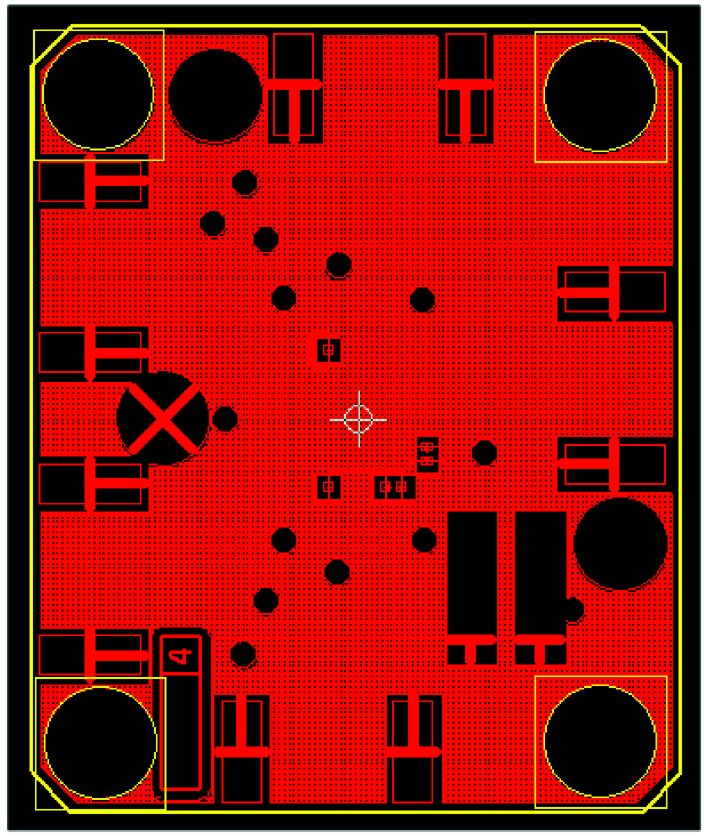

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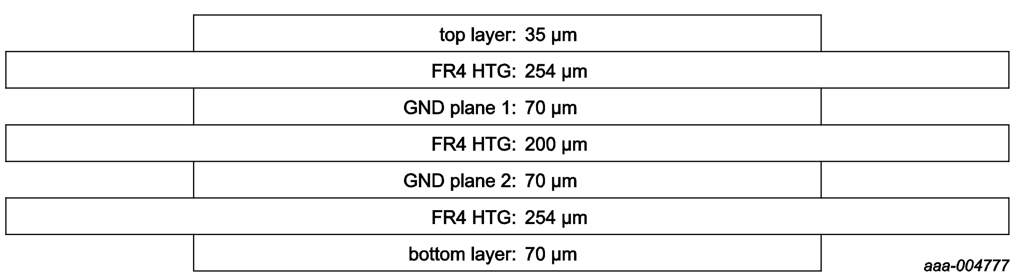
Fig 8. Evaluation board bottom layer PCB layout



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(1) Etching class: Class5 standard.

(2) Minimum copper conductor with: 150 µm.

(3) Minimum conductor spacing: 150 µm.

(4) Ni-Au (Cobalt) finishing: 3 µm - 25 µm of nickel and 0.1 µm – 1.5 µm of gold.

(5) Board dimension: 32.25 mm x 39 mm.

(6) Solder mask both sides green color.

(7) Silkscreen on top layer white color.

(8) Finished thickness: 1 mm +/- 10 %.

(9) Top layer 460 µm traces are controlled impedance, 50 Ω lines.

Fig 9. Evaluation board stack up

4. Test setup

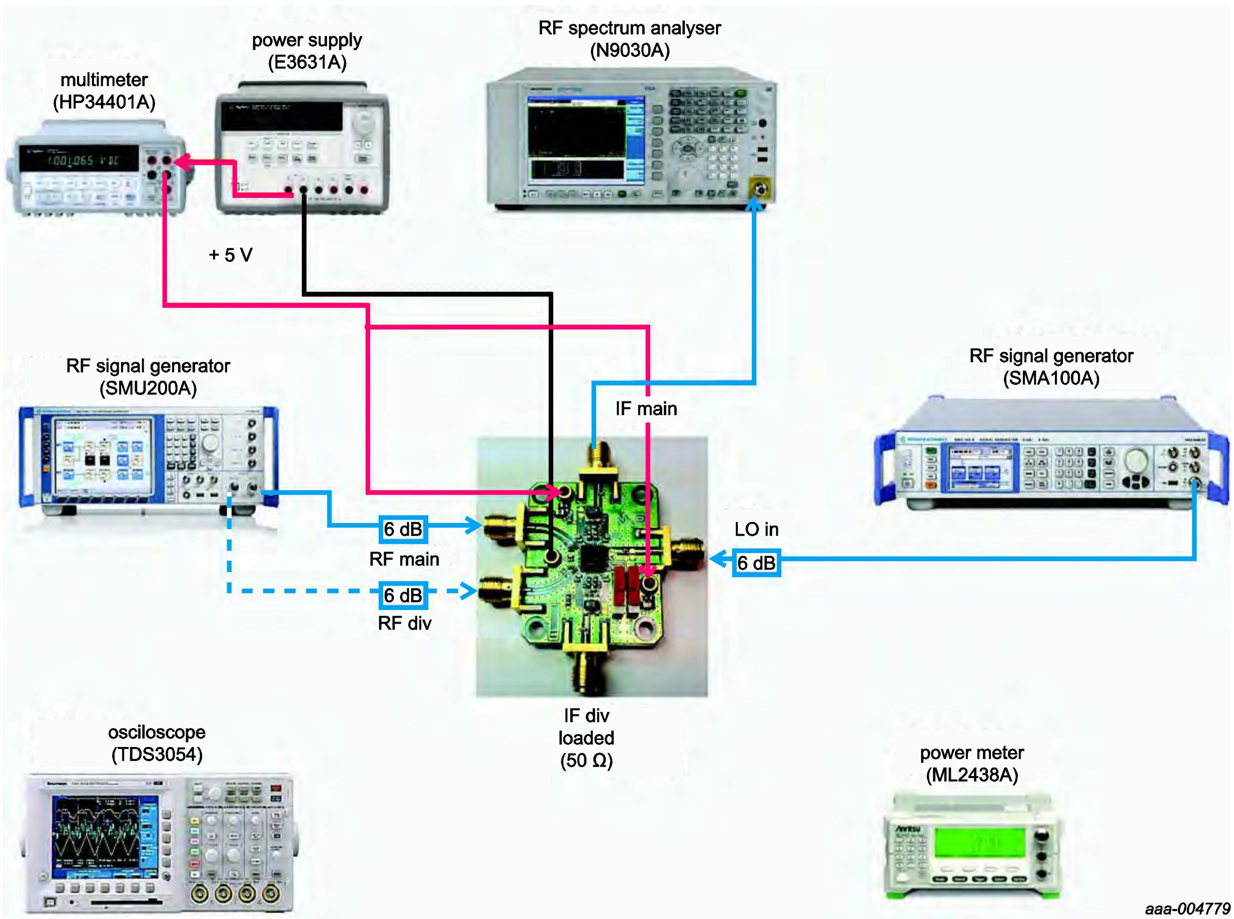

Fig 10. Test setup block diagram

5. Quick start

The BGX7221 EVB kit is fully assembled and factory tested.

5.1 Test equipment required

Fig 10 shows the equipment required to verify the operation of the BGX7221 EVB kit. It is intended as a guide only, and some substitutions are possible.

5.2 Connections

This section provides a step-by-step guide to testing the basic functionality of the EV kit. As a general precaution to prevent damaging the outputs by driving high-VSWR loads, **do not turn on DC power or RF signal generators until all connections are made**:

1) Connect 3 dB pads to the DUT ends of each RF signal generators' SMA cables (RF Main/RF Div/LO in) and 3 dB pad to the DUT output (IF Main/IF Div). This padding improves VSWR, and reduces the errors due to mismatch.

2) Measure loss in 3 dB pads and cables. Use this loss as an offset in all output power/gain calculations.
3) Disable all RF signal sources.
4) Connect the signal sources to the appropriate SMA inputs. The RF input can be connected to either the RF Main or RF Div inputs, depending on test.
5) Set the RF signal generators according to the following:
   - RF signal source: -10 dBm into DUT at 1900 MHz
   - LO signal source: 0 dBm into DUT at 1700 MHz (f_{IF} = 200 MHz)
6) According to the table 2, put the POFF_1 and POFF_2 to logical level 1 via the switches S1 and S2. Set the DC supply to +5.0 V and set a current limit around 500 mA, if possible. Connect supplies to the EVB kit through the ammeter. Turn ON the supply.
7) Enable the LO and the RF sources.
8) Power-on the mixer, put the POFF_1 and POFF_2 to logical level 0 via the switches S1 and S2.

   Readjust the supply to get +5.0 V at the EVB kit. There will be a voltage drop across the ammeter when the mixer is drawing current.
9) Shutdown the mixer, put the POFF_1 and POFF_2 to logical level 1 via the switches S1 and S2.

Table 2. Power-up control

Mode	Description	Function	POFF_1	POFF_2
Active	mixers A and B fully active	shutdown disabled	0	0
Idle	mixers A and B fully OFF; current supplied to LO buffer	shutdown enabled	1	0
Main	mixer A active and mixer B OFF	partial shutdown	0	1
Diversity	mixer A OFF and mixer B active	partial shutdown	1	1

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7. List of figures

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