AN10961

Dimmable CFL using the UBA2027X family

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Document information

Info	Content
Keywords	CFL, Triac dimmable, UBA2027X
Abstract	This application note describes the design of a dimmable Compact Fluorescent Lamp (CFL) with low dimming level using the UBA2027X.

Revision history

Rev	Date	Description
v.2	20120608	second, updated issue
Modifications:		• Text and drawings updated throughout the document.
v.1	20110815	first issue

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1. Introduction

This application note describes the design of a dimmable CFL with a low dimming level using the UBA20270 or UBA20271/UBA20272 ICs. The example illustrated is a 20 W application using the UBA20270 with SPS04N60C3 external MOSFETs. At power levels below 20 W, the UBA20271/2 with integrated MOSFETs can be used.

The UBA20270 controller can be used with both the 120 V and 230 V mains voltage applications. Select the UBA20272 for 230 V mains applications and the UBA20271 for 120 V mains applications for optimal performance.

Remark: Unless otherwise stated all voltages are AC.

A standard commercially available phase-cut wall dimmer is used as the triac wall dimmer. This type of dimmer is representative of most dimmers for 120 V or 230 V input mains applications. Some component values in the application need adapting for dimming compatibility when using other dimmers.

The topology is based on a Voltage Source Charge Pump (VSCP) that is intended to create the necessary hold current for the triac in the dimmer. An End of Life (EOL) circuit has been added externally to the main board for evaluation. The circuit senses high lamp voltage and can shut down the IC in the burn state. The coil saturation protection in the IC does not monitor any ignition or high ignition voltage.

2. Scope

This application note is organized as follows:

- Section 3 describes the basic operation of triac dimming
- Section 4 describes application design
- Section 5 Appendix 1: power calculation equations
- Section 7 Appendix 3: inductive mode preheat calculations

3. Triac dimming

3.1 Triac dimmer circuit

Figure 1 shows the circuit diagram of a triac wall dimmer used in 120 V (RMS) applications.

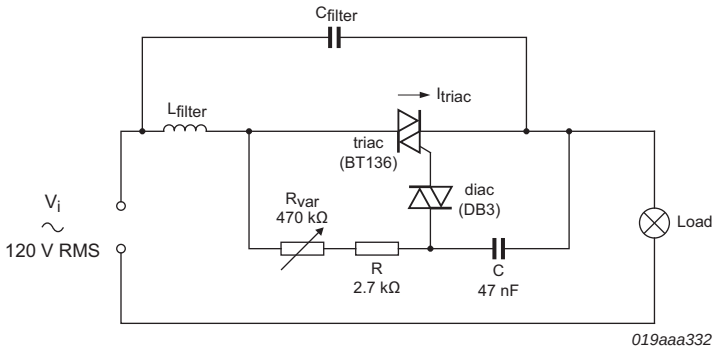


Fig 1. Triac wall dimmer with LC filter

The triac shown in Figure 1 employs forward phase-cut dimming. CFL loads such as incandescent lamps are only energized during the last part of each power-line half cycle (α to π and $\alpha + \pi$ to 2π). See Figure 2 for details.

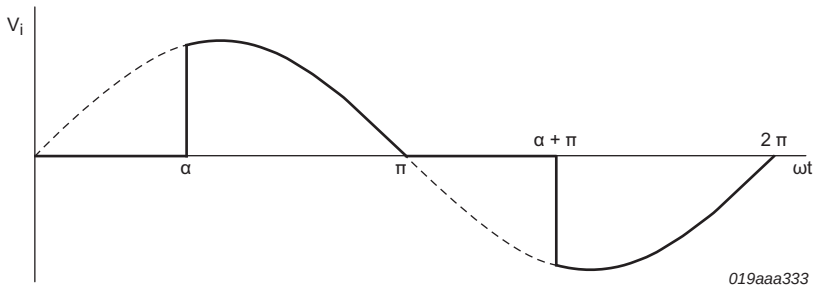


Fig 2. Triac with phase-cut dimming angle α

3.1.1 Circuit overview

In Figure 1, the capacitor C (47 nF) is charged using a fixed resistor R (2.7 kΩ) and a variable resistor R_{var} (470 kΩ). R_{var} sets the phase-cut dimming angle.

When the resistance is low, the capacitor charges quickly. As the voltage across the capacitor reaches the diac break-over voltage, the triac fires and the current I_{triac} flows. The current in the load must be as high as the triac latching current within the period the gate of the triac is fired or triggered. This current continues to flow until I_{triac} drops below its minimum hold current I_H.

If the triac latching current is not reached by the end of its gate trigger pulse, multiple triac firing can occur in a mains half cycle. Avoid multiple firings because they generate unwanted audible noise while the lamp is dimmed.

When the load is an incandescent lamp (resistive load), there is no phase shift between lamp voltage and lamp current. The current can rise high enough within the trigger period of the triac. However, for CFLs, it is not true because of the capacitor in the input filter and the buffer capacitor. The triac is a bidirectional device which operates in two quadrants (see Figure 3). During the negative half cycle, the same process as described earlier is repeated.

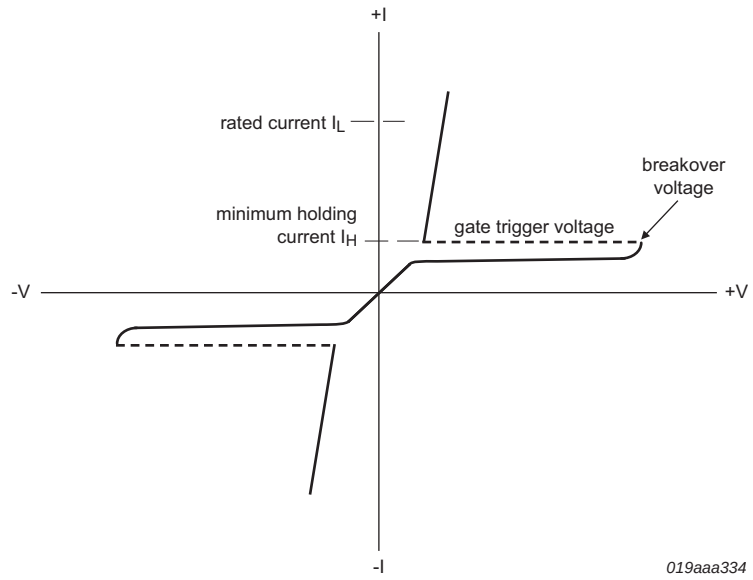


Fig 3. Typical triac voltage and current characteristics

In the triac application, the L_{filter} and C_{filter} can produce ringing of the triac current when the triac latches after a step response. The LC filter in CFL applications incorporates L_{filter} and C_{filter}. The triac ringing current must remain above I_H ensuring the triac remains powered up.

3.2 Triac wall dimmer with VSCS charge pump and CFL ballast

Figure 4 shows a triac wall dimmer and CFL ballast with a Voltage Source Current Source (VSCS) charge pump. The half-bridge MOSFETs in the circuit switch the resonant tank circuit. The lamp current at minimum dimming and lamp voltage at maximum dimming generate the triac hold current ensuring dimming stability.

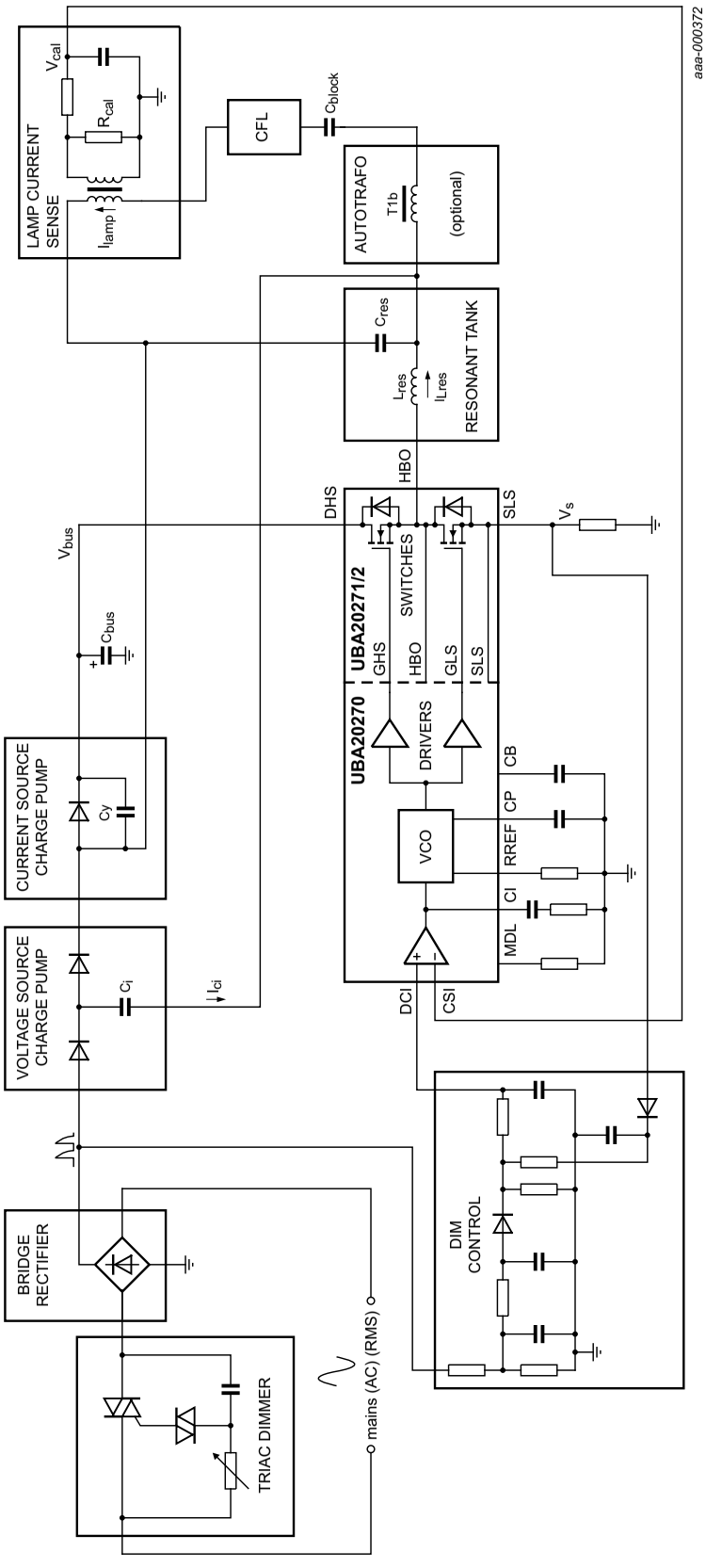
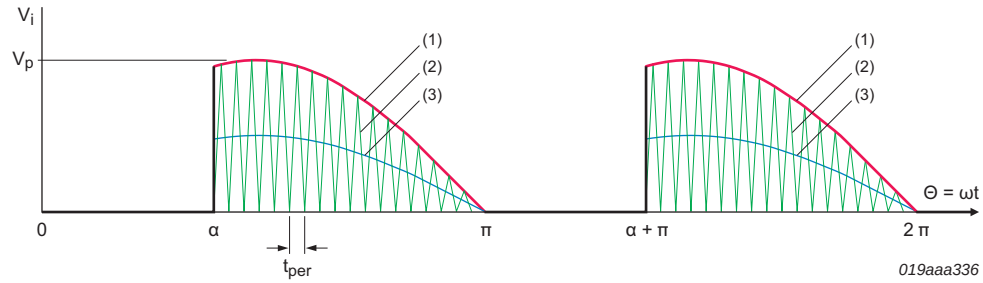


Fig 4. Triac wall dimmer with VSCS charge pump and CFL ballast

The VSCS charge pump maintains triac conduction even at deep dimming since I_H is exceeded for low phase-cut angles (down to A = 130°). A minimum hold current of 30 mA to 50 mA is sufficient for most triac dimmers. With a triac phase angle (A), the input voltage, boost and average boost current is shown in Figure 5.



(1) V_i

(2) I_{bst}

(3) $I_{bst(av)}$

Fig 5. Input waveforms as function of phase cut angle α

The average input current of the VSCS charge pump follows the input mains voltage.

The dimming control signal for pin DCI is derived from the average of the mains rectified signal. This control signal decreases during dimming and simultaneously the frequency regulation loop of the IC increases the frequency of the half-bridge. These actions ensure the voltages on pins CSI and DCI are equal at 0.34 V as shown in Section 4.6.

4. Application design

4.1 Simplified circuit diagram

Figure 6 shows the simplified circuit diagram of the UBA20270 controller in a 230 V application including VSCS charge pump.

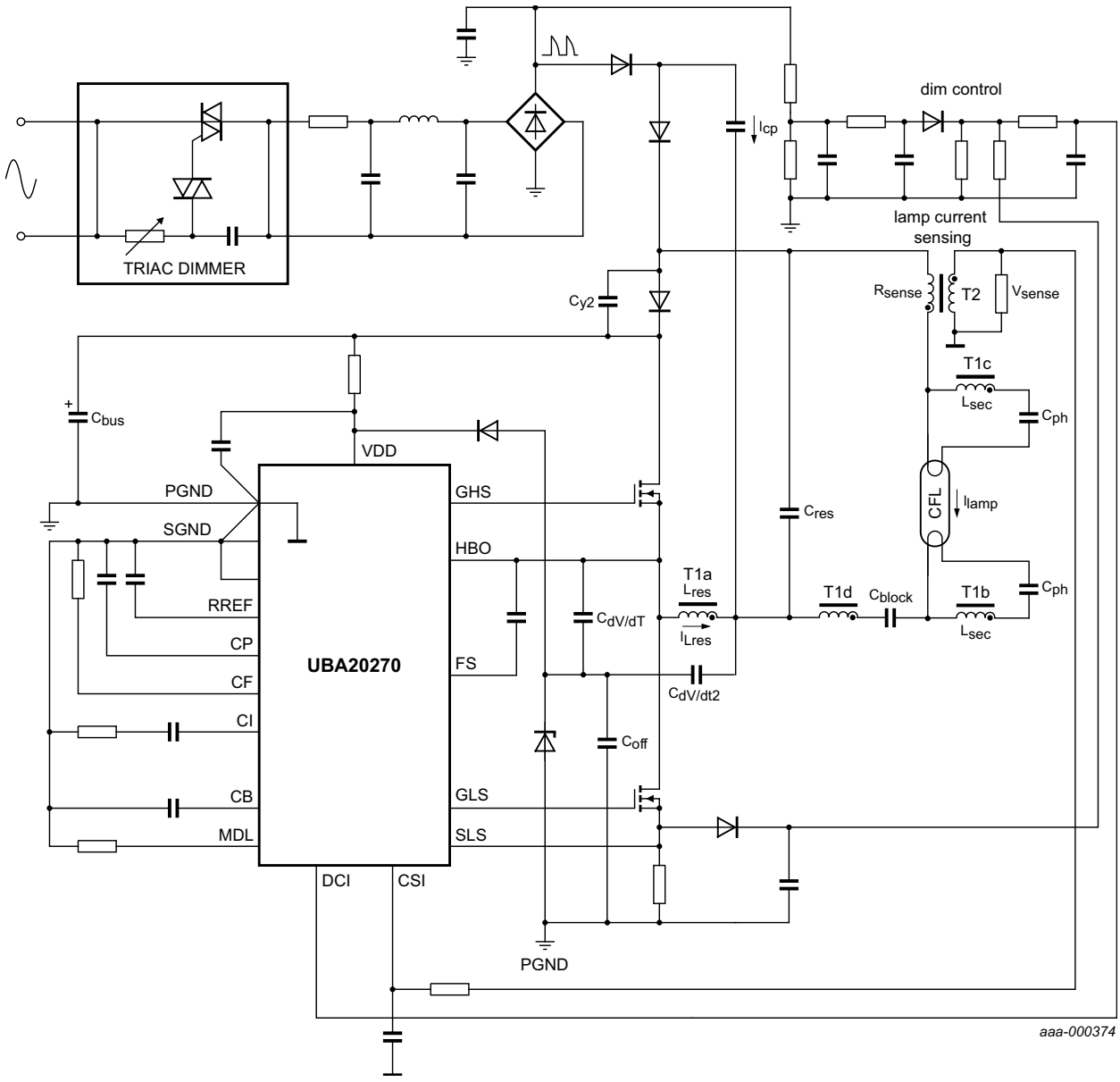


Fig 6. Simplified circuit diagram of a high PF dimming CFL and UBA20270 controller

4.2 Resonant tank parameters

The resonant inductor (L_{res}) is the dominating component for the power delivered to the lamp (P_{lamp}). However, the resonant capacitor (C_{res}) also has influence. Calculate the L_{res} value to deliver the required lamp current during the boost period. The lamp current during boost is 1.5 times the nominal lamp current. C_{res} is calculated to ensure that the operating frequency is above 40 kHz in the boost state and the minimum mains voltage is V_{mains} − 10 %.

The current in the MOSFETs increases for a higher C_{res}. At a lower C_{res}, the possibility of hard switching increases because the resonant tank is no longer inductive.

The autotransformer concept lowers the MOSFET current by reducing the voltage on C_{res} while maintaining the nominal lamp voltage.

An important parameter is the parasitic capacitance inside the transformer L_{res} and its secondary windings. Parasitic capacitance is especially important for the filament winding connected to the lamp current sense resistor (R_{CSI}). Due to parasitic capacitance, current is directly injected from the resonant tank into R_{CSI}, bypassing the lamp discharge current.

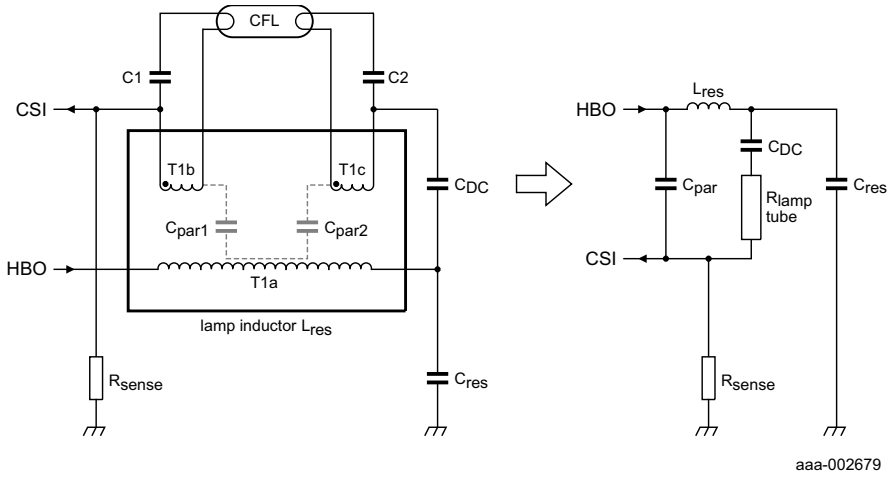


Fig 7. Transformer model L_{res} with parasitic capacitors C_{par1} and C_{par2}

This current degrades deep dimming performance because the lamp discharge current is no longer regulated. The parasitic capacitance must be less than 25 pF to ensure good deep dimming performance.

When the autotransformer winding is used in series with R_{CSI}, the capacitance between L_{res} and winding T1d must be less than 25 pF. See Section 4.3 for more information.

Table 1 and Table 2 list the resonant tank parameter starting values for 230 V and 120 V mains.

Table 1. Resonant tank values 230 V mains

Applicable to all values: C_{res} = 3.3 nF, C_{block} = 47 nF, C_{CP} = 680 pF, and C_y = 10 nF.

P_{IN} (W)	P_{lamp} (W)	V_{lamp} (V)	I_{lamp} (mA)	L_{res} with boost (mH)	L_{res} without boost (mH)
15	13	105	120	2.5	2.7
18	16	100	160	2	2.5
20	18	110	160	2	2
23	21	110	190	2	2

Table 2. Resonant tank values 120 V mains

Applicable to all values: C_{block} = 22 nF, C_{CP} = 680 pF, and C_y = 15 nF.

P_{IN} (W)	P_{lamp} (W)	V_{lamp} (V)	I_{lamp} (mA)	L_{res} with boost (mH)	L_{res} without boost (mH)
13	11	100	110	1.2	1.2[1]
15	13	105	120	-	1.2[1]
15	13	105	120	1	-[2]
20	18	110	160	-	1[2][3]

[1] C_{res} = 5.6 nF.

[2] C_{res} = 6.8 nF.

[3] Not recommended for resonant topology. Use voltage doubler topology instead.

4.3 Autotransformer

An autotransformer is concept where the primary winding of a transformer is tapped somewhere on the primary winding to generate a lower secondary voltage. Since a transformer works both ways using the center tap as primary, you can also raise the voltage. The disadvantage of the autotransformer is that the primary and secondary are non-isolated. However, when used in a CFL application, this is not a problem.

The autotransformer concept is mainly for the 120 V resonant topology. The concept reduces the reactive half-bridge loading by lowering the voltage on the resonant capacitor. In doing so, overall efficiency improves by 30 %.

Figure 6 shows the autotransformer setup. T1a forms the primary winding and T1d the secondary winding of the autotransformer.

In all applications, the output voltage of the secondary winding of the autotransformer is set at 20 V (RMS). The nominal lamp voltage increases/reduces, depending on how the primary and secondary winding are added in series.

Remark: Take note of the dots in the transformer windings if the voltage is increased/reduced. They determine how the windings are used in the schematics (see Figure 22 to Figure 25).

Use the autotransformer for 120 V mains in two cases and when the nominal lamp voltage is:

- > 110 V: to lower the voltage on the resonant tank
- < 95 V: to increase the voltage on the resonant tank

Table 3. Transformer ratios for 230 V and 120 V mains

L_{res} with boost (mH)	T1d ratio (L_{res}: T1d)	L_{res} without boost (mH)	T1d ratio (L_{res}: T1d)
Transformer ratio 230 V			
2	9.74:1	2.5	9.44:1
2.5	9.44:1	2.7	10.27:1
Transformer ratio 120 V			
1	7.26:1	1.2	6.84:1

4.4 Voltage source current source charge pump

Take into account the following four factors to design the charge pump electronic ballast optimally.

- The buffer capacitors voltage rating limits the maximum DC bus voltage
- Satisfying power factor condition: PF ≥ 0.6
- Maintain Zero Voltage Switching (ZVS)
- Input and output power balance

The design guideline for the VSCS-CP electronic ballast with enhanced conduction angle is:

- Set the lowest dim setting or monitor the bus voltage during preheat
- Set input voltage to the nominal line voltage +10 %
- Charge pumped bus voltage value must be V_{bus} ≤ bus capacitor voltage rating
- At nominal power (no dimming) PF ≥ 0.6

Usually, the bus capacitors voltage rating is the limiting factor in the design and not the voltage rating of the IC. The absolute maximum of the bus voltage is 300 V (DC) for the UBA20271 and 550 V (DC) for the UBA20270 and UBA20272. See the appendix sections for more detailed design equations.

Choose a Voltage Source Currents Source (VSCS) charge pump (see Figure 4) over the more traditional single voltage source charge pump ballast because:

- lower bus voltage stress at light load
- lower values for C_{res} and so lower reactive losses good hold current for triac dimmers
- low lamp voltage dependency
- lower lamp crest factor

The effect of both charge pumps is inconsistent. The voltage source charge pump helps at the deeper dim levels where the lamp voltage becomes more dominant. It assists in maintaining the large conduction angle for phase cut dimmers. As the lamp crest factor is close to 1.7 which ensures better lamp life.

In addition, the mains harmonic distortion is lower and the power factor under nominal conditions is much better. The only disadvantage is the current transformer that is required to measure the lamp voltage. Section 8 shows an alternative circuit that solves the problem. The current source pump is driven form an additional winding on the resonant inductor.

At nominal lamp power, the average input current the charge pump delivers, the input current and the input power are calculated in Equation 1 and Equation 2:

Average input current:

$$I_{i(av)} = f_{s(hb)} \cdot C_{y2} \cdot V_i + f_{s(hb)} \cdot C_{y2} \cdot \left[\frac{I_{Lres}}{C_{y2} \cdot f_{s(hb)} \cdot \pi} - V_{bus}\right] \quad (1)$$

Input power:

$$P_i = \frac{1}{2} \cdot f_{s(hb)} \cdot C_{y2} \cdot V_{i(pk)}{}^2 + \frac{2}{\pi} \cdot f_{s(hb)} \cdot C_{y2} \cdot V_{i(pk)} \cdot \left[\frac{I_{res}}{C_{y2} \cdot f_{s(hb)} \cdot \pi} - V_{bus}\right] \quad (2)$$

Where:

- $V_{i(pk)}$ = peak input voltage
- $f_{s(hb)}$ = the half-bridge switching cycle
- V_{bus} = bus voltage (see Figure 5)

See Ref. 3 for more information.

There is no unity power factor condition for the VSCS charge pump with enlarged conduction angle. The second term in Equation 1 is always > 0, because the current source charge pump is dominant over the voltage source charge pump.

The power delivered to the lamp is:

$$P_{lamp} = \frac{V_{lamp}{}^2}{\omega_s \cdot L_{res}} \cdot \sqrt{\left(\frac{\sqrt{2} \cdot V_{bus}}{\pi \cdot V_{lamp}}\right)^2 \cdot (1 - \omega_s{}^2 \cdot L_{res} \cdot C)^2 - (1 - \omega_s{}^2 \cdot L_{res} \cdot (C + C_{res}))^2} \quad (3)$$

Where:

- $\omega_s = 2\pi \cdot f_s$
- V_{lamp} = lamp RMS voltage
- L_{res} = resonant indicator
- C_{res} = resonant capacitor plus the equivalent resonant capacitor (see Section 5)
- C = inductive mode heating circuit secondary capacitance which is transferred to the primary side.

The expression for P_{lamp} in Equation 3 has been derived using the equivalent circuit shown in Figure 8.

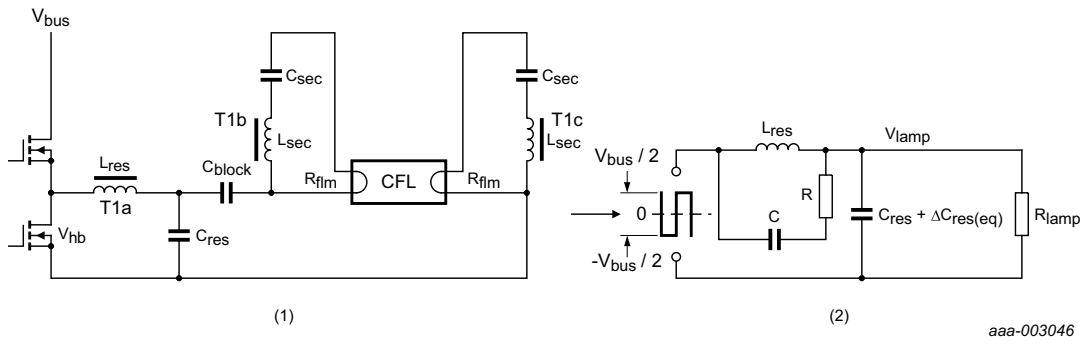


Fig 8. Resonant tank equivalent for inductive mode heating

$$V_{hb} = \frac{\sqrt{2}}{\pi} \cdot V_{bus}\ (RMS) \tag{4}$$

$$R = R_{flm} \cdot \frac{L_{res}}{2 \cdot L_{sec}} \tag{5}$$

$$C = \frac{(2 \cdot L_{sec} \cdot C_{sec})}{L_{res}} \tag{6}$$

$$R_{lamp} = \frac{V_{lamp}^{2}}{P_{lamp}} \tag{7}$$

The power delivered from the mains by the VSCS charge pump and delivered to the lamp is: $P_{lamp} = \eta \cdot P_{in}$.

$C_{dV/dt}$ is chosen so that the resonant tank remains inductive over the complete dimming range, that is, the high-bridge current lags the half-bridge voltage. For a nominal lamp power of 21 W, the phase lags half-bridge voltage is 51°, calculations are shown in Section 7.

The instantaneous current in each MOSFET ($I_{CP} - I_{hb}$) is calculated in Section 7.

The RMS current is approximately 410 mA which agrees with measurements. The instantaneous current $I_{CP} - I_{hb}$ together with the $C_{dV/dt}$ capacitor determine the rise time (t_r) and fall time (t_f) of the half-bridge voltage according to Equation 8:

$$\frac{I_{CP} - I_{hb}}{C_{dV/dt}} = \frac{V_{bus}}{t_{no(r)}\ or\ t_{no(f)}} \tag{8}$$

The rising/falling non-overlap time ($t_{no(r)}$ or $t_{no(f)}$) remains within specification when using a 470 pF capacitor, which is required to maintain zero voltage switching, that is, no hard switching.

4.5 Inductive mode preheating and Sum of Squares (SoS)

The lifetime of the electrode determines the lifetime of a fluorescent lamp. Keep the electrode temperature within certain limits to ensure sufficient lifetime. Above a certain temperature, the electrodes are too hot, leading to enhanced evaporation of the emissive material and severe end-blackening. Below a certain temperature the electrode is too cold and sputtering of the emitter occurs, leading to an extremely short life of the lamp.

The Sum of Squares (SoS) is a measure of the expected amount of heat generated in the filaments and is expressed as:

$$SoS = I_{LL}^{2} + I_{LH}^{2} \quad (9)$$

Where:

- $I_{LH} = I_{lamp} + I_{LL}$

Figure 9 shows the waveform direction of I_{LL} and I_{LH} against time for the period the filaments are inductively preheated. By definition the higher of the two currents is called I_{LH}, the lower of currents I_{LL}. In addition to the relation between the lamp current and the Lead-High current, the Lead-Low current (I_{LL}) can have any value lower than the maximum allowed Lead-Low current. Lead-Low currents exceeding the maximum allowed Lead-Low current cause accelerated end-blackening.

Within limits of the nominal lamp current (I_{lamp}), additional heating is not strictly required. If the lamp current is dimmed over a broader range, additional heating must be supplied to the electrode for it to maintain its optimum temperature. This is equivalent to the ideal target value of 4.75 times the cold filament resistance. In this case, keep the currents in the lead-in wires within limits. The best lifetime and the minimum end-blackening of the lamp is obtained when the “target setting” for I_{LH} and I_{lamp} is observed over the entire dimming range.

Keep the SoS value below a maximum value where the filament resistance is 5.5 times (minimum = 4 times) the cold filament resistance. Alternatively, keep the minimum and maximum settings the manufacturer has specified.

However, an SoS setting close to the target setting is preferred for optimal long-life operation of the lamp. Maintaining, within specification, adequate filament preheating and optimum SoS is difficult, because these are conflicting requirements.

Two points of the SOS target line are easiest to obtain:

- **Preheat or deep dimming**:

  The lamp current is significantly lower than the heating current.
- **Nominal**:

  The nominal lamp discharge current dominates the heating current.

The power required to heat the filament to a constant of 4.75 times the cold resistance can easily be obtained by using a low voltage DC power source and measuring the power required from the source to set the condition. The line between these points can be used as the SoS target over the dimming range.

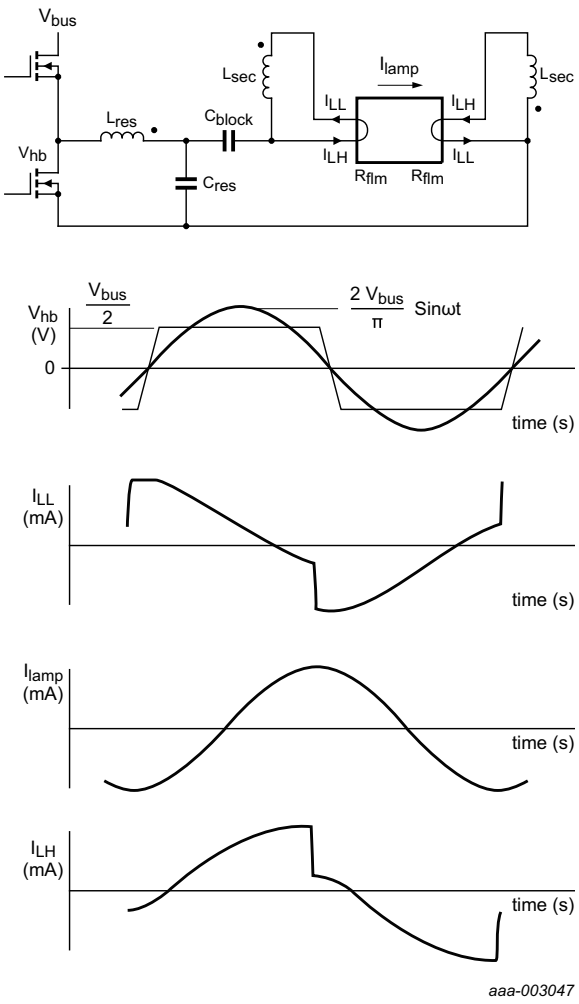


Fig 9. Lamp filament currents for inductive mode heating

Preheating the filament correctly is required to ensure long lamp operating life. However, it also provides the advantage of a lower ignition voltage.

The preheat time is applied to the filaments during the preheat period and is set using Equation 10:

$$t_{ph} = \frac{C_{CP}}{I_{o(CP)}} \cdot (16 \cdot V_{hys(CP)} + 5 - V_{th(CP)max}) \quad (10)$$

Where:

- C_{CP} = 330 nF
- $I_{o(CP)}$ = 5.9 µA
- $V_{hys(CP)}$ = 0.7 V
- $V_{th(CP)max}$ = 4.5 V

The preheat time is 0.65 s

The preheat frequency can be set by measuring the voltage across the SLS resistor between the source and ground of the lower MOSFET (see Figure 25). The half-bridge frequency starts at $f_{VCO(max)}$ and sweeps down until the voltage on pin SLS reaches the V_{ph} level that is defined in the specification. The sweep then stops for the duration of the preheat time t_{ph}.

During the preheat time, the frequency is controlled so that the voltage on pin SLS stays constant, implying that the half-bridge current is kept constant. The half-bridge current level can be adapted by changing the value of the SLS resistor. However, the value selected must not cause the lamp to ignite during the preheat time. Also, the saturation protection and overcurrent protection use the same resistor. Practical values for R_{SLS} at 120 V mains are between 0.9 Ω and 1.5 Ω. At 230 V mains, they are between 1.5 Ω and 2.2 Ω. A value that is too low causes the lamp voltage to become too high during low mains. A value that is too high causes the triggering of the saturation protection.

Adjust the secondary turns or the secondary capacitors if the preheat energy or SoS is not within limits.

Figure 10 shows the frequency as a function of time.

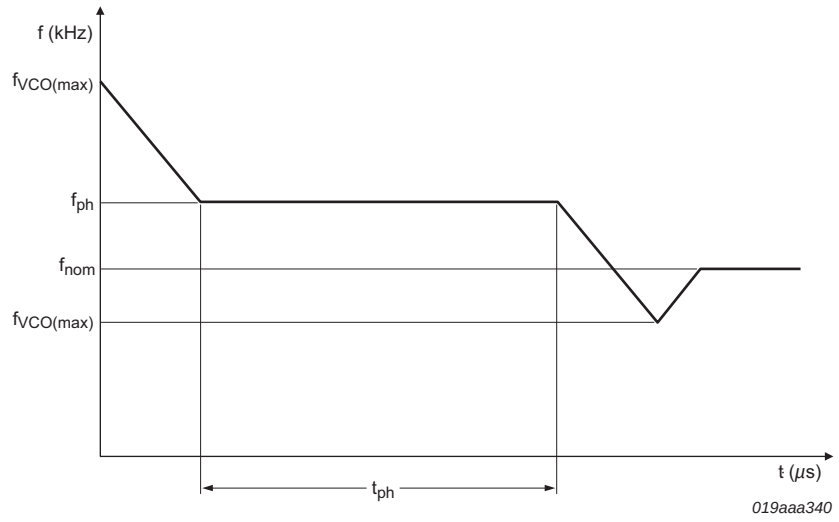


Fig 10. Frequency as a function of time during start-up

The relationship for the preheat (filament) current for Inductive mode heating is calculated in Section 7.

When the half-bridge frequency is 71 kHz, the non-overlap time is 1.5 µs and the RMS filament current is 0.25 A. The filament power dissipated is approximately 1.6 W when the hot filament resistance R_{filter} = 25 Ω. The power supplied to the filament during preheat is $f_s \times C \times V_{sec}^2$ and for a capacitance of 47 nF:

$$V_{sec} = \frac{V_{pri}}{n} \quad (11)$$

Where:

- V_{pri} = 350 V
- $n = \sqrt{\frac{L_{res}}{L_{sec}}} = 16$

The power supplied to the filament is approximately 1.6 W.

The hot-to-cold ratio of the filament resistance must preferably be 4.75:1 to guarantee sufficient filament current is provided at the end of the preheat period. If however, this conflicts with the SoS at deep dimming, choose the lower ratio of 4:1. A higher ratio can overload the filament and reduce the operating lifetime. After the preheat period, the frequency sweeps down rapidly and the lamp ignites when the ignition frequency (f_{ign}) is reached. The lamp can be modeled now as a (negative) resistance where:

$$R_{lamp} = \frac{V_{lamp}^{2}}{P_{lamp}} \quad (12)$$

Before ignition, the lamp has a much higher impedance as no lamp current is flowing. Both characteristics are shown in Figure 11.

Capacitor $C_{CF,}$ resistor R_{RREF} and the voltage on pin CI determine the internal Voltage Controlled Oscillator (VCO) frequency (half-bridge frequency). The minimum and maximum frequencies are as defined in Equation 13:

$$f_{VCO(min)} = 40.5 \cdot 10^{3} \cdot \left(\frac{100 \cdot 10^{-12}}{C_{CF}}\right) \cdot \left(\frac{33 \cdot 10^{3}}{R_{RREF}}\right)$$

$$and$$

$$f_{VCO(max)} = 2.5 \cdot f_{min} \quad (13)$$

Example:

- P_{lamp} = 20 W
- V_{lamp} = 110 V
- L_{res} = 2 mH
- L_{sec} = 10 µH
- C_{res} = 4.7 nF

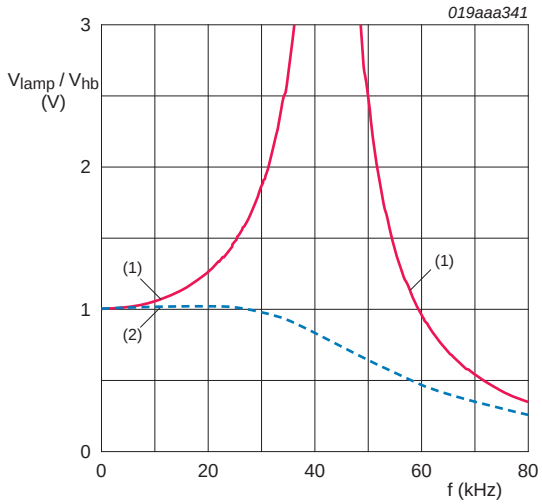
$$R_{lamp} = \frac{V_{lamp}^{2}}{P_{lamp}} = 605\ \Omega \quad (14)$$

$$C_p = 2 \cdot C_{sec} \cdot \frac{L_{sec}}{L_{res}} = 33 \cdot 10^{-9}\ nF \quad (15)$$

$$H(\omega, R_{lamp}) = \frac{p(\omega)^2 \cdot L_{res} \cdot C_p + 1}{p(\omega)^2 \cdot (C_{res} + C_p) \cdot L_{res} + p(\omega) \cdot \frac{L_{res}}{R_{lamp}} + 1} \quad (16)$$

Where:

- $C_p = 2.4\ pF \cdot 10^{-10}$
- $\omega(f) = 2 \cdot \pi \cdot f$
- $p(\omega) = j \cdot \omega$



(1) Hω(f, 2000 Ω)

(2) Hω(f, 650 Ω)

Fig 11. Transfer of frequency before and after ignition

4.6 Dimming using frequency feedback control loop

After lamp ignition and when the IC is in the burn state, the internal average current sensor at pin CSI is regulated to the DCI voltage minus an offset. The voltage on pin CSI is derived by sensing the lamp current and converting it to voltage using a sense resistor as shown in Figure 12.

This voltage is supplied to the CSI pin as:

$$V_{i(CSI)} = I_{lamp}\ (RMS) \cdot R_{sense} \tag{17}$$

The high-frequency feed through the transformer and ignition spike is reduced by adding a low-pass filter. After R_{sense}, the –3 dB point of the filter is set to 1.5 MHz.

Because the UBA2027X incorporates overpower protection, the maximum voltage pin CSI is regulated to in the burn state is 1 V (RMS). This means that the unboosted lamp current is calculated with Equation 18:

$$I_{lamp}\ (RMS) = \frac{1}{R_{sense}} \tag{18}$$

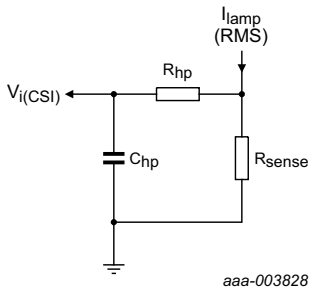


Fig 12. Lamp current sensing

The DCI pin voltage is derived from the mains rectified signal (see Figure 13). This circuit is designed to give a dimming voltage range of 1.5 V to 0.25 V for a phase-cut range of α = 0° – 25° to 130°, respectively. This voltage (after being averaged with the double filter C8, C10, R5 and R6) is applied to pin DCI where:

Table 4. Component values

Component	230 V	120 V
R8	470 kΩ	270 kΩ
R9	470 kΩ	270 kΩ
R10	33 kΩ	39 kΩ
R11	39 kΩ	39 kΩ

The nominal voltage on pin DCI is set 10 % higher than the maximum of 1.34 V. The extra 10 % compensates for small line voltage variations and the minimum phase cut angle that every phase cut dimmer incorporates. This compensation ensures that the lamp does not dim immediately but remains at a constant output. In this setup, the maximum lamp voltage occurs in the first 0° to 25° of the phase angle. The diac or gate trigger circuit's leading-edge phase-cut dimmers cannot start from 0° which always presents a small phase cut. The exact DCI can be calculated using:

$$\left(\frac{V_{pk}\cdot R10\cdot(R5+R11)+R10\cdot(R8+R9)\cdot V_d}{R10\cdot(R5+R11)+R10\cdot(R8+R9)\cdot(R8+R9)\cdot(R5+R11)}-V_d\right)\cdot\frac{R11}{R5+R11} = V_{i(DCI)calc} \quad (19)$$

Where:

- V_{pk} = the rectified peak voltage
- V_d = the diode junction voltage drop

$$V_{i(DCI)offset} = \frac{R}{R+R11}\cdot(V_{i(SLS)}-V_d) \quad (20)$$

$$V_{i(DCI)} = V_{i(DCI)offset}+V_{i(DCI)calc} \quad (21)$$

The circuit that adds a rectified current from the SLS pin to resistor R11 adds a small offset to the DCI when the lamp ignites. Most triac dimmers sense the ignition of the lamp as a load change. They change the triac trigger angle to a smaller phase-cut angle in most cases. Because of this change the DCI voltage drops below 0.24 V for a short moment, when the dimming level is set to a very low level. The lamp turns off. The added rectified

SLS voltage resolves this problem. It lifts the DCI level for a short moment during the ignition of the lamp, creating a stable and flicker-free lamp ON/lamp OFF at lowest dim level. The voltage drop of the diode also prevents that during preheat the DCI voltage is affected.

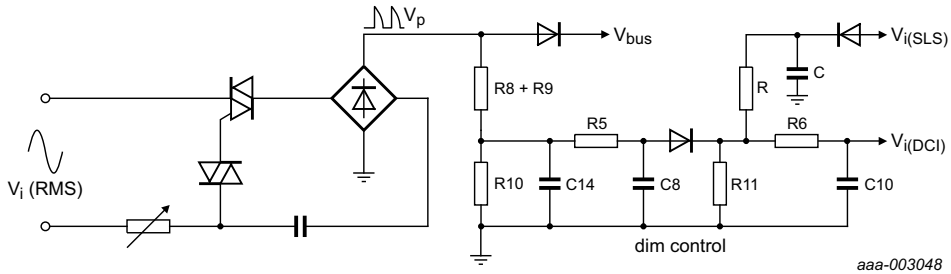


Fig 13. Dimming control

The loop regulation is in balance when the RMS voltage of $V_{i(CSI)}$ equals $V_{i(DCI)}$ (−0.34 V). Voltage levels between 1.34 V and 5 V do not increase the maximum regulation voltage of 1 V (RMS) on pin CSI.

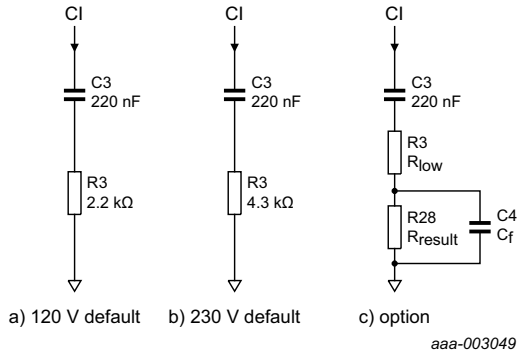
During dimming, regulation is achieved with frequency control:

- $V_{i(DCI)}$ decreases
- The voltage on pin CI decreases
- frequency of the half-bridge increases
- The lamp current decreases
- The RMS value of $V_{i(CSI)}$ decreases

When the voltage on pin DCI is between 0.24 V and 1.34 V, the loop regulation forces the RMS voltage of $V_{i(CSI)}$ to follow $V_{i(DCI)}$ until an equilibrium is reached.

4.7 CI integrator circuit and differential feedback

Normally, a simple resistor (R) in series with a 220 nF integrating capacitor connected to pin CI is used to get a stable lamp operation. The integrating capacitor can be kept constant and the resistor can be tuned to the time constant of the connected burner. Select a resistor value that obtains the most constant and flat lamp current regulation over the entire dimming range.



$$R_{result} = R_{high} - R_{low}$$

$$C_f = \frac{1}{(2\pi \cdot R28 \cdot 3000)}$$

Typical 230 V: R3 = 1 kΩ; R28 = 3.3 kΩ; C4 = 10 nF

Fig 14. CI networks

This simple resistor (R) and capacitor (C) series network cannot solve the problem of burners showing significant lamp flicker for the first minute of a cold lamp start-up.

When using high-temperature amalgam lamps flicker can be observed when the lamp is new, is cold or has been switched off for a long time. Once the lamp is warm or aged, the flickering reduces and eventually disappears.

Differential feedback reduces the first run-up lamp flicker to a minimum (see Figure 15).

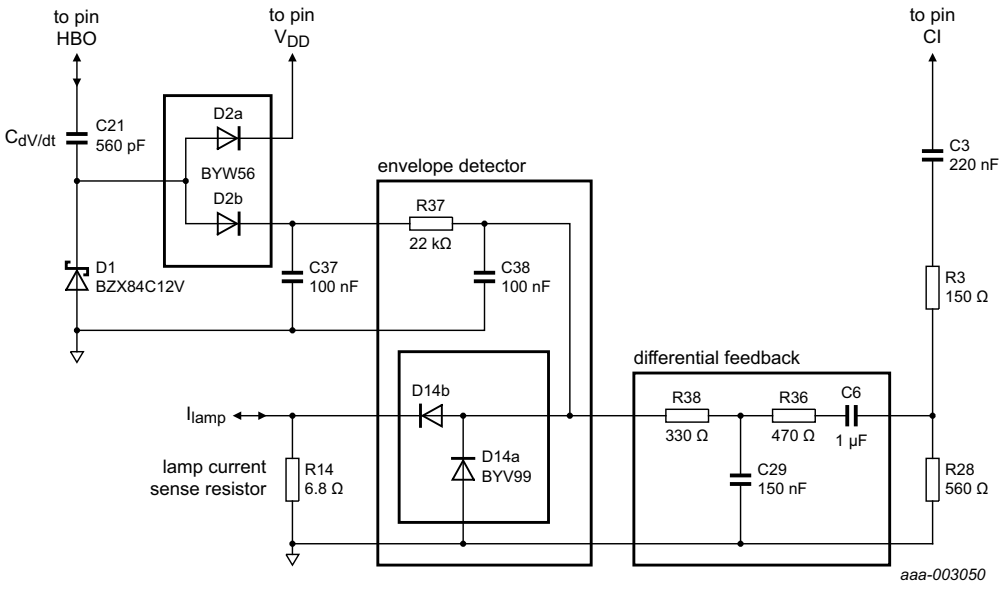


Fig 15. Differential feedback circuit in 120 V mains application

The differential feedback circuit consists of an envelope detector and the differential gain stage. The envelope detector supply comes from a secondary dV/dt supply set up by D2b and C37 to avoid overloading the start-up resistors.

The negative envelope of the lamp current is sensed on the lamp current sense resistor R14. Resistor R38 and capacitor C29 filter it to approximately 4 kHz. Resistors R36 and R28 and capacitor C6 set the amount of differential feedback.

The circuit in Figure 15 is for a 120 V lamp with a particular 12.5 W burner.

Different burners from other manufactures have different lamp specifications. Therefore the lamp time constants differ. The circuit still requires some tuning to get the right amount of differential feedback. Keep capacitor C3 always at 220 nF to tune the circuit. Different values for resistors R3, R28 and R36 can be chosen to get the right mix of integrator action and differential feedback.

In a 230 V lamp the differential feedback is not required as C_{res} is lower. A simple RC integrator is sufficient (see Figure 14 (b)).

In some cases, flicker can be seen when the lamp is dimmed to about 10 % to 80 %. However, it is stable at 5 % to 10 % dimming. In this case, a larger and smaller resistor R3 is preferred. The larger resistor for the gain at lower frequencies, the smaller resistor for the gain at higher frequencies in the feedback loop. Figure 14 (c) shows the circuit that can be used to resolve the issue.

Temporarily replacing R3 with a variable resistor of 10 kΩ in series with a 330 Ω resistor can assist in finding the high and low values for resistor R3. Adjust R3 by looking at the lamp voltage over dimming on an oscilloscope. The envelope of the lamp voltage over dimming must show a line that is as level as possible. Deep valleys in the envelope show that the chosen value for resistor R3 is too low. Noise with peaks above the envelope at the point where the buffer capacitor is charged from the mains indicates that the chosen value for resistor R3 is too low. The corner frequency of resistor R28 and capacitor C4 is set at around 3 kHz. Up to about 2 kHz there is a higher gain. At 11 kHz, there is a lower gain in the feedback loop.

$$R_{result} = R_{high} - R_{low} \tag{22}$$

$$C_f = \frac{1}{(2\pi \cdot R28 \cdot 3000)} \tag{23}$$

At 230 V (typical): R3 = 1 kΩ, R28 = 3.3 kΩ and C4 = 18 nF

Special tools are available to adjust this circuit to fit the parameters of the lamp.

4.8 Boosting of the lamp

When first switched on (in the first 180 s), Amalgam lamps have a slow run up or less light output. A fixed ratio of 1.5:1 boosts the lamp current to resolve this problem. The capacitor on pin CB (C_{CB}) sets the boost time and is calculated with Equation 24.

$$t_{bst} = \frac{C_{CB}}{I_{o(CB)}} \cdot (126 \cdot V_{hys(CB)} + V_{th(CB)min} - 0.6) \tag{24}$$

Where:

- $I_{o(CB)}$ = 1 µA
- $V_{hys(CB)}$ = 2.5 V
- $V_{th(CB)min}$ = 1.1 V
- C_{CB} = 150 nF

These parameters lead to a boost time of 48 s. Shorting pin CB to ground turns off the boost circuit.

During the boost period, the maximum voltage on pin CSI regulates to 1.5 V (RMS), effectively boosting the lamp current by a factor of 1.5. It is important that during the boost the filament current is still operating within their SoS limits, to avoid degrading the lamp operating life. If the lamp does not have higher current rated filaments (not intended for boost), then:

- Lower the lamp operating current to 80 % of nominal
- Run boost at 1.25 % of nominal

In simple terms, run a 12 W burner at 10 W nominal and 15 W during boost.

With higher rated lamps, set the power use to the full 150 %. For example, use an 18 W burner for a 12 W lamp because the filaments automatically have a higher rating.

4.9 Setting Minimum Dimming Level (MDL)

The minimum dim level can be used to prevent the lamp from entering the glow phase at the lowest setting of the dimmer. Glow is observed when there is some light coming from the lamp but the CFL tube is not fully lit. This effect also causes flicker when the lamp changes from glow to normal burn constantly. Resistor R_{MDL} sets the MDL voltage as follows: $V_{MDL} = R_{MDL} \times I_{MDL(src)}$. It is lamp-dependent.

4.10 IC supply and capacitive mode protection

The IC starts when its supply voltage V_{DD} exceeds $V_{DD(start)}$. $R_{startup}$ completes the first charge of the supply decoupling capacitor C_{VDD}. This resistor must be large enough to supply at least 0.32 mA at 12.5 V. The half-bridge begins to switch and the IC is supplied using a capacitor that is connected at the half-bridge (see Figure 16).

A larger capacitor is required when more current is required in the external MOSFETs and thus in the internal drivers which drive the external MOSFETs. However if $C_{dV/dt}$ is too large, hard switching at higher frequencies can occur since the non-overlap time decreases at higher frequencies (adaptive non-overlap time). The minimum required value can be calculated using:

$$C_{dV/dt} = \frac{\left(2 \cdot the\ gate\ charge\ of\ the\ MOSFETs + \frac{I_{DD}}{f_{bridge(min)}}\right)}{V_{bus(min)}} \quad (25)$$

A capacitor value of 470 pF is a good compromise between these two situations. A 12 V Zener diode clamps the voltage and a fast recovery diode supplies it to V_{DD}.

The capacitor C_{off} across the Zener diode turns off the V_{DD} supply of the IC when the bus voltage becomes too low. During lamp preheat and a DC bus voltage that is too low, the UBA2027x regulates to a very low half-bridge frequency. This frequency is close to the ignition frequency, causing a lamp voltage that is too high during preheat. Eventually, this leads to a premature ignition, causing lamp flicker and decreasing the lamp life.

Typically, C_{off} is between 1.5 nF and 3.3 nF depending on the maximum open-lamp voltage of the tube during preheat.

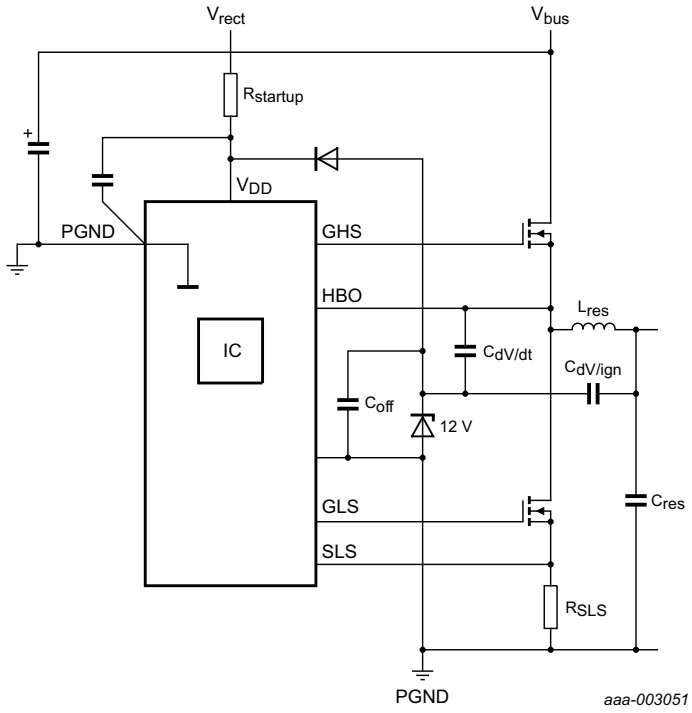


Fig 16. IC supply circuit

4.10.1 Capacitive mode protection

The UBA2027X checks capacitive mode operation by measuring the voltage on pin SLS. Typical waveforms are shown in Figure 17. If the voltage across R_{SLS} ($V_{th(capm)SLS}$) is higher than −5 mV after the preheat state when the LS MOSFET is switched on, the internal logic of the UBA2027X assumes capacitive mode operation at the half-bridge. The half-bridge frequency is increased to $f_{VCO(max)}$ to counter this operation (see for more information Ref. 2).

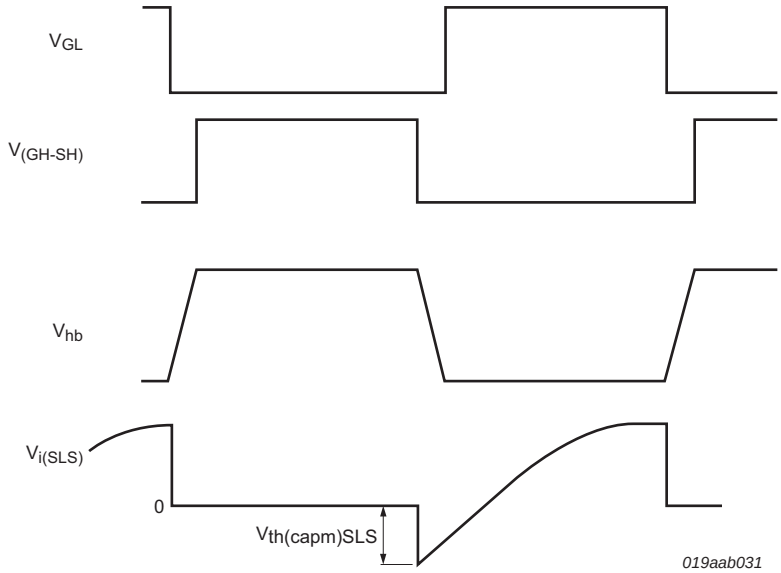


Fig 17. Driver, half-bridge and $V_{i(SLS)}$ capacitive mode detection

4.11 Mains input filtering

A Resistance, Inductance, Capacitance (RLC) filter is used to filter the mains to maintain high EMI performance at the half-bridge frequency and across the harmonic range. The inductor blocks the HF charge pump and operating current, the capacitor provides a low ohmic path for this current. HF current damping can be determined using Equation 26.

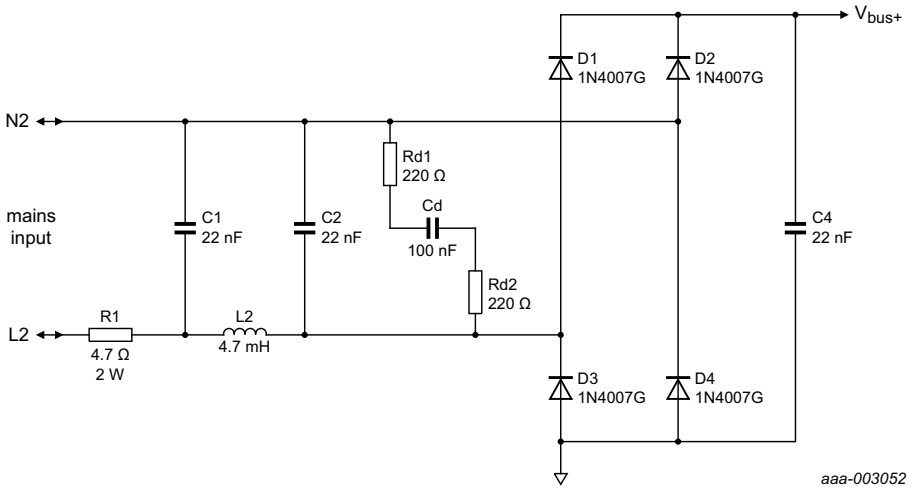


Fig 18. Multiple fire suppression

Because of the diode bridge and the buffer capacitor in the application, the RLC filter does not have a constant load. It can cause mains current ringing when connected to a leading-edge triac dimmer. This ringing in turn causes the triac to shut down after it has been triggered. This leads to unwanted audible noise because of multiple triggering of the triac. Figure 18 shows a solution for suppressing multiple triggering.

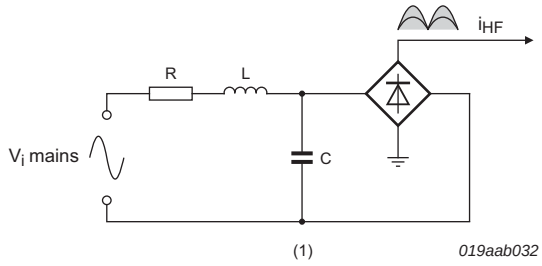
Resistors Rd1 and Rd2 and capacitor Cd create a load for the triac dimmer at higher frequencies which effectively dampen the ringing in the mains current. Rd is split in two enabling distribution of the power into small resistors. Optimum damping for a parallel damped filter is obtained when $Rd = \sqrt{\frac{L2}{C2}}$ and $Cd = 4 \cdot C2$.

Given:

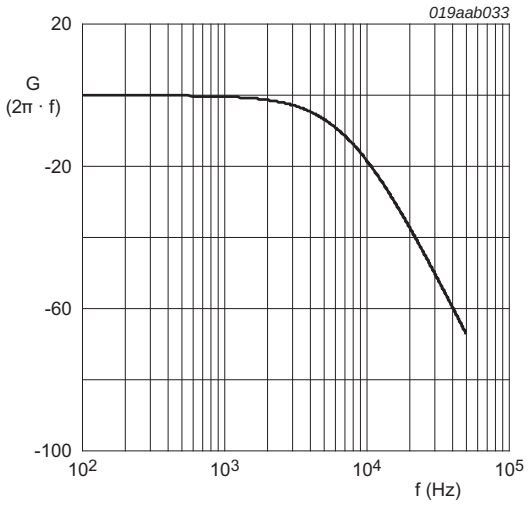
- L = 4.7 mH
- C = 22 nF
- R = 4.7 Ω

$$20log\frac{1}{(1+\omega^2 \cdot L \cdot C)^2 + (\omega \cdot R \cdot C)^2} \quad (26)$$

The calculated damping at 45 kHz relative to 50 Hz is more than 60 dB (see Figure 19 (a)).



a. HF current damping



b. Graphical representation

Fig 19. Transfer function input filter

The fused resistor R (= 4.7 Ω) is used to limit/damp the inrush current during start-up and during large steps of input current during triac operation (see for more information Ref. 1).

4.12 Extra protections

4.12.1 OverPower Protection (OPP)

Since the measured lamp current is clamped at 1 V (RMS), the lamp current remains nominal during mains voltage fluctuations. During overvoltage conditions, the half-bridge frequency increases to keep the lamp current constant. Maintain a 10 % higher voltage level on the DCI pin than the required maximum of 1.34 V for this reason. This action resolves any AC line voltage changes in underpower situations.

4.12.2 Coil Saturation Protection (CSP) and OverCurrent Protection (OCP)

The resonant tank inductor is one of the largest components in the application. Therefore it is practical to select the smallest inductor possible. The maximum current capability of a coil is only important at power-up. Choose a parameter that is sufficient under CFL cold start conditions. During warm starts coil parameters are different as the core material degrades at higher temperatures. These conditions often lead to saturation of the coil when the CFL lamp is ignited. Saturation in turn leads to excessive dissipation of the half-bridge MOSFETs or even the destruction of the MOSFETs.

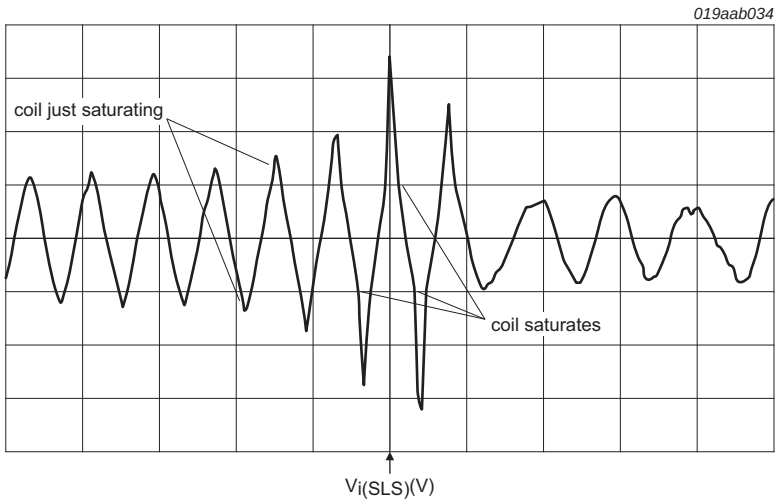


Fig 20. Coil saturation

The IC is equipped with coil saturation protection. This protection enables the use of small inductors in the resonant tank and the inverter without destroying the power MOSFETs.

The circuit monitors the current through the source of the lower MOSFET. The current forces a voltage across R_{SLS}. If the voltage is greater than 2.5 V (set by R17 in Figure 23 and Figure 25) of the current during ignition, the IC limits the frequency decrease. The IC shuts down, if the lamp does not ignite within a quarter of the preheat time.

Only for the UBA20271 and UBA20272 the coil saturation threshold can be adjusted to lower saturation currents.

4.13 End of life circuit (optional)

The autotransformer winding can be used for an optional End Of Life (EOL) circuit when:

- T1d is not used
- The autotransformer winding is placed in series with R_{sense}.

The EOL circuit senses a high lamp voltage during operation by sensing the voltage across the lamp inductor L_{res}. An aged (or old lamp) or a lamp which breaks during operation can cause the high voltage.

The EOL circuit only works when the IC is in the burn state by pulling the CP pin below 1 V.

Adjustment of the circuit can be done by changing the value of R22.

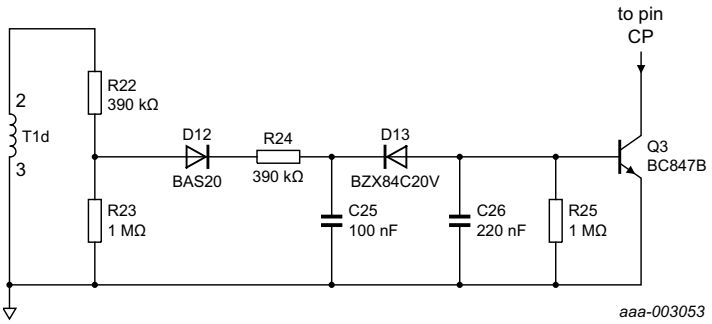


Fig 21. Optional EOL circuit

4.14 23 W 120 V dimmable CFL schematic with UBA20270

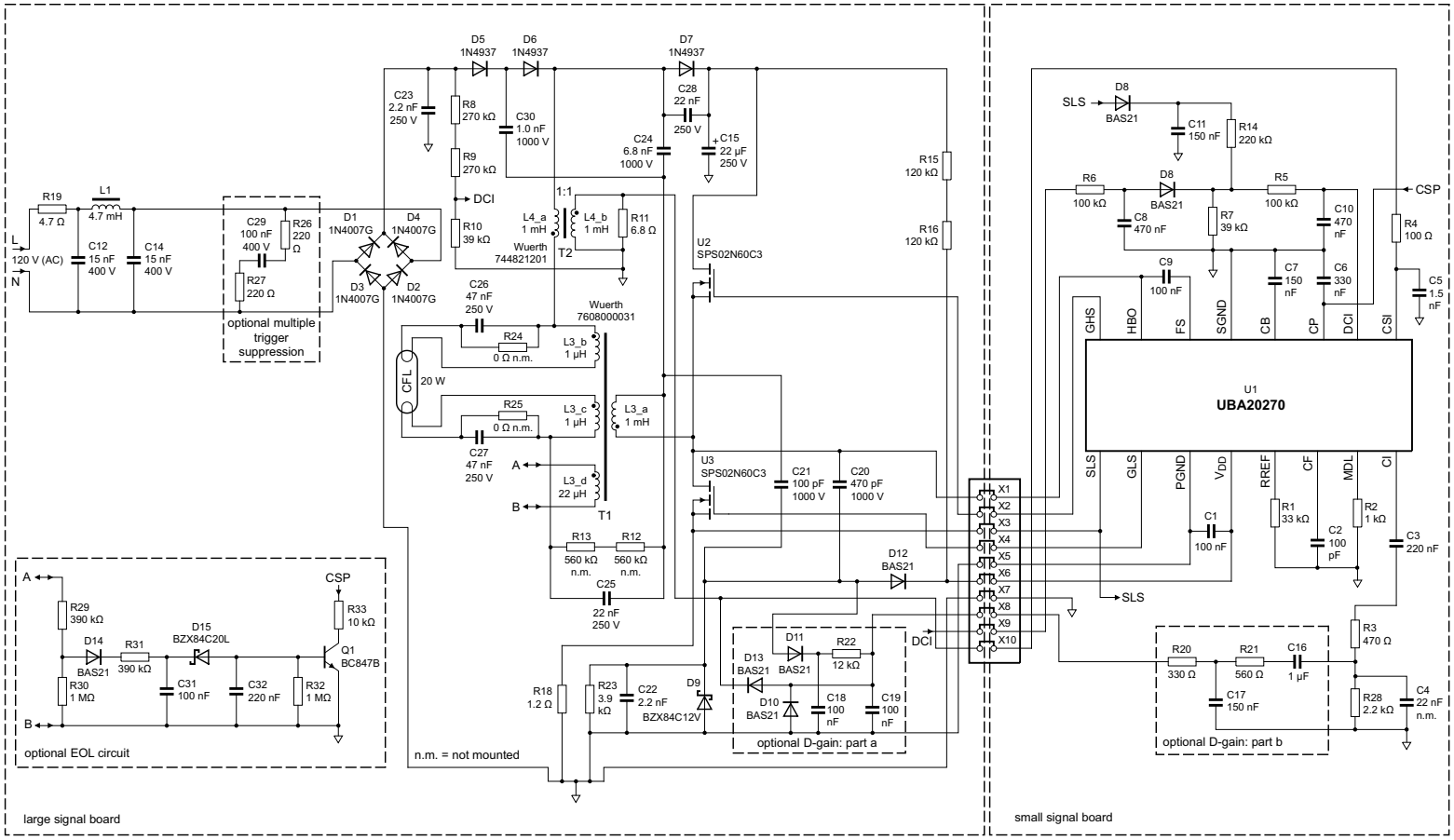


Fig 22. 23 W 120 V dimmable CFL schematic with UBA20270

4.15 23 W 230 V PF dimmable CFL schematic with UBA20270

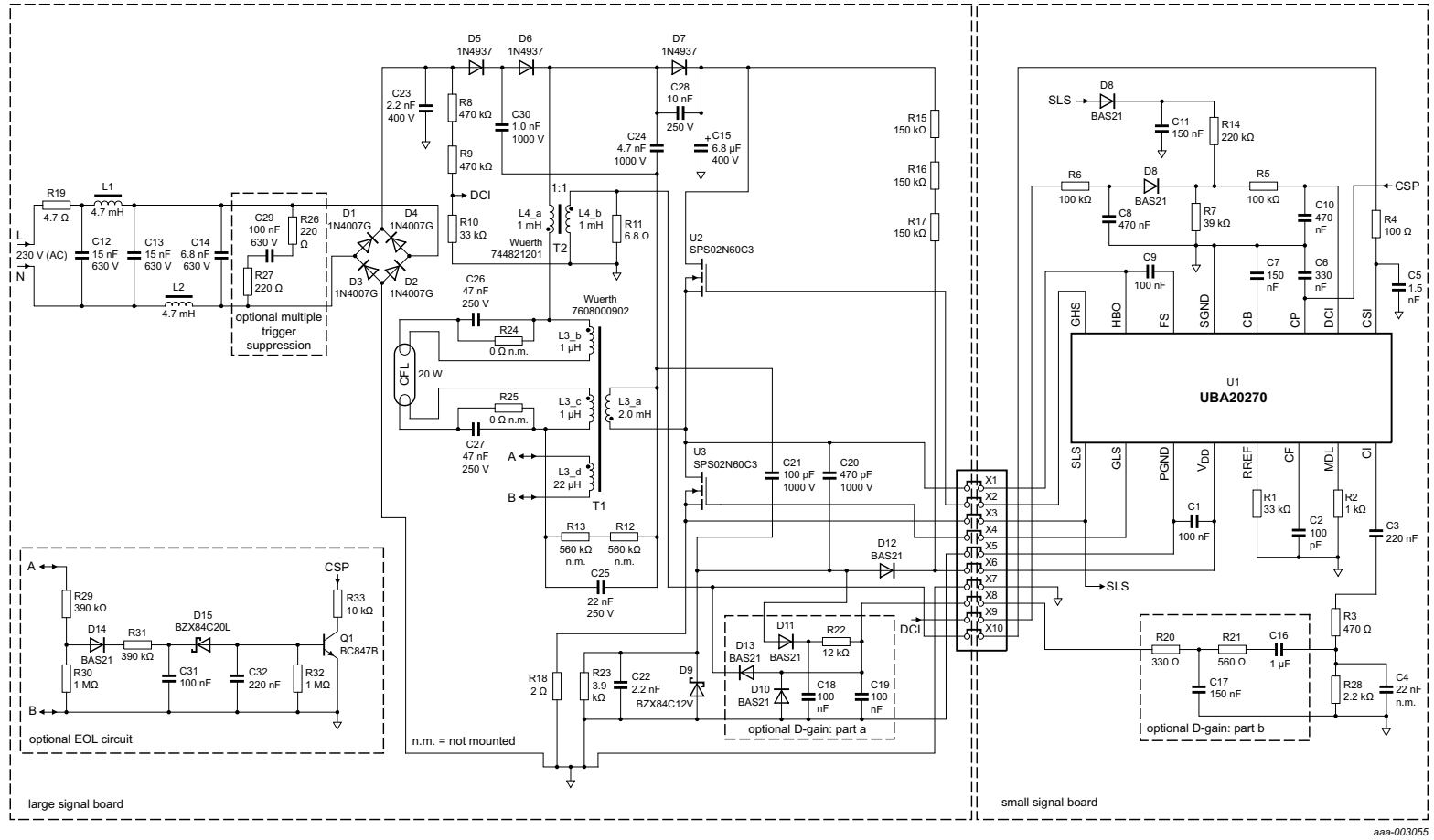


Fig 23. 23 W 230 V dimmable CFL schematic with UBA20270

4.16 18 W maximum 120 V dimmable CFL schematic with UBA20271

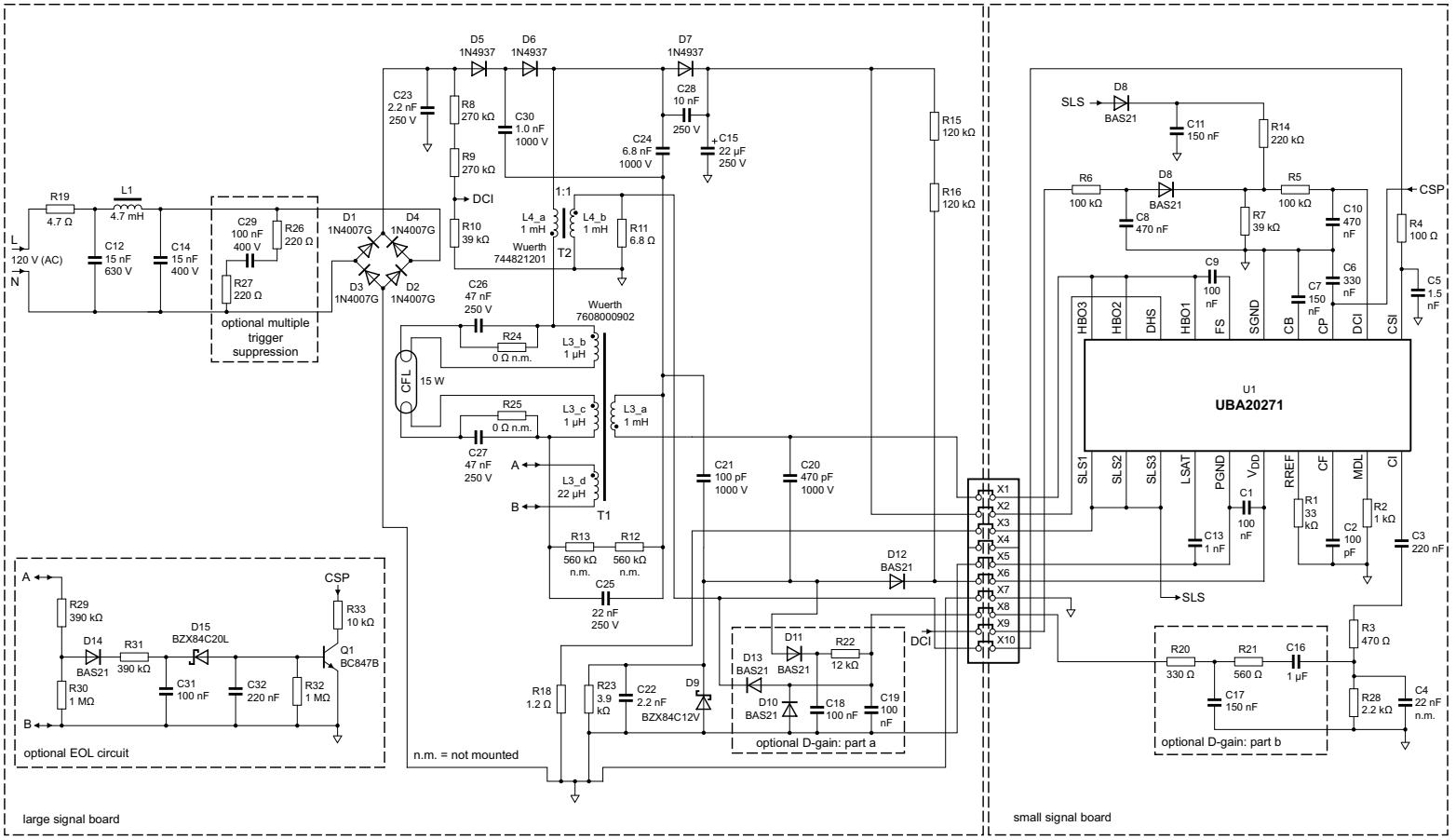


Fig 24. 20 W 120 V maximum dimmable CFL schematic with UBA20271

4.17 18 W maximum 230 V dimmable CFL schematic with UBA20272

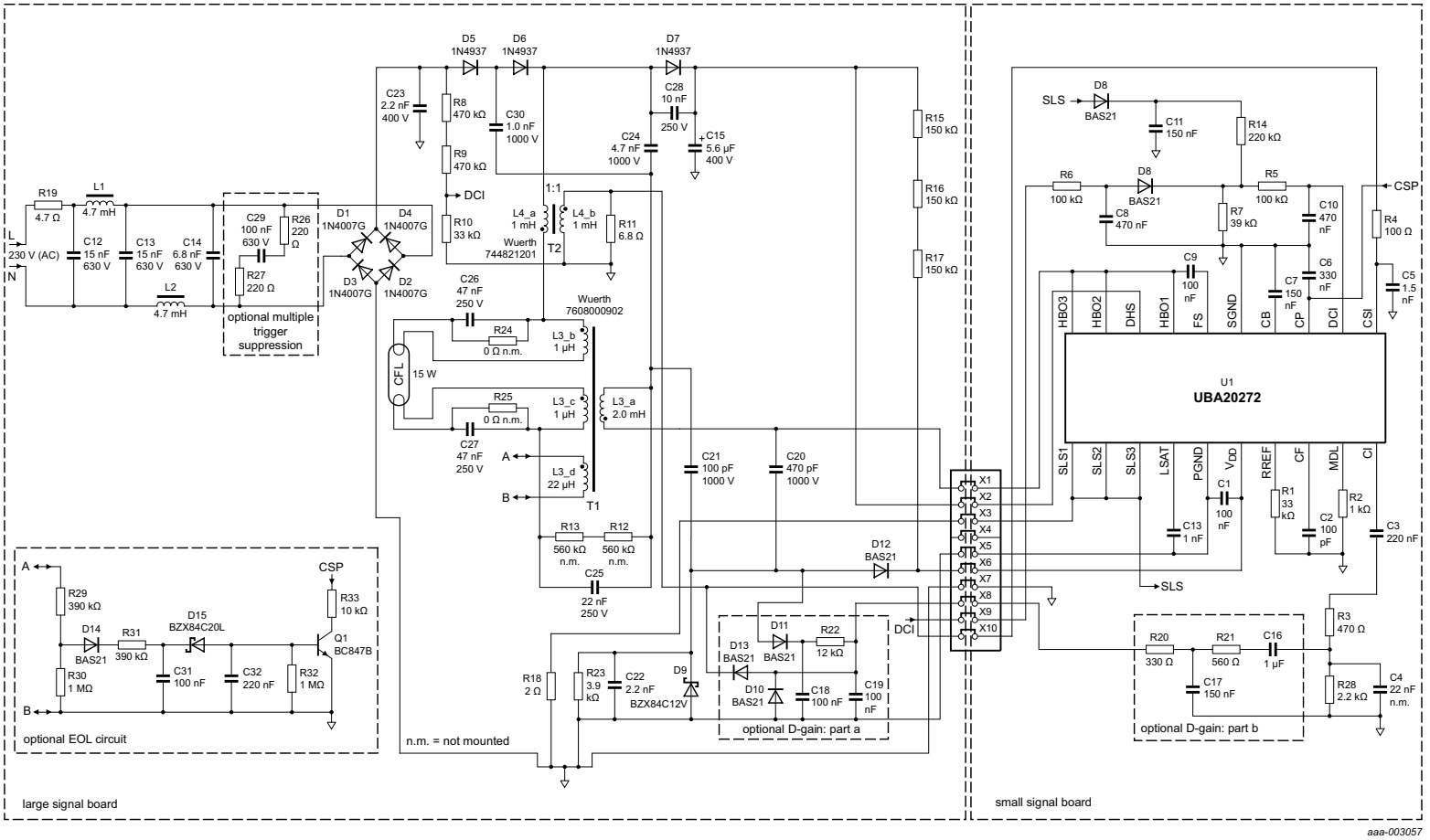
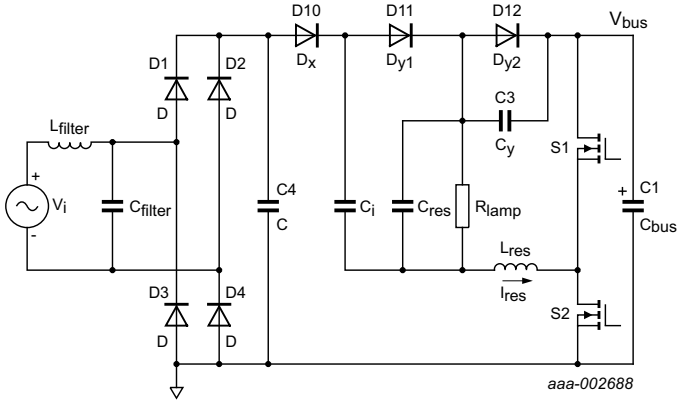


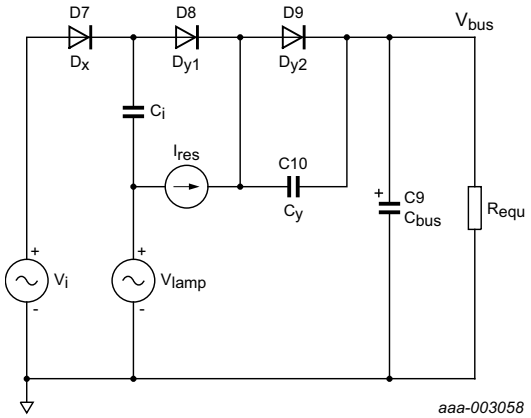
Fig 25. 20 W 230 V maximum dimmable CFL schematic with UBA20272

5. Appendix 1: Power calculations

5.1 VSCS-CP with enhanced conduction angle design equations



a. VSCS charge pump with enlarged conduction angle



b. Simplified equivalent circuit of figure a

Fig 26. VSCS-CP with enhanced conduction angle design

5.2 Assumptions

- V_{bus} is always higher than the input peak voltage and is ripple free
- The lamp voltage V_{lamp} (equal to the voltage across C_{res}) is considered to be a frequency voltage source
- The rectified line voltage V_i is assumed constant over one switching cycle. The switching frequency f_s is much higher than double the line frequency
- The phase shift between the voltage source V_{lamp} and the current source I_{res} is 90 degrees

5.3 Lamp current crest factor

ΔC_{equ} is maximum difference of equivalent resonant capacitance during different topological stages. It is a criterion to determine the approximate crest factor.

$$\Delta C_{equ} = C_i + \frac{C_{res}^{\ 2}}{C_{y2} + C_{res}} \quad (27)$$

$$C_{res(equ)} = C_{res} + \Delta C_{equ} \quad (28)$$

5.4 Current stress in output stage steady state mode (burn state)

$$I_{res(burn)} \approx \frac{\pi \cdot V_{bus}}{V_{i(pk)}} \cdot I_{i(pk)} \quad (29)$$

Where:

- Unity power factor is assumed
- $I_{res(burn)}$ is the resonant inductor current during burn state. It equals the total output current of the MOSFET output stage
- $I_{i(pk)}$ is the peak line input current
- $V_{i(pk)}$ is the amplitude of the line voltage

5.5 DC bus voltage stress during burn state

$$V_{bus(run)} = 2 \cdot V_{lamp(pk)} \cdot \sqrt{\left(\frac{C_i + C_{res}}{C_{y2}}\right)^2 + \left(\frac{\eta}{2\pi} \cdot \frac{V_i^{\ 2}}{V_{lamp}^{\ 2}}\right)^2} \quad (30)$$

Where:

- C_i is the input capacitor
- C_{res} is the resonant capacitor
- η is the conversion efficiency of the circuit in burn state
- $V_{lamp(pk)}$ is the amplitude of the lamp voltage in burn state

5.6 DC bus voltage stress during ignition state

$$V_{bus(max)} = \frac{\frac{I_{res(ign)}}{I_{res(burn)}}}{\frac{f_{ign}}{f_{burn}}} \cdot V_{bus(burn)} + \frac{\pi}{4} \cdot V_{i(pk)} \cdot \left[1 - \frac{\frac{P_{loss}}{\left(\frac{P_{rated}}{\eta}\right)}}{\frac{f_{ign}}{f_{burn}}}\right] \quad (31)$$

Where:

- $I_{res(ign)}$ is the peak resonant inductor current at lamp ignition
- P_{loss} is the total loss in ignition phase state
- P_{rated} is the lamps nominal or rated power
- f_{start} is the starting frequency
- f_{burn} is the frequency in burn state

η = 80 % in the burn state is a practical value.

5.7 Average input line current and power over one switching cycle

If the circuit is designed so Equation 32 is satisfied through all operating periods in a single switching cycle and the conduction angle is enlarged, then:

$$I_{res} \geq C_i \cdot 2(\pi \cdot f_s \cdot V_{lamp(pk)} + C_{y2} \cdot \pi \cdot f_s \cdot V_{bus}) \quad (32)$$

The average input current over one switching cycle is:

$$I_{i(av)} = f_s \cdot C_{y2} \cdot V_i + f_s \cdot C_{y2} \cdot \left[\frac{I_{res}}{C_{y2} \cdot f_s \cdot \pi} - V_{bus}\right] \quad (33)$$

$$P_i = \frac{1}{2} \cdot f_s \cdot C_{y2} \cdot V_{i(pk)}{}^2 + \frac{2}{\pi} \cdot f_s \cdot C_{y2} \cdot V_{i(pk)} \cdot \left[\frac{I_{res}}{C_{y2} \cdot f_s \cdot \pi} - V_{bus}\right] \quad (34)$$

There is no unity power factor condition. The second term is always greater than zero because the current source is dominant over the voltage source.

When the conditions set for I_{res} in Equation 32 are not met, a boundary voltage $V_{i(b)}$ exists:

$$V_{i(b)} = V_{bus} + \frac{1}{\pi \cdot f_s \cdot C_{y2}} \cdot [C_i \cdot f_s \cdot V_{lamp(pk)} - I_{res}] \quad (35)$$

The conduction angle becomes smaller when the instantaneous input voltage is lower than $V_{i(b)}$.There is also a no unity power factor condition and the circuit is more complicated. As design guide line, Equation 36 and/or Equation 37 can determine the average input current over one switching cycle:

$$I_{i(av)} = f_s \cdot \frac{C_i \cdot C_{y2}}{C_i + C_{y2}} \cdot V_i + f_s \cdot \frac{C_i \cdot C_{y2}}{C_i + C_{y2}} \cdot \left[2 \cdot V_{lamp(pk)} + \frac{I_{res}}{C_{y2} \cdot f_s \cdot \pi} - V_{bus}\right] \quad (36)$$

$(V_i \leq V_{i(b)})$

$$I_{i(av)} = f_s \cdot C_{y2} \cdot V_i + f_s \cdot C_{y2} \cdot \left[\frac{I_{res}}{C_{y2} \cdot f_s \cdot \pi} - V_{bus}\right] \quad (37)$$

$$V_i \geq V_{i(b)}$$

6. Appendix 2: New NXP VSCP pump topology

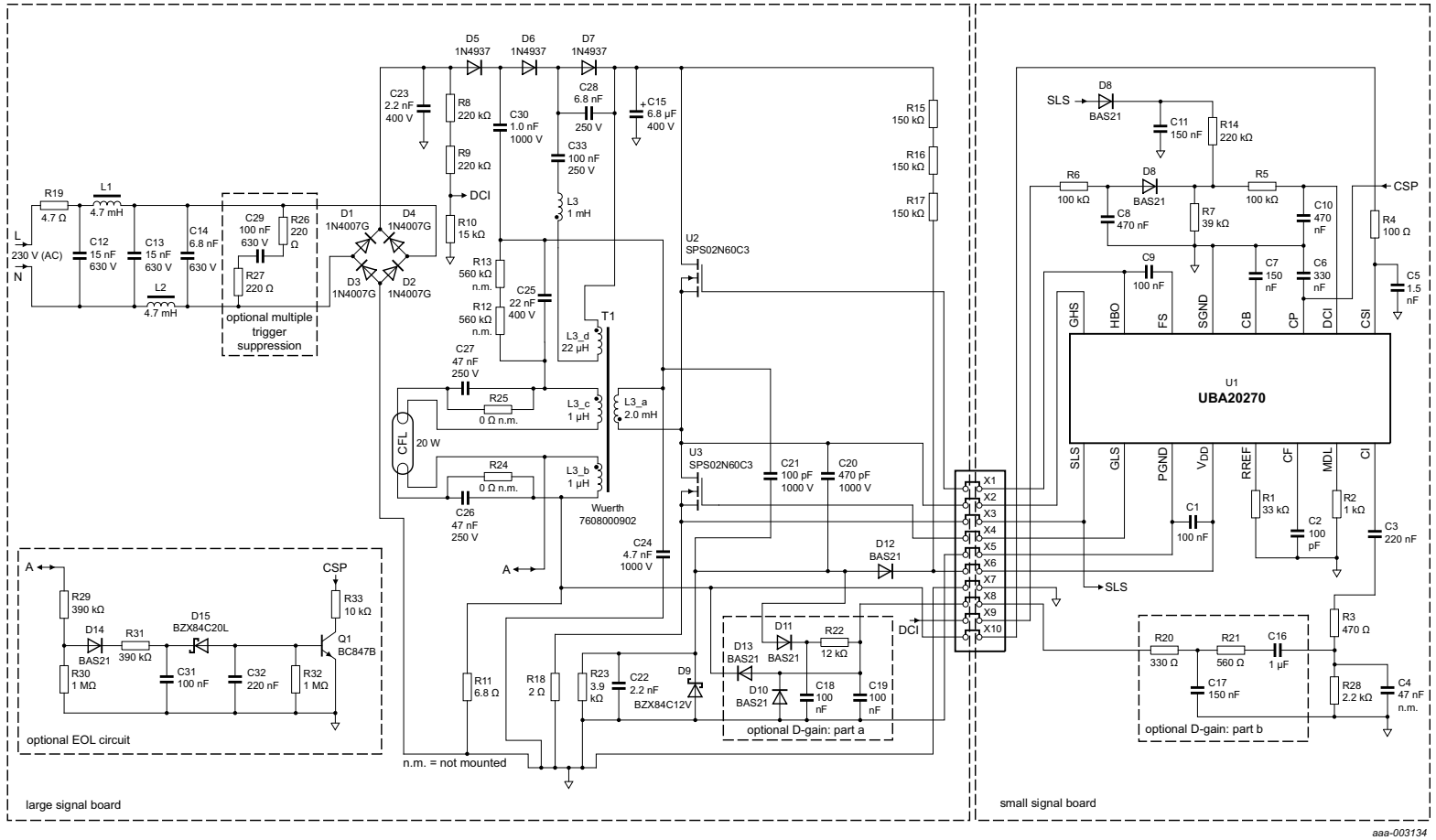


Fig 27. Schematic diagram: New NXP VSCP pump topology

This NXP topology has a separate floating current source pump which makes it possible to measure lamp current with common ground as reference.

7. Appendix 3: Inductive mode preheat calculations

The following values and equations are used for inductive mode preheat calculations. Half-bridge preheat winding are shown in Figure 28.

Where:

- V_{bus} = 350 V
- t_{hb} = 10 µH
- t_r = 0.5 µs

t_r is the time it takes to rise from the minimum to maximum value.

$$f_{hb} = \frac{1}{t_{hb}} \tag{38}$$

Where:

- f_{hb} = 100 kHz
- $\omega_{hb} = 2\pi \cdot f_{hb}$
- $\omega_{hb} = 628.319 \cdot 10^3$

$$\gamma = \frac{t_r}{t_{hb}} \cdot \pi \tag{39}$$

$\gamma = 0.157$

Where:

- $t = 0, 0.001 \cdot t_{hb}$ to $2 \cdot t_{hb}$

$$V_{hb(f)}(m) = j \cdot \frac{V_{bus}}{2 \cdot \pi \cdot \gamma} \cdot \frac{(-1)^m - 1}{m^2} \cdot sin(m \cdot \gamma) \tag{40}$$

Where:

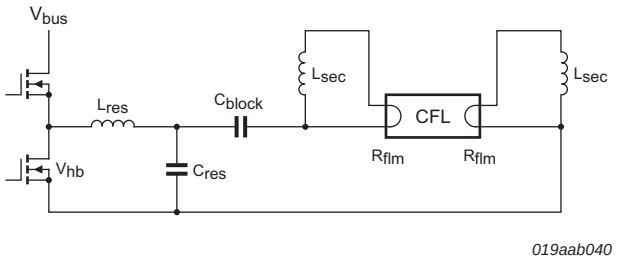
- $V_{hb(f)}$ (m) is the voltage $V_{hb(f)}$ as a function of m
- m = 1, 2 to 80

$$V_{hb(t)}(t) = 2 \cdot R_e \cdot \left[\sum_m (V_{hb(f)} \cdot (m) \cdot e^{j \cdot 2 \cdot \pi \cdot f_{hb \cdot m \cdot t}})\right] \tag{41}$$

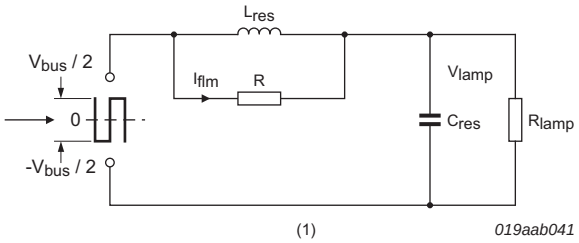
Where:

- $V_{hb(t)}$ (t) is the voltage $V_{hb(t)}$ as a function of time

Figure 28 (a) shows that the half-bridge voltage is supplied to the LC filter from which the inductor has two preheat windings. The circuit with the two preheat windings can be redrawn as shown in Figure 28 (b).



a. Inductor with two preheat windings



(1) Related equations see Equation 42, Equation 43 and Equation 43

b. Reduced circuit with two preheat windings

Fig 28. Half-bridge and preheat windings

$$R = \frac{1}{2} \cdot \frac{L_{res}}{L_{sec}} \cdot R_{flm} \tag{42}$$

$$R_{lamp} = \frac{V_{lamp}^{2}}{P_{lamp}} \tag{43}$$

$$I_{flm(f)}(m) = \frac{-(m \cdot \omega_{hb})^{2} \cdot L_{res} \cdot C_{res} \cdot \sqrt{\frac{L_{sec}}{L_{res}}}}{j \cdot 2 \cdot m \cdot \omega_{hb} \cdot L_{sec} + R_{flm} - (m \cdot \omega_{hb})^{2} \cdot L_{res} \cdot C_{res} \cdot R_{flm}} \cdot V_{hb(f)}(m) \tag{44}$$

Where:

- $I_{flm(f)}$ (m) is the current $I_{flm(f)}$ as a function of m
- $V_{hb(f)}$ (m) is the voltage $V_{hb(f)}$ as a function of m
- $L_{res} = 2.75\ mH \cdot 10^{-3}$
- $L_{sec} = 10\ \mu H \cdot 10^{-6}$
- $C_{res} = 4.7\ nF \cdot 10^{-9}$
- $R_{flm} = 50\ \Omega$

$$I_{flm(RMS)f} = \sqrt{2 \cdot \left[\sum_{m} \left(\left|I_{flm(f)}(m)\right|\right)^{2}\right]} \tag{45}$$

$I_{flm(RMS)f} = 0.18\ A$

$$I_{flm(t)} = 2 \cdot Re\left[\sum_{m}\left(I_{flm(f)}(m) \cdot e^{j \cdot 2 \cdot \pi \cdot f_{hb} \cdot m \cdot t}\right)\right] \quad (46)$$

8. Appendix 4: Cook book

With the release of three different types of the UBA2027x dimmable CFLi driver controller, nine different applications can be made. The design cook book gets the CFLi designer started quickly by selecting the IC and CFLi applications in accordance with the design parameters. From the given applications the CFLi designer can then start to use the calculation tools to find the proper component values.

The following chapters show design selection parameters obtained that are used for the application selection. Two flow diagrams are listed, one for each mains voltage that helps a CFLi designer select the right IC and application for a given CFL burner. The design selection steps are listed from left to right. The selection of the final application design is based upon basic burner and driver parameters.

Finally, a listing for each of the nine circuit diagrams that are the results of the design selection.

8.1 Selection variables

8.1.1 Nominal burner voltage

Ideally, the nominal RMS burner voltage is between 95 V and 110 V. The voltage can be measured directly at the burner, when the lamp is driven at 100 % ON and no dimmer is attached.

The RMS burner voltage is a very important parameter, as it is a primary parameter that determines the charge pump topology used in all applications. A charge pump topology is used to create the necessary triac hold currents which enable a CFL to work with standard incandescent light bulb dimmers. The lamp voltage also plays a role in the reactive losses in the resonant tank when the lamp is dimmed.

The voltage source current source topology is especially useful for dimming high-voltage amalgam lamps.

Later, the autotransformer circuit is used. Calculate the number of windings. Make sure that the nominal burner voltage + the voltage the autotransformer adds, is within the range of 95 V to 110 V (100 V typical).

Burners that exceed the 130 V nominal burner voltage are difficult to dim with more traditional voltage source charge pump topologies as shown in Figure 32, Figure 33, Figure 34.

8.1.2 Burner power

The nominal burner power divided by the RMS burner voltage gives the nominal burner discharge current. It is an indicator for the half-bridge IC current. The burner power is measured when the lamp is driven at 100 % ON. Obtain the value after 10 minutes of warming up. The burner current determines the resonant tank inductor size. Base the design of the resonant tank on the boosted output current (= 1.5 times the nominal output current) if the current boost option of the UBA2027x family is enabled.

8.1.3 IC dissipation

When the burner nominal burner power is known and the resonant inductor is calculated, a proper estimation can be made of the total half-bridge current. The total RMS half-bridge current multiplied by the R_{DSon} of the internal MOSFETs at a junction temperature of 150 °C, and an application ambient temperature of 105 °C (typical), must be ≤ 0.5 W. Use a UBA20270 with external MOSFET transistors if the RMS power > 0.5 W. Preferably, the RMS half-bridge current stays below 500 mA for the UBA20271 or below 300 mA for the UBA20272.

The autotransformer offers a simple solution to lower IC dissipation by lowering the voltage across the resonant tank capacitor therefore lowering the reactive current.

8.1.4 Circuit topology

Preferably, the voltage source topology is used to dim compact fluorescent lamps on a triac dimmer as the dominant current source draws the necessary hold current at nominal and minimal dimmed lamps. The voltage source enforces an enlarged conduction angle to keep the triac ON until the end of the mains period. It draws hold current at maximum dimmed lamps. Two voltage source current source topologies are presented. One with a separate current transformer to sense lamp current. And one that uses an extra winding on the resonant inductor to create a floating current source. A separate current transformer to measure lamp current is not required. However, the resonant transformer requires extra winding and increases in size.

8.2 Selection guides

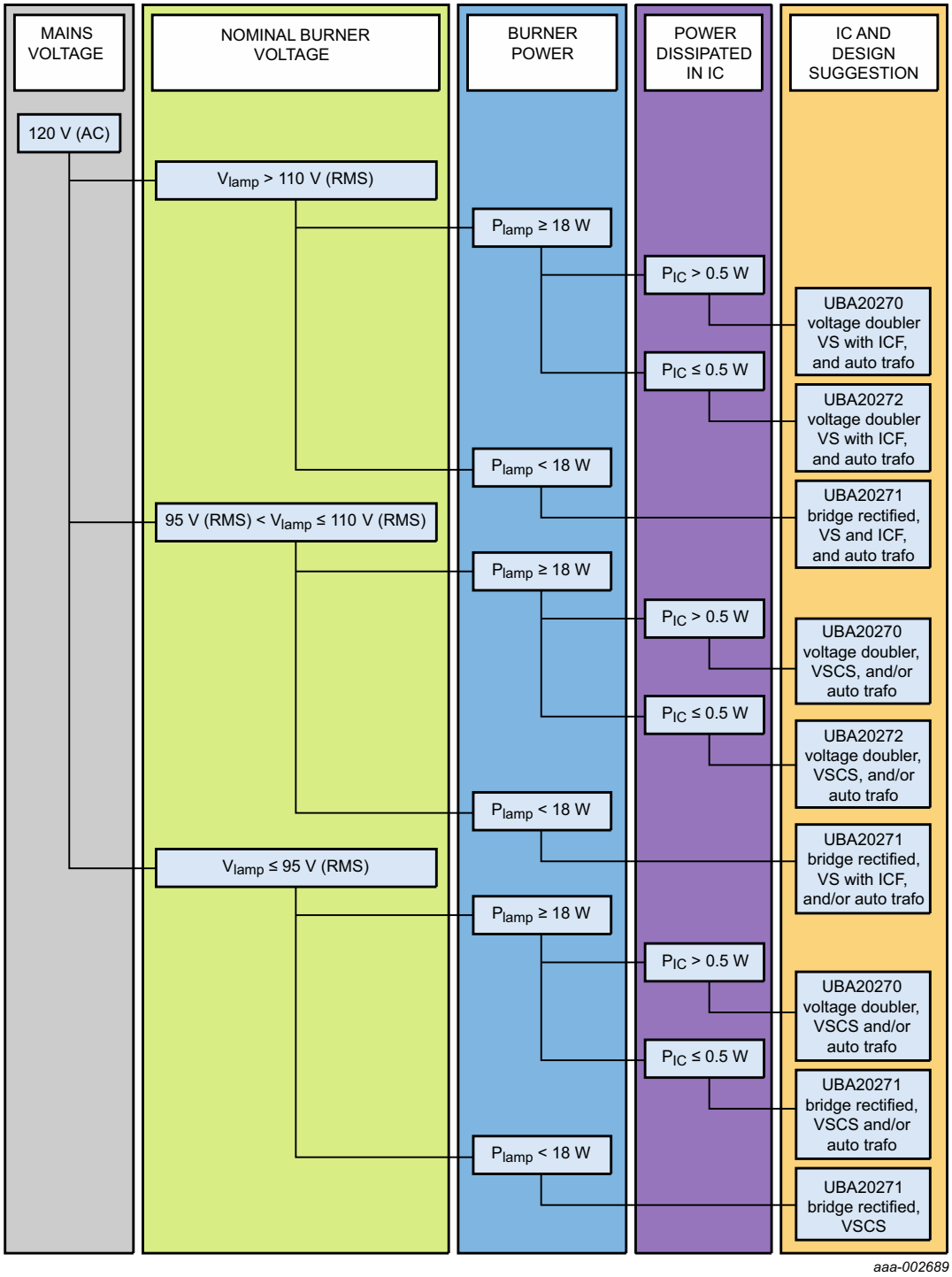


Fig 29. 120 V main

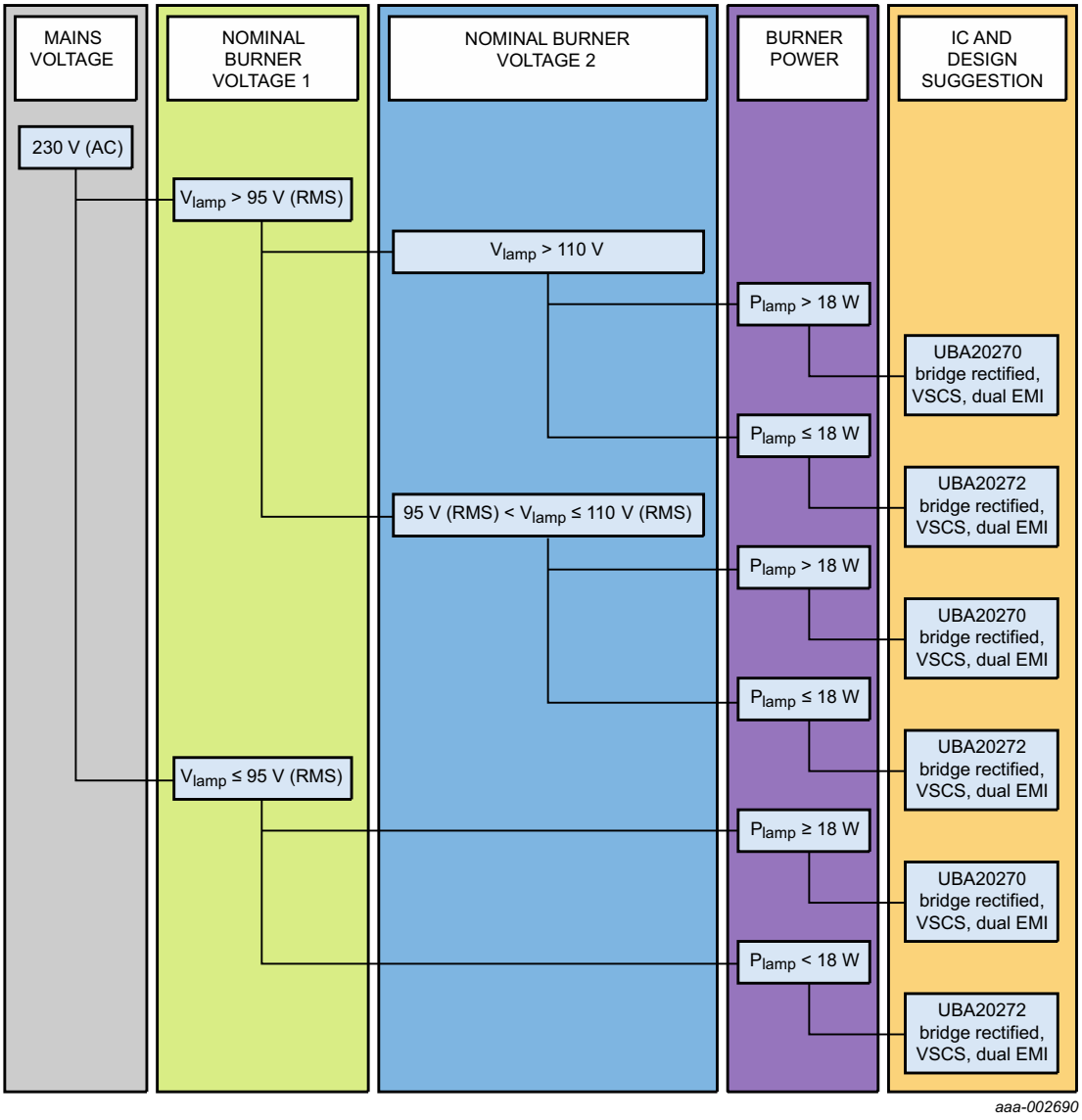


Fig 30. 230 V main

8.3 Application diagrams

8.3.1 Bridge rectified voltage source charge pump with ICF 120 V

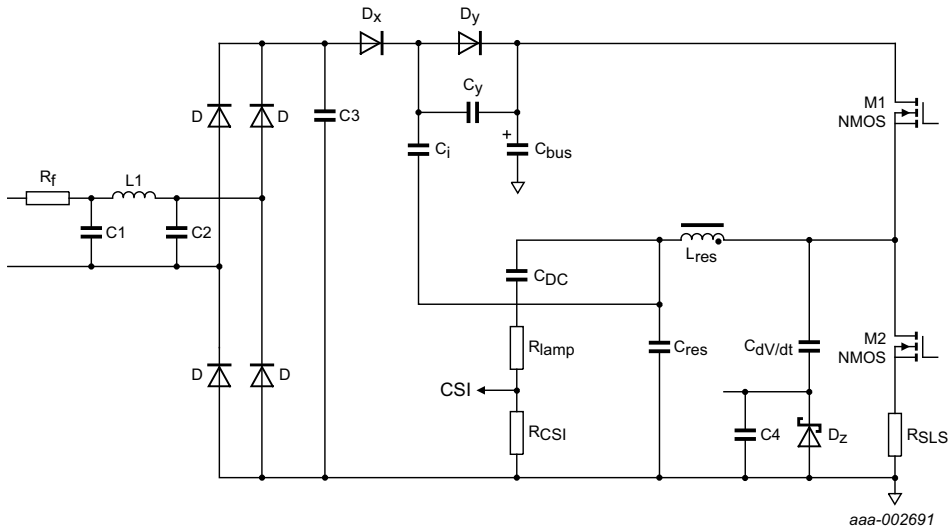


Fig 31. Single power feedback with single stage EMI filter

Typical applications:

- UBA20271; 120 V mains; up to 18 W

Advantages:

- Low component count
- Medium-voltage lamps
- Crest factor = 2.2

Disadvantages:

- High lamp voltage sensitivity
- Moderate power factor
- Lower hold current undimmed lamp
- more sensitive to multiple triggers

8.3.2 Bridge rectified voltage source charge pump with ICF and autotransformer 120 V

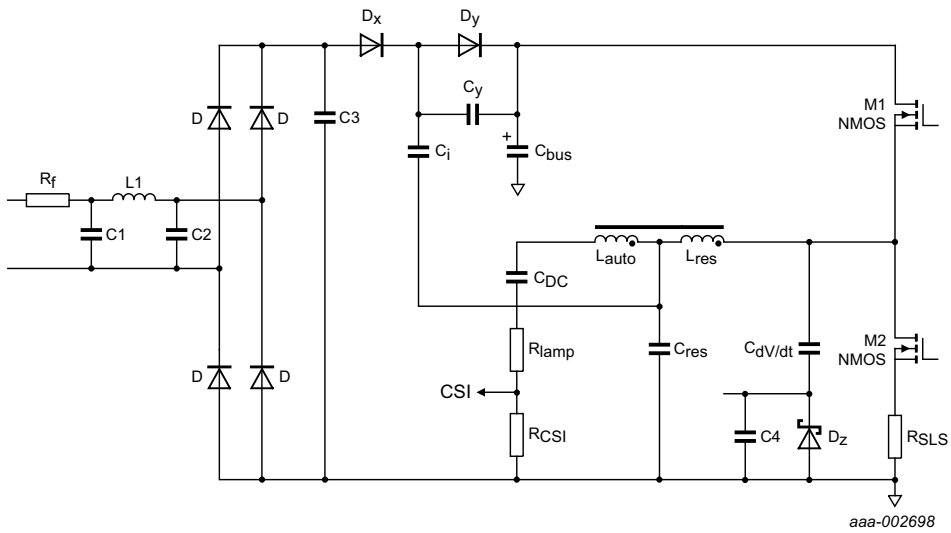


Fig 32. Single power feedback with improved crest factor to lower bus voltage stress, single stage EMI filter and autotransformer to improve efficiency

Typical applications:

- UBA20271; 120 V mains; up to 18 W

Advantages:

- Low component count
- Good for medium-voltage lamps
- Better efficiency (improves overall efficiency)
- Crest factor = 2.1

Disadvantages:

- High lamp voltage dependency/sensitivity
- Extra winding on resonant transformer required

8.3.3 Voltage doubler and voltage source charge pump with ICF 120 V

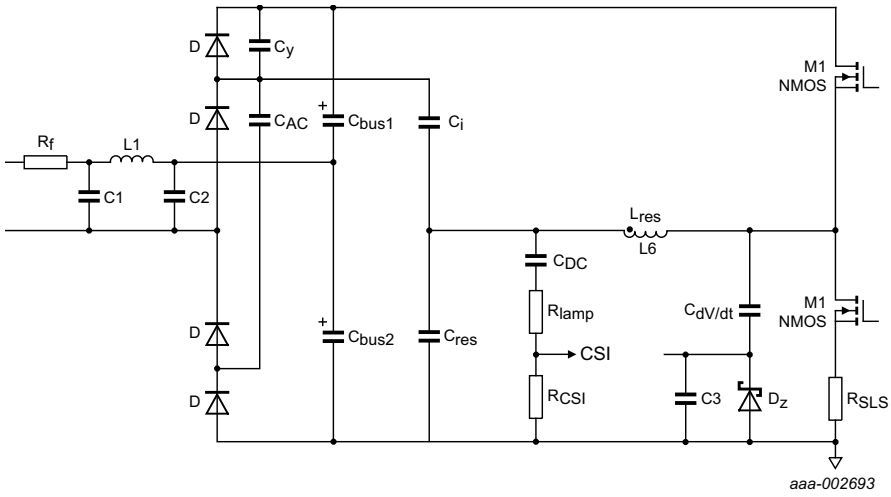


Fig 33. Single power feedback with single stage EMI filter, autotransformer and improved crest factor lower stress on bus voltage at light load

Typical applications:

- UBA20270; 120 V mains; up to 23 W

Advantages:

- Low component count
- Higher power medium-voltage lamps
- Crest factor = 2.2

Disadvantages:

- High lamp voltage sensitivity
- Two buffer capacitors

8.3.4 Voltage doubler and voltage source charge pump with ICF and autotransformer 120 V

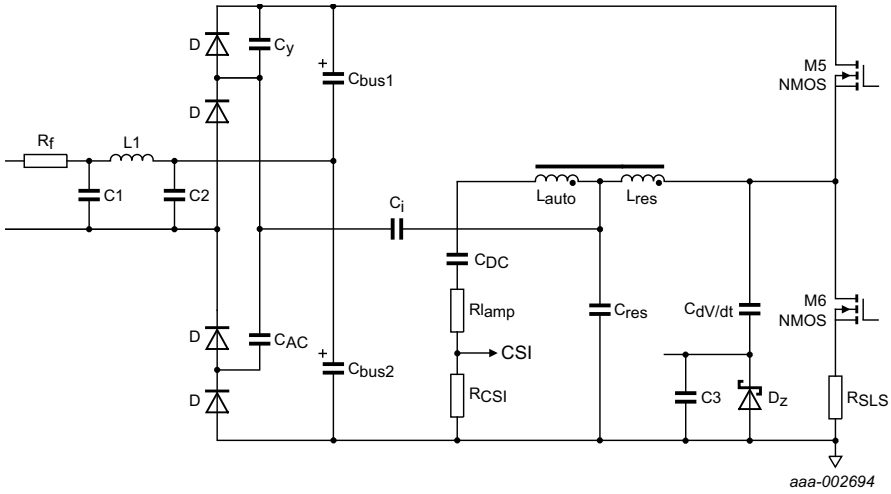


Fig 34. Single power feedback with single stage EMI filter, improved crest factor lower stress on bus voltage at light load and autotransformer to improve efficiency

Typical applications:

- UBA20270; 120 V mains; up to 23 W

Advantages:

- Low component count
- Higher power medium-voltage lamps
- Better efficiency
- Crest factor = 2.2

Disadvantages:

- High lamp voltage sensitivity
- Two buffer capacitors
- Extra winding on resonant transformer

8.3.5 Voltage doubler and voltage source current source charge 120 V

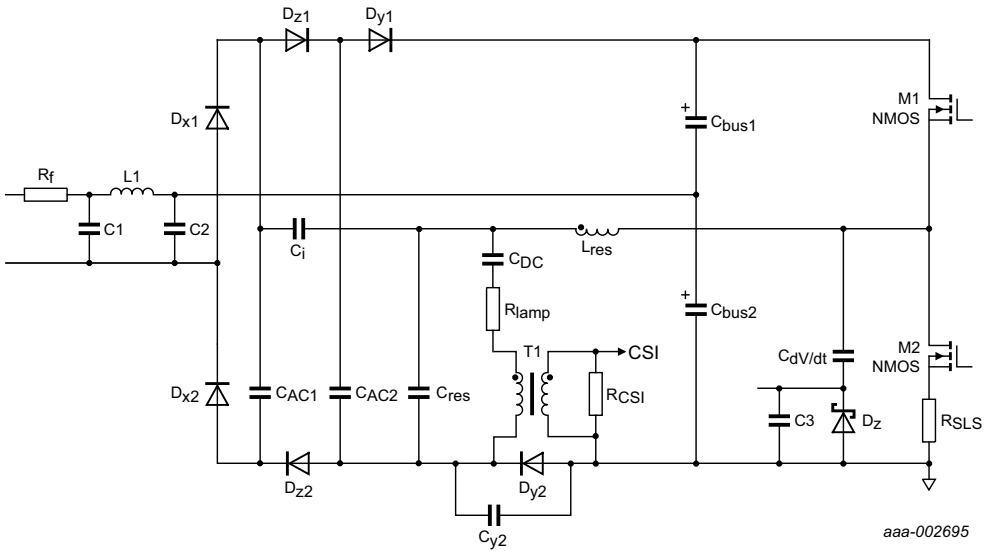


Fig 35. Double power feedback with single stage EMI filter and autotransformer to improve efficiency

Typical applications:

- UBA20270; 120 V mains; up to 23 W

Advantages:

- Low lamp voltage sensitivity
- Suitable for high-voltage lamps
- Crest factor = 1.75

Disadvantages:

- Extra 1:1 current transformer required

8.3.6 Bridge rectified voltage source current source charge pump 120 V

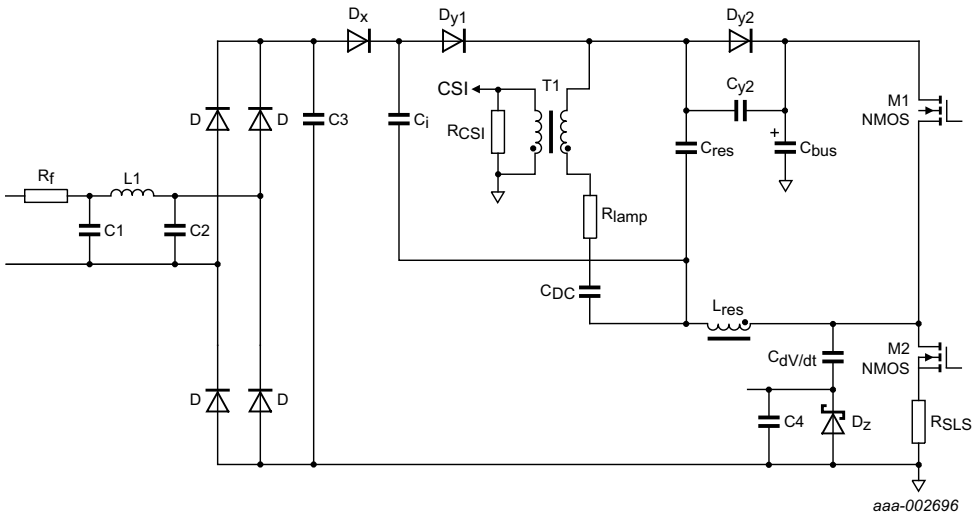


Fig 36. Double power feedback with single stage EMI filter

Typical applications:

- UBA20271; 120 V mains; up to 18 W

Advantages:

- Low lamp voltage sensitivity
- Works with low to medium-voltage amalgam lamps
- Less sensitive to parasitic capacitor in coupling from half-bridge output to CSI input L_{res}
- Good THD
- Crest factor = 1.75

Disadvantages:

- Extra 1:1 current transformer required

8.3.7 Bridge rectified voltage source current source charge pump with autotransformer 120 V

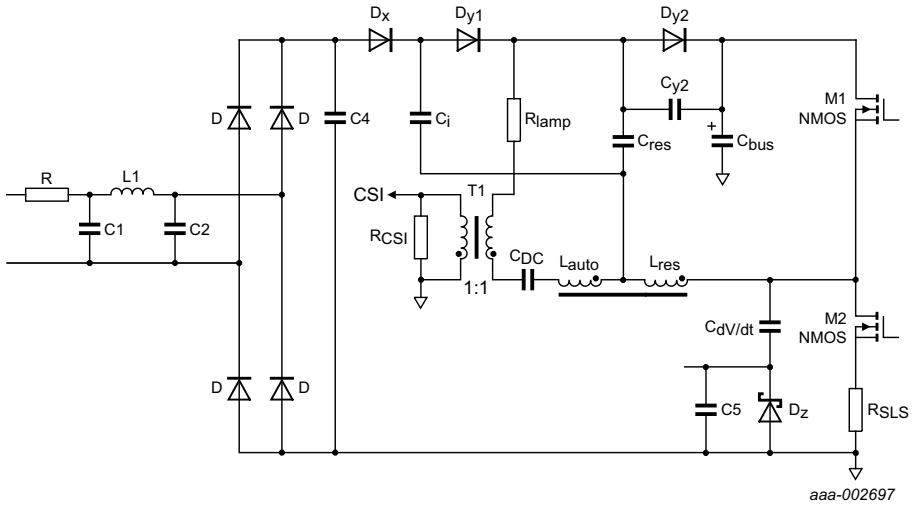


Fig 37. Double power feedback with single stage EMI filter and autotransformer to improve efficiency

Typical applications:

- UBA20271; 120 V mains; up to 18 W
- UBA20270; > 18 W; external MOSFET

Advantages:

- Low lamp voltage sensitivity
- Works with medium to high-voltage amalgam lamps
- High PF (> 0.85)
- Low THD (< 40 %)
- Better efficiency
- Less sensitive to parasitic capacitor coupling from half-bridge output to CSI input, resulting in deeper and stable dimming
- Lower half-bridge current
- Crest factor = 1.75

Disadvantages:

- Extra 1:1 current transformer required
- Extra winding on resonant transformer

8.3.8 Bridge rectified voltage source current source 230 V

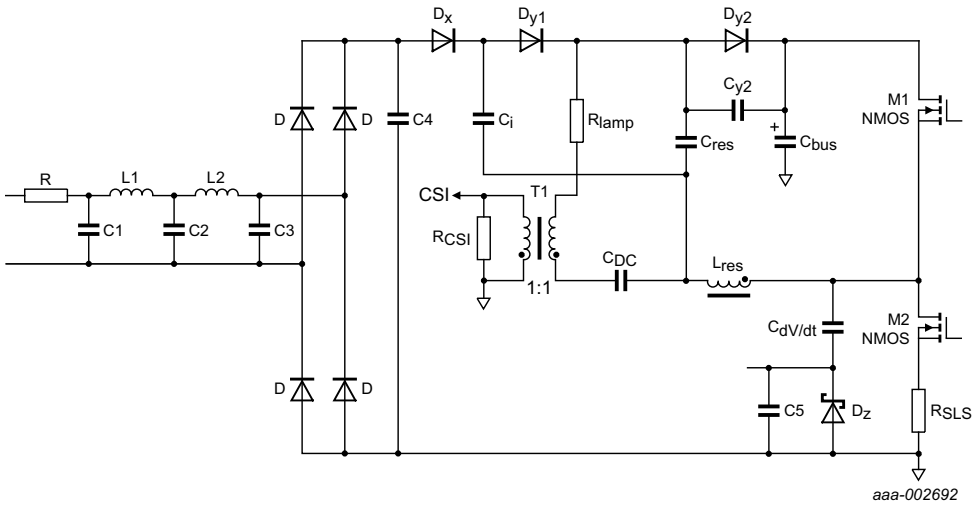


Fig 38. Double power feedback with dual-stage EMI filter and autotransformer to improve efficiency

Typical applications:

- UBA20272; 230 V mains; up to 18 W
- UBA20270; > 18 W; external MOSFET

Advantages:

- Low lamp voltage sensitivity
- Works with medium to high-voltage amalgam lamps
- High PF (> 0.85)
- Low THD (< 40 %)
- Not sensitive to parasitic capacitor coupling from half-bridge output to CSI input, resulting in deeper and stable dimming
- Crest factor = 1.75

Disadvantages:

- Extra 1:1 current transformer required

8.3.9 Bridge rectified voltage source current source charge pump with lamp to ground 230 V

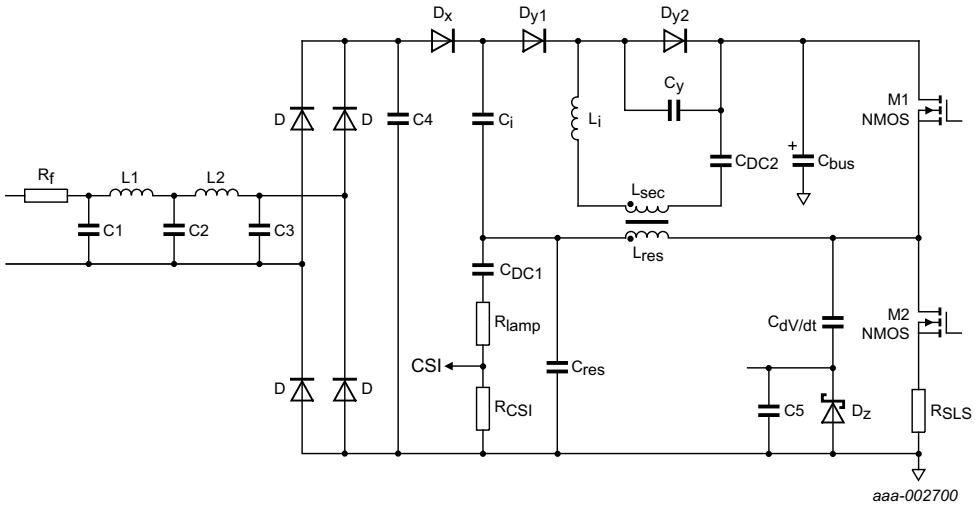


Fig 39. Double power feedback with dual stage EMI filter, auto and floating current source, no current transformer required and lamp to ground operation

Typical applications:

- UBA20272; 230 V mains; up to 18 W
- UBA20270; > 18 W; external MOSFET

Advantages:

- No extra 1:1 current transformer required
- Good for low to medium-voltage lamps
- Less overpumping

Disadvantages:

- Lamp voltage sensitivity
- Extra inductor required
- Extra winding on resonant transformer required

8.3.10 Bridge rectified voltage source current source charge pump with lamp to ground 120 V

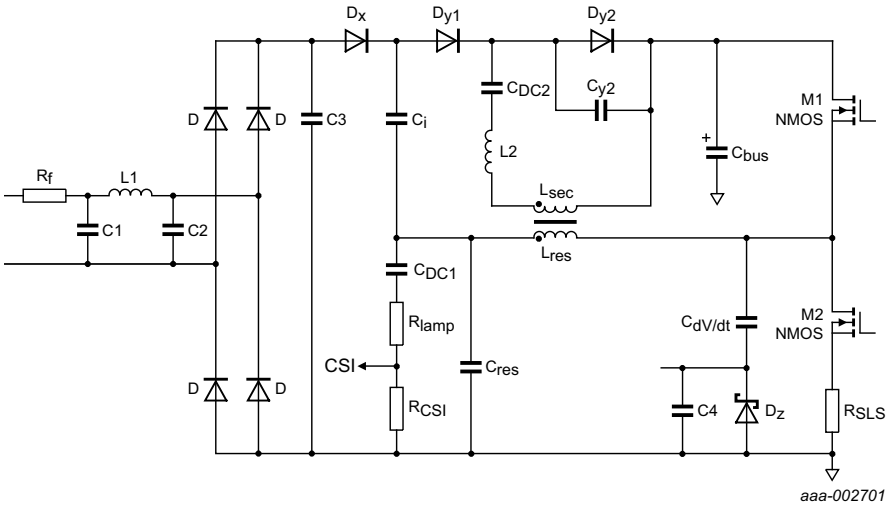


Fig 40. Double power feedback with single stage EMI filter, auto and floating current source, no current transformer required and lamp to ground operation

Typical applications:

- UBA20271; 120 V mains; up to 18 W

Advantages:

- No extra 1:1 current transformer required
- Good for low-voltage lamps
- Less overpumping

Disadvantages:

- Lamp voltage sensitivity
- Extra inductor required
- Extra winding on resonant transformer required

9. Abbreviations

Table 5. Abbreviations

Acronym	Description
CFL	Compact Fluorescent Lamp
CSP	Coil Saturation Protection
CMD	Capacitive Mode Detection
EMI	ElectroMagnetic Interference
OCP	OverCurrent Protection
OVP	OverVoltage Protection
PF	Power Factor
PFC	Power Factor Correction
RLC	Resistance, Inductance, Capacitance
SoS	Sum of Squares
UVLO	UnderVoltage LockOut
VSCP	Voltage Source Charge Pump
VSCS	Voltage Source Current Source
VSCS-CP	Voltage Source Current Source Charge Pump
ZVS	Zero Voltage Switching

10. References

[1] **AN10803 —** Application note: triac dimmable CFL application using the UBA2028/UBA2014/UBA2027.

[2] **UBA20270 and UBA20271/2 —** Data sheets: dimmable CFL control ICs.

[3] **Power factor correction 1989 IEEE —** Current waveform distortion in power factor correction circuits employing discontinuous mode boost converters.

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