AN10958
Fluorescent lamp driver with PFC using the UBA2015/16 family

Rev. 2 — 9 August 2012   **Application note**

Document information

Info	Content
Keywords	UBA2015, UBA2015A, UBA2016A fluorescent lamp driver, PFC
Abstract	This application note describes designs using IC family UBA2015, UBA2015A and UBA2016A for common ballast topologies. The IC is a controller used in electronic ballast for fluorescent lamps incorporating controllers and NMOST drivers for Power Factor Correction (PFC) and the half-bridge circuit. The high-voltage fluorescent lamp ballast controller drives a zero-voltage switching resonant topology. The lamp controller module includes a high-voltage level shift circuit and several protection features. The protection features include hard switching/capacitive mode protection, half-bridge overcurrent (coil saturation) protection, lamp overvoltage (lamp removal) protection and temperature protection. In addition to the lamp controller, the IC also contains a PFC controller. The quasi-resonant operation guarantees efficient operation of the PFC circuit. Overcurrent protection, overvoltage protection and demagnetization sensing ensure safe operation under all conditions. The brownout protection of the PFC controller reduces the half-bridge frequency to prevent excessive currents. The proprietary high-voltage BCD power logic process enables efficient, direct start-up from the rectified universal mains voltage. The IC can drive half-bridge circuits with a supply voltage up to 600 V (AC). The PFC and lamp controller combination makes the IC suitable for dimmable or fixed current output fluorescent ballasts with a PFC for AC mains voltages up to 390 V.

Revision history

Rev	Date	Description
v.2	20120809	second version
v.1	20110620	first version

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AN10958

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Application note **Rev. 2 — 9 August 2012** **2 of 56**

1. Introduction

1.1 General IC description

Today's market demands high-quality, reliable, lightweight, small and efficient electronic High Frequency (HF) ballast with lamp end-of-life detection. The high-end market segment also requires dimming functionality.

Electronic ballasts provide high efficiency performance because the lamp is operated at high frequencies above 10 kHz. At this frequency, the lamp is more efficient when compared to a magnetic ballast operating at 50 Hz to 60 Hz. High frequency operation enables smaller magnetic components in the electronic ballast to be smaller. This reduction makes electronic ballasts are approximately one fifth the weight of magnetic ballasts.

The UBA2015, UBA2015A and UBA2016A combines Power Factor Correction (PFC) and half-bridge controller in one IC which reduces the component cost significantly and increases reliability. It has several protection mechanisms such as overvoltage/no ignition, coil saturation, overtemperature and on some pins, open/short protection to guarantee reliable and safe operation.

The integrated dimming option allows control of the lamp current down to 1 % of the nominal lamp current. The integrated double-sided rectification of the lamp current feedback signal and a control loop compensation network pin allows stable lamp operation and achieves good dimming performance.

The IC is intended for fluorescent lamp ballast with fixed or dimmable light output, with PFC for AC mains voltages up to 390 V.

A feature list, block diagram and flow chart for the IC are provided in the IC data sheet.

1.2 Basic electronic ballast circuit

The feedback signals are not shown.

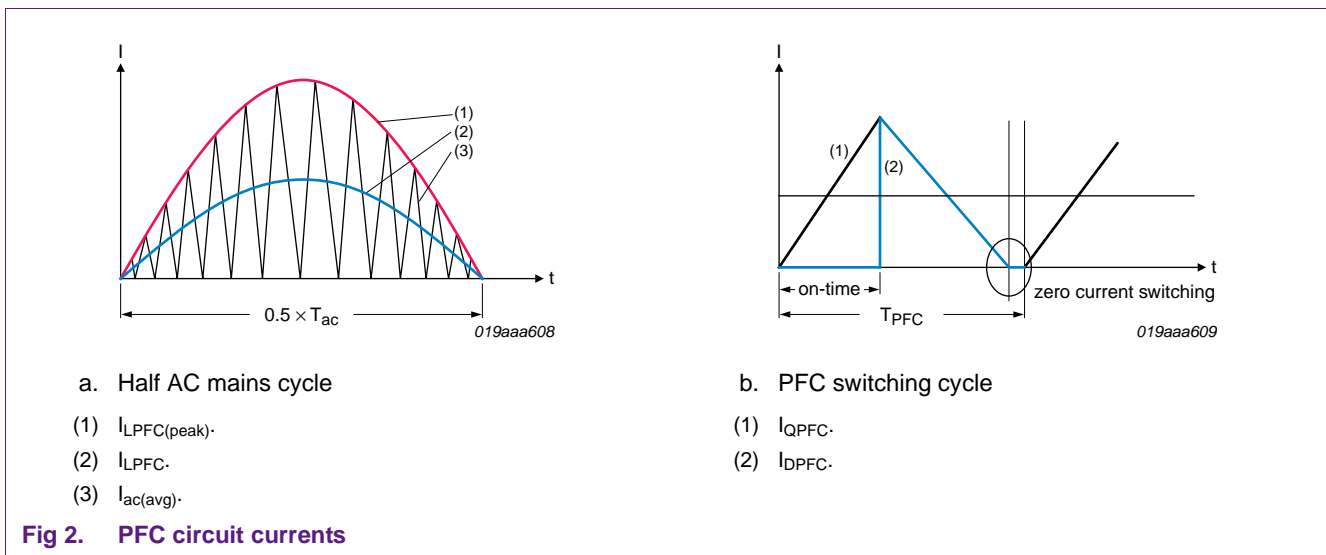**Fig 1.   Basic electronic ballast circuit for inductive heating topology**
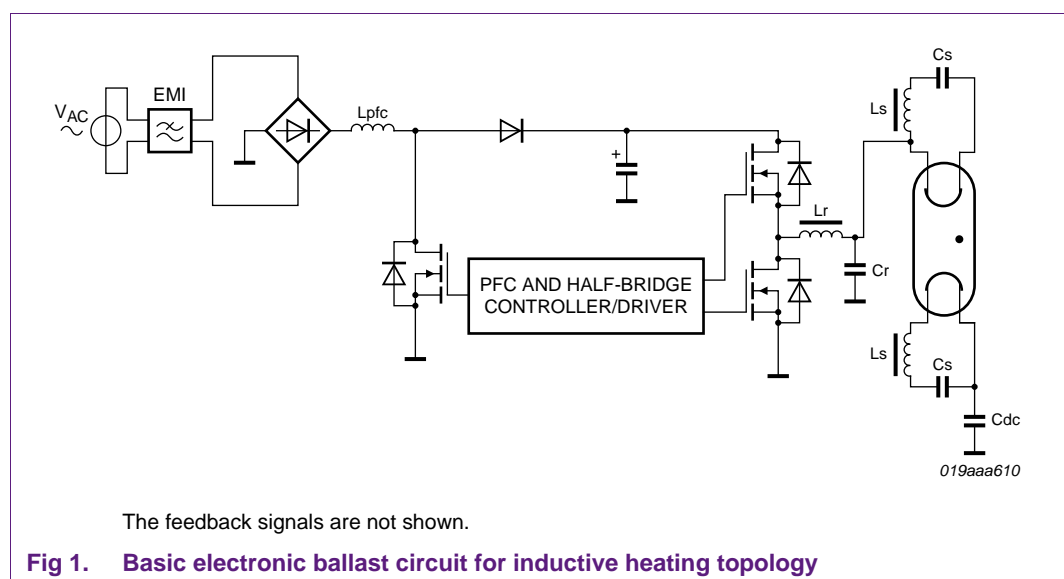
1.2.1 Power factor correction

Lighting applications above 25 W need a PFC circuit to fulfill the Total Harmonic Distortion (THD) and Power Factor (PF) requirements. The PFC circuit is actually a boost or step-up converter, therefore the output voltage must be higher than the peak AC mains voltage. The PFC provides a fixed DC output voltage which helps to create a better defined half-bridge circuit and therefore longer lamp life. A high DC voltage also results in more efficient ballasts for lamps operating at higher voltages.

The PFC operates at a fixed on-time over one mains cycle. The PFC circuit inductor peak current follows the sinusoidal mains waveform. EMI filtering averages the PFC switching current and blocks common mode currents (see Figure 2).

The frequency limit also reduces switching losses using valley skipping are reduced which is very effective at low AC mains input voltage and medium to low output load conditions.

a. Half AC mains cycle

(1) $I_{LPFC(peak)}$.
(2) I_{LPFC}.
(3) $I_{ac(avg)}$.

b. PFC switching cycle

(1) I_{QPFC}.
(2) I_{DPFC}.

Fig 2. PFC circuit currents

A fixed output voltage has the advantage that the half-bridge circuit can be designed for a high input voltage. The fixed bus voltage makes the half-bridge design more efficient for lamps with a high operating voltage such as T5 lamps.

1.2.2 Inductive heating half-bridge and ballast

Refer to Figure 1. The capacitor (C_r) across the lamp is the resonant capacitor and inductor (L_r) is the resonant inductor. The capacitor in series with the lamp is the DC blocking capacitor (C_{DC}). Before ignition, the electrodes are preheated at a predefined half-bridge current (UBA2016A) or frequency (UBA2015).

After preheat, the lamp voltage increases while sweeping the half-bridge operating frequency down to the resonant frequency. Finally, the lamp ignites when the lamp ignition voltage is reached. When the lamp does not ignite, the switching frequency ramp down is stopped to avoid damage to components. Then a new ignition attempt is started. After a maximum of two ignition attempts, the IC enters a standby mode.

Once the lamp is ignited, the resonant tank and switching frequency limit the amount of current through the lamp. The half-bridge operating frequency controls the lamp current.

AN10958

Application note **Rev. 2 — 9 August 2012** **4 of 56**

1.2.3 IC family overview

This family of half-bridge controller ICs comprises three functionally different versions. All versions are available in both SO20 and DIP20 packages. The functional differences are explained in Table 1.

Table 1.   IC family overview

Function	UBA2015	UBA2015A	UBA2016A
PFC controller	yes	yes	yes
Preheat operation	current controlled and fixed frequency	current controlled and fixed frequency	current controlled
Boost function	no	no	yes
Dim function	no	yes	yes

1.2.3.1 Preheat operation

The current controlled preheat operation is intended for a series-resonant topology where the half-bridge current is equal to the filament currents. The accuracy is independent of the LC tank tolerances. Therefore, the preheat frequency is closer to the maximum preheat voltage allowed. As a result, the preheat current is higher than with fixed frequency preheat.

The fixed frequency preheat operation is intended for multi-lamp ballasts where the total half-bridge current is not equal to the filament current. For example: the half-bridge current is reduced by a factor of two when a lamp is removed in a two-lamp ballast with conventional series-resonant topology.

1.2.3.2 Boost function

The boost function is used for amalgam lamps or outdoor applications to provide a rapid light output run-up time. The run-up time is the time a discharged lamp takes to reach 80 % of the nominal light output. The boost function allows the lamp to be operated at 1.5 to 2.0 times its nominal current. As a result, the lamp reaches the optimum operating temperature sooner. The boost is applied at ballast power-on. A capacitor in the application determines the boost time.

1.2.3.3 Dim function

The dim function is intended for energy harvesting or light reduction.

2.   Basic circuit description

This section describes the deep dimming ballast in the inductive series-resonant topology shown in Figure 1. The inductors L_s and L_r are coupled, therefore the current through the filaments is inductively coupled to the current through L_r in the LC tank.

A complete electronic schematic of a ballast with dimming and boosting using the UBA2016A is shown in Figure 3. This application note uses this schematic as a guide.

AN10958

Application note **Rev. 2 — 9 August 2012** **5 of 56**

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Fluorescent lamp driver with PFC using the UBA2015/16 family
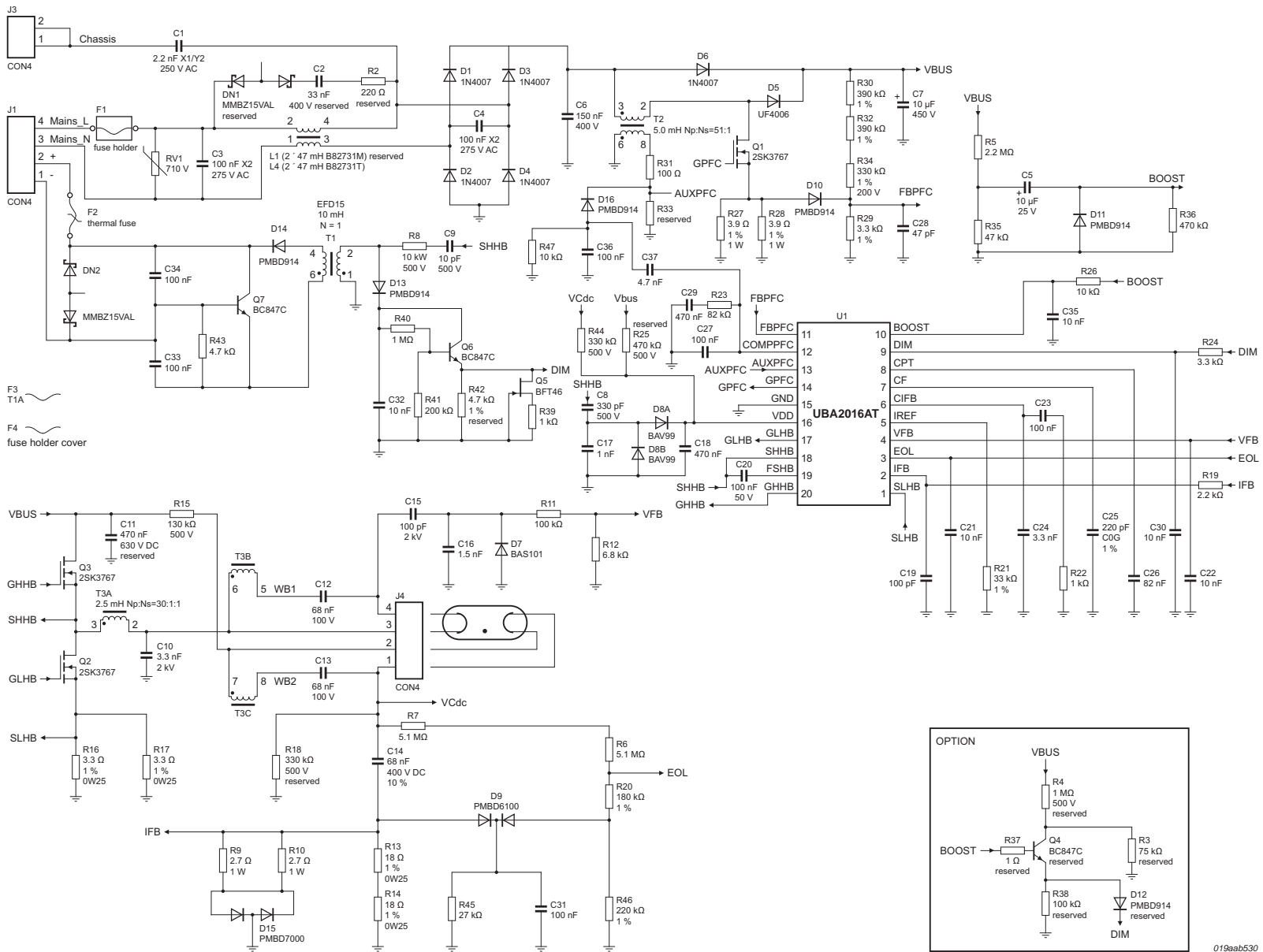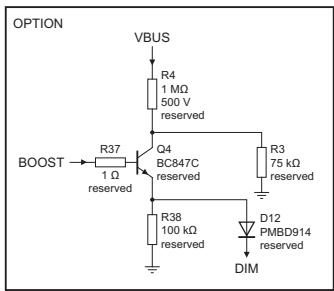
AN10958

Fig 3.   Complete electronic ballast circuit for inductive series-resonant topology

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The circuit diagram of the PFC section is shown in Figure 4. Signal FBPFC is the feedback to the controller. The bus voltage VBUS connects to the half-bridge circuit. The AUXPFC signal is fed to the controller. The GPFC is the gate drive signal from the controller.
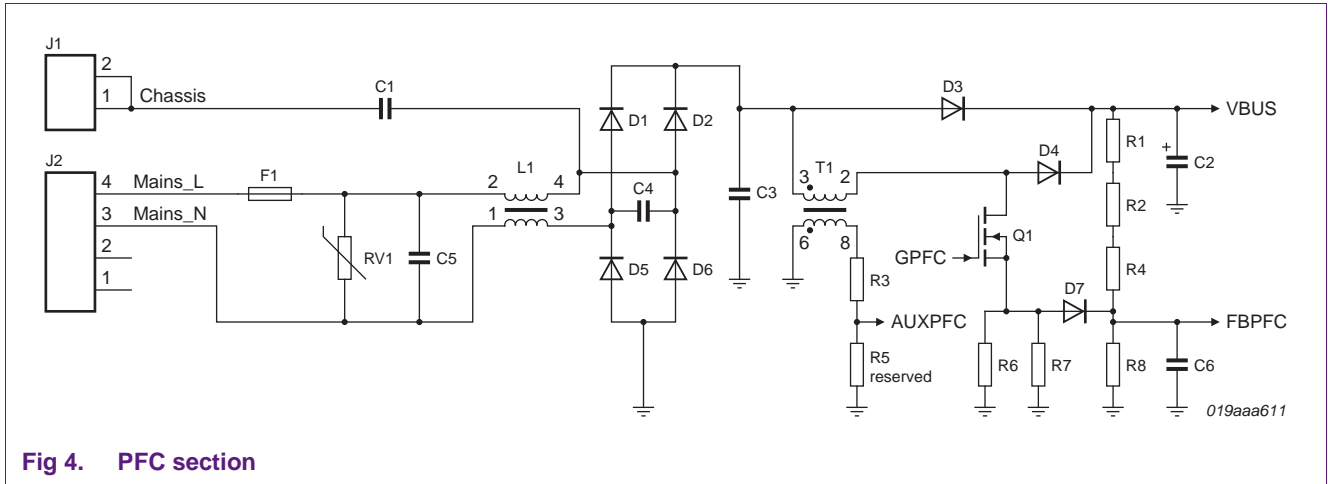

Fig 4.   PFC section

The inductive mode series-resonant topology is shown in Figure 5. An inductor coupled to the resonant inductor heats the electrodes. The bus voltage is from the PFC circuit output. GHHB and GLHB are the gate drive signals from the controller. SHHB is connected to the input of the controller and provides a supply for the controller during oscillation states. SLHB is connected to the input of the controller. The VFB signal is the lamp voltage feedback. IFB is the lamp current feedback. EOL is the feedback of the DC blocking capacitor C12. The V_{CDC} signal provides the start-up current to the VDD pin.
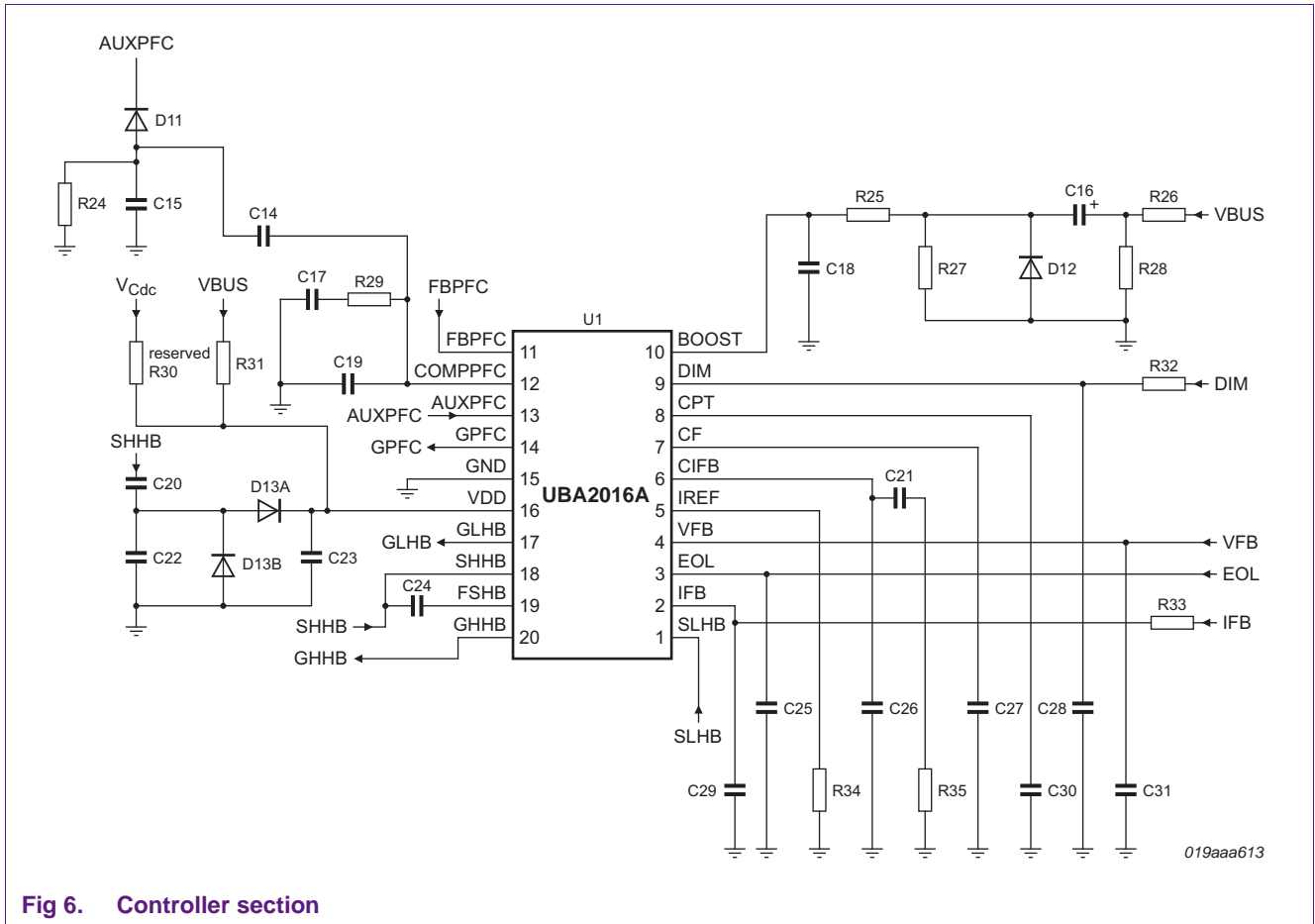
Fig 5. **Half-bridge section inductive mode series-resonant topology**

The circuit diagram of the PFC and half-bridge controller is shown in Figure 6. AUXPFC, FBPFC and GPFC connect to the PFC circuit. The VDD pin receives the start-up current from V_{CDC} (support relamp) or VBUS (no support for relamp). During oscillation states, the VDD pin is supplied by the dV/dt supply generated using the SHHB pin. The signals SHHB, GHHB, GLHB, and SLHB connect to the half-bridge NMOSTs. The boost signal is generated from the VBUS voltage. The dimming input circuit generates the DIM signal. The VFB signal is the lamp voltage feedback signal. IFB is the lamp current feedback signal. EOL is the voltage of the DC blocking capacitor used for lamp end-of-life detection. The start-up resistor R31 can be connected to the output of the bridge rectifier to reduce the power cycle time.

AN10958

Application note **Rev. 2 — 9 August 2012** **8 of 56**

Fig 6. **Controller section**

The dim control input circuit is described in Figure 7. An AC current from node SHHB of the half-bridge circuit is fed through the galvanic isolation transformer T3. The voltage from an external DC voltage source of 0 V to 10 V can be connected to the user side of T3. Due to the current through T3, the transformer voltage is clamped to the input voltage. The clamped voltage is sensed on the ballast side of T3 and filtered. The DIM signal is fed to the controller.
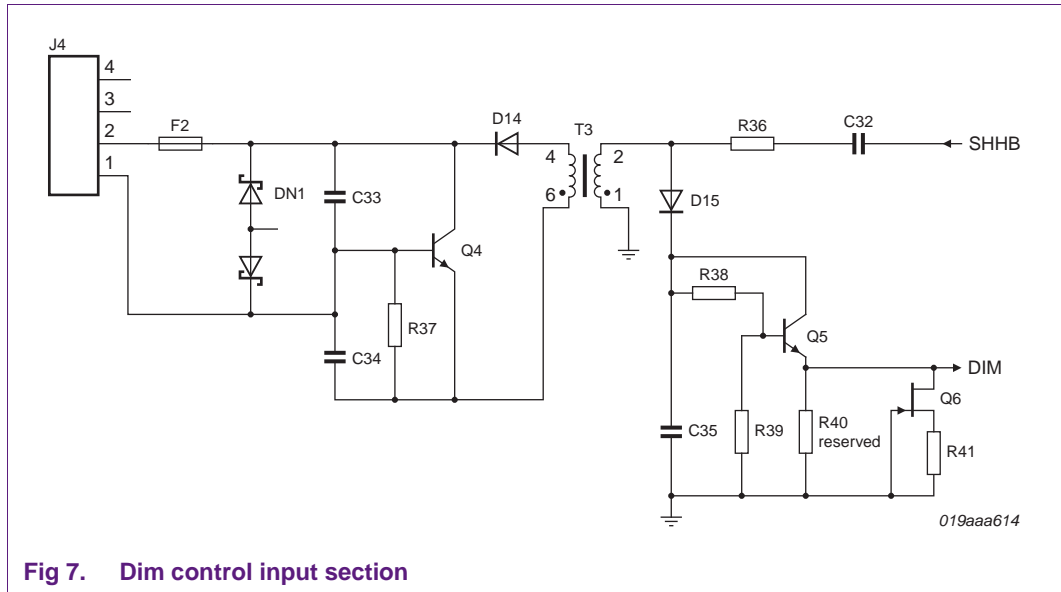
Fig 7. Dim control input section

3. Pin-to-pin component selection

The functionality of the ballast circuit subblocks is described in Table 2 to Table 4 based on the functions assigned to each pin.

Table 2. **PFC function pins**

Symbol	Pin	Description
FBPFC	11	PFC voltage feedback, overvoltage protection, overcurrent protection, open/short protection; see Section 3.12 on page 34
COMPPFC	12	PFC voltage control loop compensation network, input of on-time modulator; see Section 3.13 on page 36
AUXPFC	13	demagnetization detection, THD wave shaping, open pin protection; see Section 3.14 on page 37.
GPFC	14	PFC gate drive; see Section 3.15 on page 38

Table 3. **Half-bridge function pins**

Symbol	Pin	Description
SLHB	1	preheat current regulation, coil saturation protection; see Section 3.1 on page 11
IFB	2	lamp current feedback input, lamp-on detection, internal lamp current rectifier, lamp overcurrent detection; see Section 3.2 on page 13
EOL	3	lamp end-of-life detection; see Section 3.3 on page 18
VFB	4	lamp voltage feedback, lamp overvoltage detection, open/short protection; see Section 3.4 on page 21
CIFB	6	input of the internal VCO, time constant of the lamp current control loop, ignition frequency ramp down speed after preheat; Section 3.6 on page 26
CF	7	timing capacitor of oscillator; Section 3.7 on page 27
CPT	8	preheat timer, fault timer, open/short protection; see Section 3.8 on page 28

AN10958

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Application note

Rev. 2 — 9 August 2012

10 of 56

Table 3. **Half-bridge function pins** *…continued*

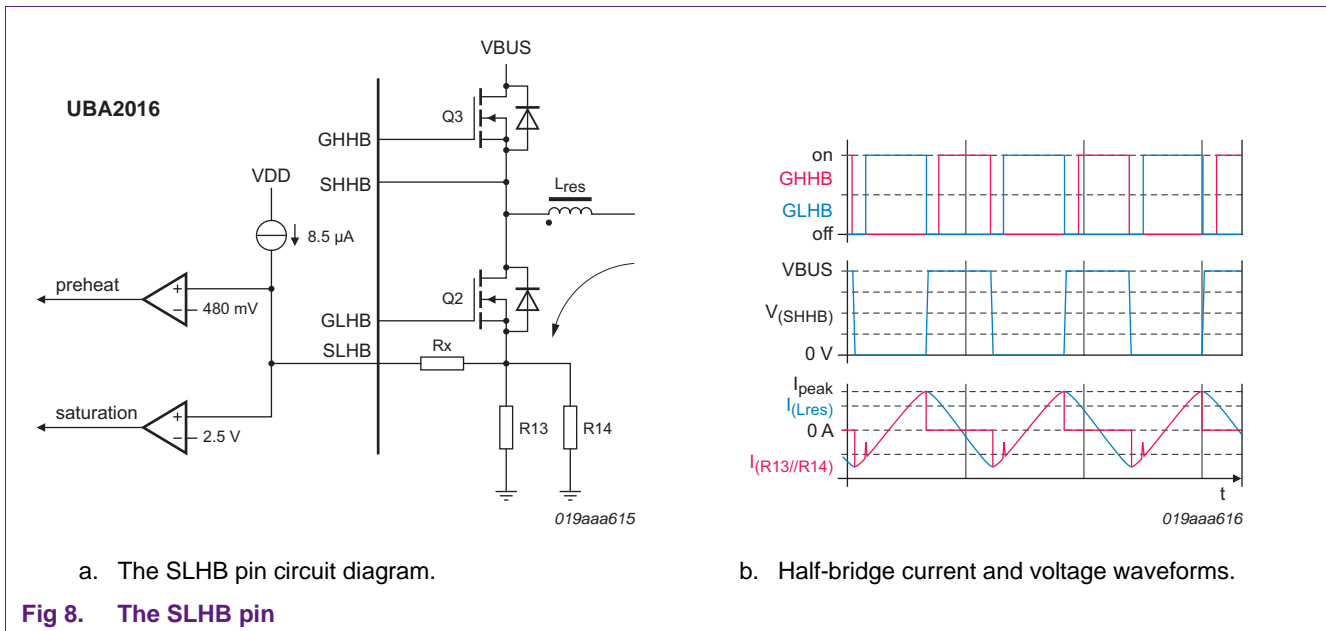| Symbol	Pin	Description
DIM	9	dimming input, reducing the lamp-on-detection threshold; see Section 3.9 on page 29
BOOST	10	lamp current boost input (UBA2016A); see Section 3.10 on page 30
PH/EN	10	preheat frequency setting and enable/disable (UBA2015/UBA2015A); see Section 3.11 on page 33
GLHB	17	low-side half-bridge gate driver; see Section 3.18 on page 43
SHHB	18	hard switching regulation and protection input, ground of high-side driver, source of the dV/dt supply; see Section 3.19 on page 43
FSHB	19	floating supply of the high-side driver; see Section 3.20 on page 43
GHHB	20	high-side half-bridge gate driver; see Section 3.21 on page 43

Table 4. **Other function pins**

Symbol	Pin	Description
IREF	5	IC reference current; see Section 3.5 on page 26
GND	15	IC ground reference; see Section 3.16 on page 39
VDD	16	IC supply, gate drive supply, restart after relamp; see Section 3.17 on page 39

3.1 SLHB pin: preheat current regulation, coil saturation protection

Refer to Figure 8. The resistors R13 and R14 in parallel (R13//R14 = R_{SLHB}) sense the half-bridge current. During preheat, the half-bridge controller with a preheat threshold $V_{th(ph)(SLHB)} = 0.5$ V regulates the half-bridge current. As a result, $V_{SLHB(peak)} = 500$ mV.

a. The SLHB pin circuit diagram.

b. Half-bridge current and voltage waveforms.

Fig 8. **The SLHB pin**

The saturation protection is always active and it protects the circuit against:

- coil saturation
- overvoltage of the resonant tank and the lamp

The IC has a fixed ratio of five between the preheat level and the saturation voltage level. The internal bias current source of 8.5 μA allows the current ratio (saturation/preheat) to be increased by adding resistor Rx in series with the SLHB pin.
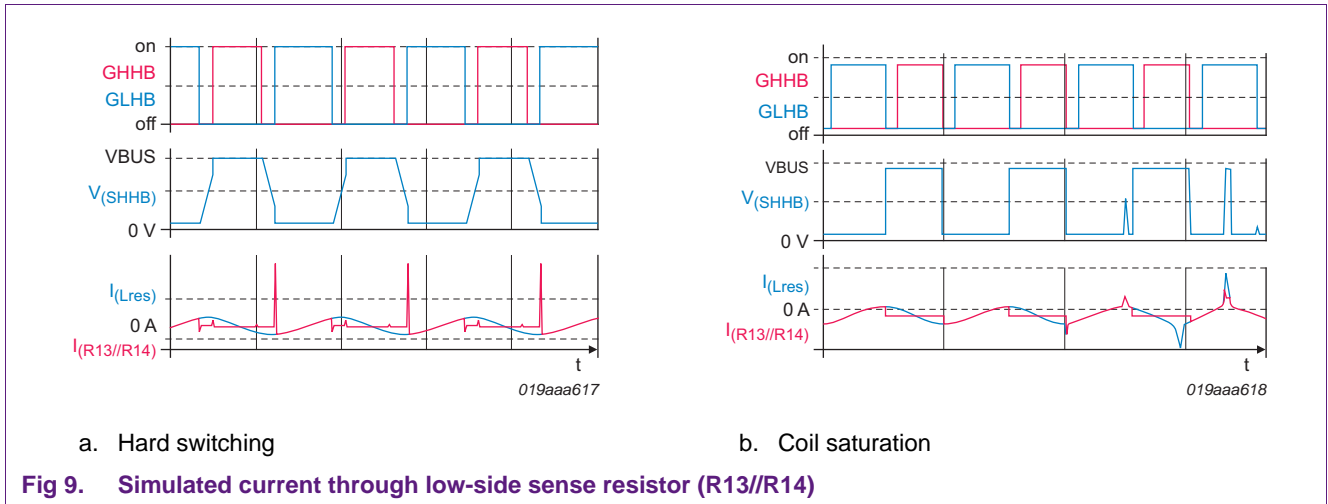
Equation 1 results the value for resistor Rx:

$$Rx = \frac{V_{th(ph)(SLHB)} \times I_{bias(SLHB)} + V_{th(ph)(SLHB)} \times I_{sat} - V_{th(sat)(SLHB)} \times I_{bias(SLHB)} - V_{th(sat)(SLHB)} \times I_{ph(peak)}}{I_{bias(SLHB)} \times (I_{sat} - I_{ph(peak)})} \tag{1}$$

$V_{th(ph)(SLHB)}$ = 0.5 V; $V_{th(sat)(SLHB)}$ = 2.5 V; $I_{bias(SLHB)}$ = 8.5 μA.

When Rx is known, Equation 2 calculates the R13 and R14 resistor values:

$$R(13//14) = \frac{V_{th(ph)(SLHB)} - I_{bias(SLHB)} \times Rx}{I_{bias(SLHB)} + I_{ph(peak)}} \tag{2}$$

a. Hard switching   b. Coil saturation

Fig 9. Simulated current through low-side sense resistor (R13//R14)

The hard switching spikes on the SLHB are internally blanked with 300 ns (leading edge blanking) to prevent a false trigger of the coil saturation.

During preheat and ignition, the saturation protection increases the HB operating frequency to reduce the HB inductor current. In preheat and ignition state the slow fault timer is used for saturation protection.

In burn state, the saturation protection reacts very fast to detect lamp removal or broken lamp conditions.

3.2 IFB pin: lamp current feedback, lamp-on detection, internal lamp current rectifier, overcurrent detection

Ballasts that run at the minimum operating frequency do not require a lamp current sense resistor and lamp-on detection. The IFB pin can be left open or shorted to ground. If no lamp-on is detected, the controller sweeps the frequency down. When the minimum switching frequency is reached, the IC assumes that the lamp has ignited. The IC has an internal double-sided rectifier on the IFB pin which has no voltage drop.

3.2.1 Lamp-on detection (LOD)

The LOD limits the visible flash when the ballast is switched on while the ballast control input is at a deep dim level.

After LOD (also known as ignition detection) is triggered, the IC enters Burn state. The IFB and VFB pins on the IC trigger the LOD. The voltage on the IFB pin must exceed $V_{th(lod)(IFB)}$ and the voltage on the VFB pin must be $< V_{th(lod)(VFB)}$. Both pin conditions must apply for a continuous period of $t_{d(lod)} = 3$ ms. The delay is implemented to ensure that sufficient ionization energy is transferred to the lamp. This implementation ensures the ignition of multi-lamp applications while limiting the flash at start-up.

IFB pin $V_{th(lod)(IFB)} > 0.35 \sim 1.0\ V^{(1)}$

VFB pin $V_{th(lod)(VFB)} < 1.0$ V

Delay $t_{d(lod)} = 3$ ms

State IGNITION BURN

time

aaa-002817

(1) See Figure 11.

Fig 10. Lamp-on detection delay time
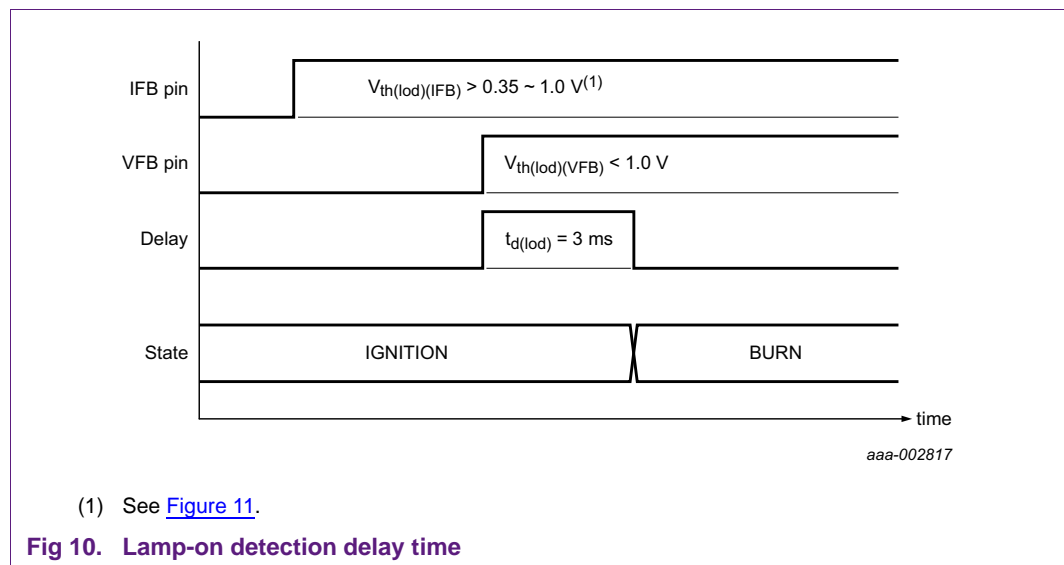
The threshold $V_{th(lod)(IFB)}$ is a function of the voltage on the DIM pin. The relationship between the LOD threshold and the DIM voltage is shown in Figure 11. The $V_{th(lod)(IFB)}$ signal is filtered using a time constant of approximately 100 μs. The threshold is therefore compared to the average double-sided rectified voltage on the IFB pin.
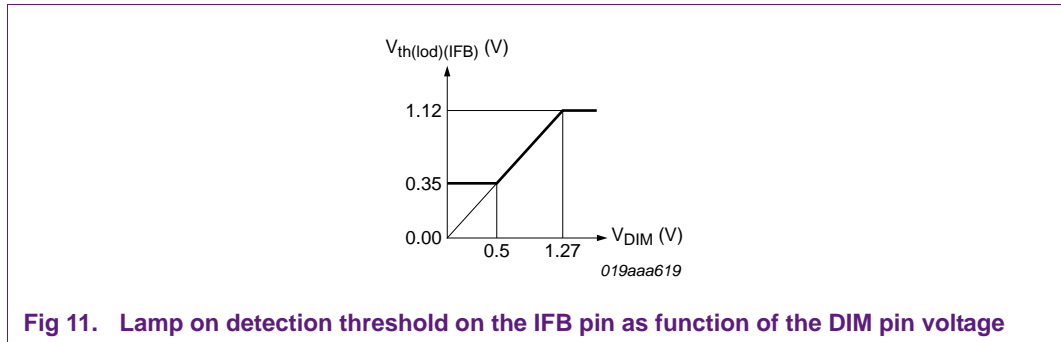
Fig 11. **Lamp on detection threshold on the IFB pin as function of the DIM pin voltage**

The voltage on the VFB pin must drop $< V_{th(lod)(VFB)} = 1$ V to trigger the LOD function.

Remark: If controller reaches the minimum operating frequency of ($V_{CIFB} = 3$ V) and the LOD condition is not met, the controller assumes that the lamps are ignited. In this case, the controller always enters the burn state.

3.2.2 Lamp current feedback

Ballasts that require only lamp current control without deep dimming, a single sense resistor is sufficient.

Applications that require deep dimming (below 10 %) are advised to use a non-linear sense circuit. The intention of the non-linear circuit is to guarantee a strong feedback signal for low lamp currents. Non-linear sensing has two advantages during deep dimming:

- The circuit is less sensitive to tolerances
- The circuit is less sensitive to low frequency ripples
- The minimum lamp current setting via input the DIM pin is more accurate

Place resistor R33 and C29 close to the IC (see Figure 12b).

3.2.3 Overcurrent lamp protection

The IC enters Stop state when both of the following conditions are met:

- The peak of the absolute voltage at the IFB pin exceeds $V_{th(ocd)(IFB)}$
- The IC is oscillating at f_{high}

AN10958

Application note **Rev. 2 — 9 August 2012** **14 of 56**

a. Normal application with basic IC

b. Deep dimming

R18, R19, D10 not mounted.

Fig 12. Lamp current sense circuit and the IFB pin
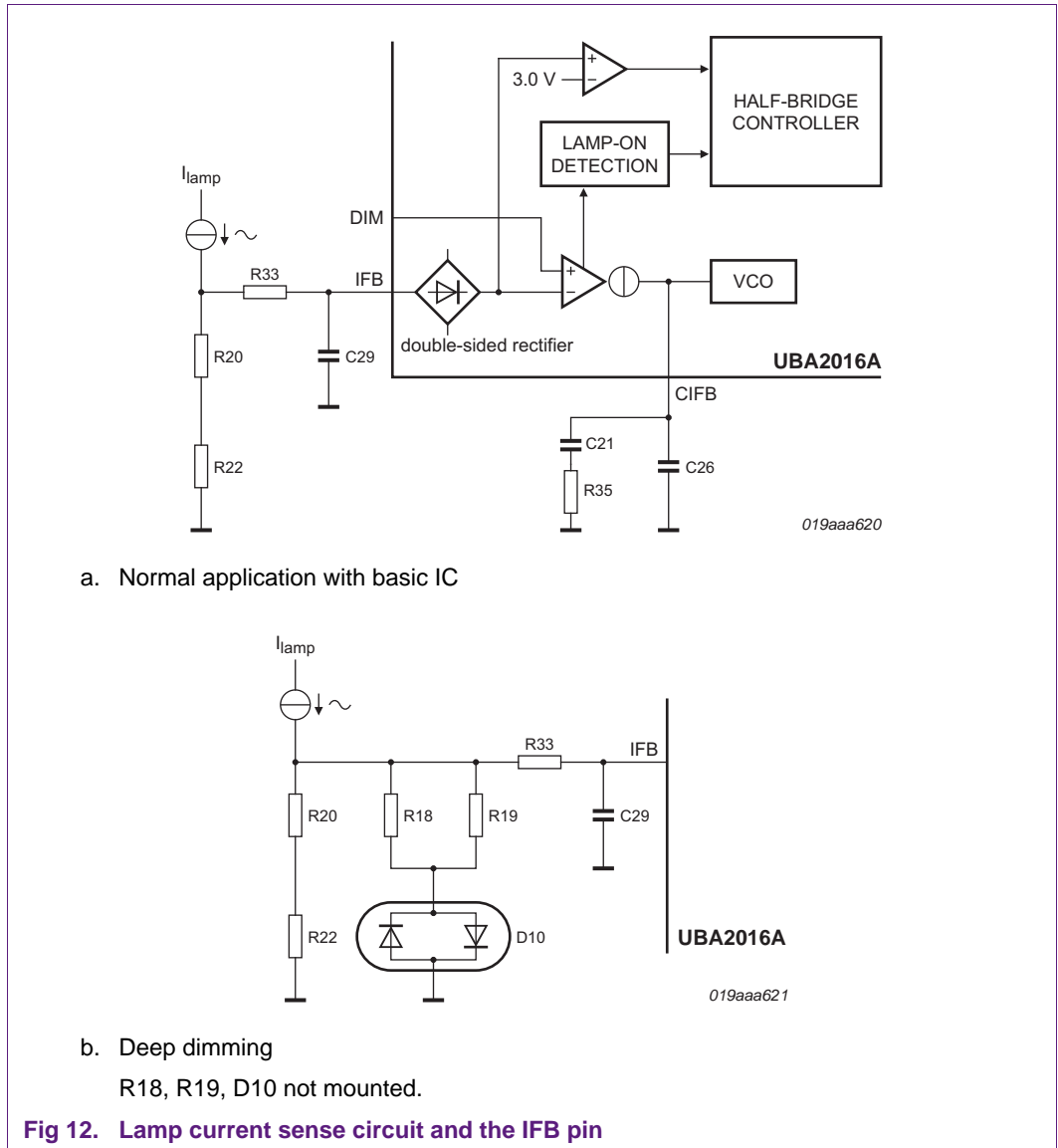
Typical values for lamps with nominal current of 300 mA:

Figure 12a: R20 = R22 = 2.4 Ω; R33 = 1.0 kΩ; C29 = 100 pF; R18 = R19 = reserved; D10 = reserved.

Figure 12b: R20 = R22 = 18 Ω; R18 = R19 = 2.7 Ω; R33 = 1.0 kΩ; C29 = 100 pF; D10 = PMBD7000.

3.2.3.1 Calculations for Figure 12a

$$I_{lamp(nom)(peak)} = I_{lamp(nom)} \times SQRT(2) = 424\ mA \tag{3}$$

After double-sided rectifying, Equation 4 gives the average lamp current.

$$I_{lamp(nom)(avg)} = I_{lamp(nom)(peak)} \times (2/\pi) = 270\ mA \tag{4}$$

AN10958

Application note **Rev. 2 — 9 August 2012** **15 of 56**

The internal regulation voltage $V_{reg(IFB)}$ = 1.27 V when application does not pull-down the DIM voltage.

Equation 5 calculates the value for R20 plus R22.

$$R20 + R22 \; = \; \frac{V_{reg(IFB)}}{I_{lamp(nom)(avg)}} \; = \; 4.7\,\Omega \tag{5}$$

Therefore R20 = R22 = 2.35 Ω.

3.2.3.2 Calculations for Figure 12b

Equation 6 calculates the parallel resistance value for R18 and R19.

$$R(\text{R18//R19}) \; = \; \frac{V_{reg(IFB)} - V_{f(avg)}}{I_{lamp(nom)(avg)}} \; = \; 1.37\,\Omega \tag{6}$$

The average forward voltage of the diode increases as a function of the current through the diode, the $V_{f(avg)}$ = $V_f \times$ 1.5 (based on measurements).

The dimming target of the RMS lamp current is 2 % of nominal. $I_{lamp(dim)(rms)}$ = 6 mA.

Equation 7 calculates the average lamp dimming current.

$$I_{lamp(dim)(avg)} \; = \; I_{lamp(dim)(rms)} \times SQRT(2) \times \frac{2}{\pi} \; = \; 5.4\,mA \tag{7}$$

The IFB pin voltage level in deep dimming must be 150 mV or higher. The reason for this requirement is the accuracy of the internal double-sided rectifier.

Equation 8 calculates the series resistance value of R20 plus R21.

$$R(20 + 22) \; = \; \frac{V_{reg(IFB)(dim)}}{I_{lamp(dim)(avg)}} \; = \; 28\,\Omega \tag{8}$$

Where $V_{reg(IFB)(dim)}$ = 150 mV, therefore R20 = R22 = 14 Ω.

3.2.3.3 Lamp at end-of-life and deep dimming sense circuit

The IC tries to ignite the broken lamp, until the fault timer expires, while the voltage on VFB regulates the operating frequency. Current flows through the lamp current-sense circuit due to the parasitic capacitances inside the half-bridge transformer because of the high voltage across the resonant circuit.

Take care to ensure that the lamp-on detection is not triggered. Therefore the R20 and R22 values in Figure 12b (deep dimming) must not be too high (see Figure 13).

a. Positions of stray capacitances in the half-bridge transformer

b. Simplified model showing the stray current

Fig 13. Stray capacitances of a half-bridge transformer for inductive topology
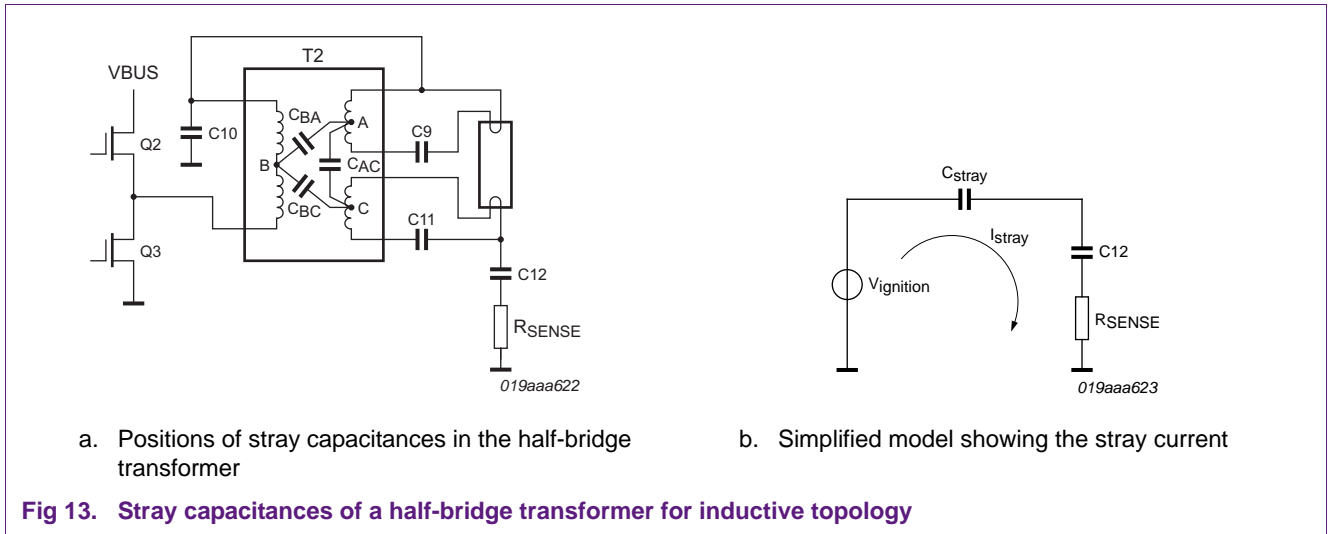
R_{sense} = R20 + R22.

The stray capacitance is the combination of all inter-winding capacitances (Equation 9).

$$C_{stray} = C_{BC} \equiv (C_{BA} + C_{AC}) \tag{9}$$

C12 is much larger than C_{stray}, therefore C12 can be ignored. Equation 10 calculates the stray current.

$$I_{stray} = V_{ignition} \times (2 \times \pi \times f_{ignition} \times C_{stray}) \tag{10}$$

Equation 11 calculates the average stray current.

$$I_{stray(avg)} = 4 \times V_{ignition(peak)} \times f_{ignition} \times C_{stray} \tag{11}$$

A design requirement is applied to prevent false LOD triggering in deep dimming non-linear current sense circuits as shown in Equation 12.

$$I_{stray(avg)} \times R_{sense} < 150\, mV \tag{12}$$

which is equal to Equation 13.

$$4 \times V_{ignition(peak)} \times f_{ignition} \times C_{stray} \times R_{sense} < 150\, mV \tag{13}$$

Some realistic values are:

$V_{ignition(peak)}$ = 1.2 kV; $f_{ignition}$ = 60 kHz; C_{stray} = 15 pF → R_{sense} < 35 Ω.

3.2.3.4 Multiple lamp current sense

The lamp current sense circuit for multiple lamps is very similar to the single lamp application; see Figure 14.

AN10958

Application note **Rev. 2 — 9 August 2012** **17 of 56**

a. Lamps in series   b. Lamps in parallel

Fig 14. Lamp current sense for multiple lamps
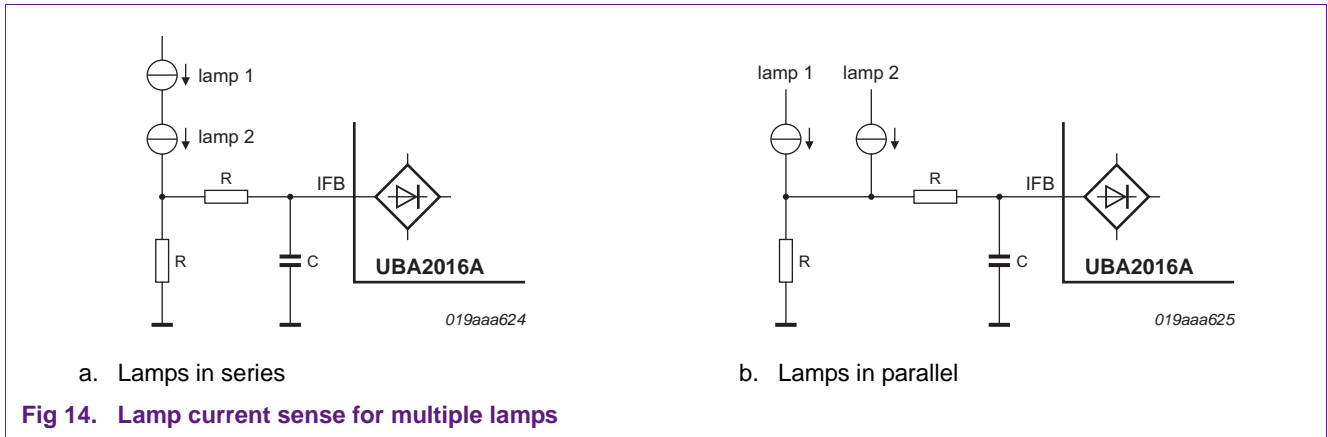
3.3 e EOL: lamp end-of-life detection

The voltage on the EOL pin is fed to the internal window comparator. The window lower limit equals the FBPFC voltage and the upper limit is equal to twice the FBPFC voltage.

Asymmetric aging effects of the lamp (IEC rectifying and asymmetric pulse) can be sensed by sensing the voltage on DC blocking capacitor C12. The sensitivity and DC shift can be adjusted independently due to the internal current source $I_{bias(EOL)}$ (see Figure 15).

a. Lamp end-of-life IEC test circuit (the diode can be connected in either polarity)

b. Relationship between DC blocking capacitor voltage and asymmetric power consumption

Fig 15. Asymmetrical lamp end-of-life IEC test circuit and DC blocking voltage
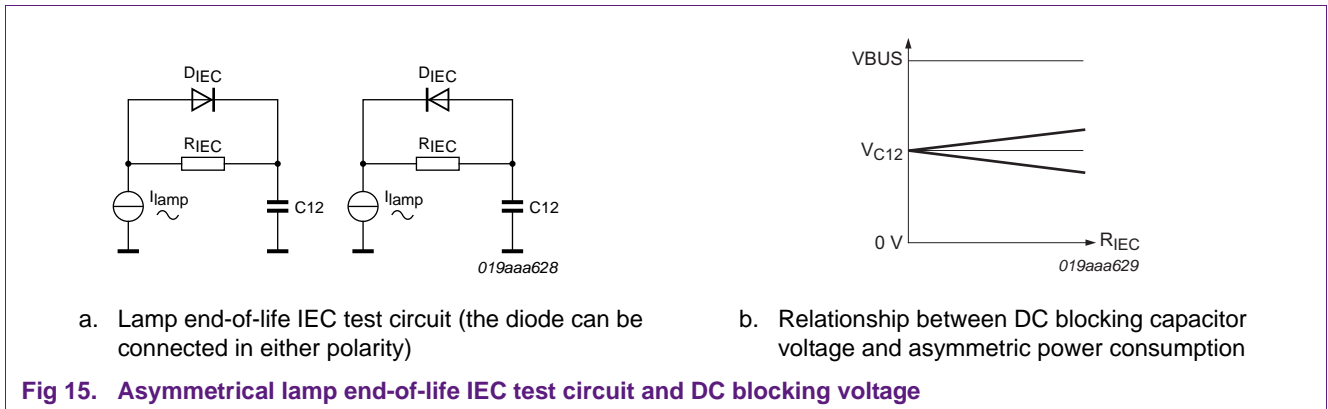
The power dissipated in the test resistor R_{IEC} must be below the IEC requirement of $P_{EOL(max)}$ = 7.5 W for T5 and $P_{EOL(max)}$ = 5.0 W for T4 lamps. Practical measurement determines R_{IEC}: R_{IEC} is increased until the maximum power is reached.

Equation 14 calculates the voltage on C12.

$$V_{C12} = \frac{VBUS}{2} \pm \frac{P_{eol}}{I_{lamp}}$$

(14)

The voltage on C12 shifts as a function of the power dissipated in R_{IEC}.

The maximum EOL power $P_{EOL(max)}$ is an IEC requirement. $P_{EOL(max)}$ for T5 is 7.5 W and for T4 it is 5 W. Currently there are no IEC requirements for T8 lamps. The voltage shift of the DC blocking capacitor due to asymmetrical aging can fit into the IC end-of-life window by the application resistor divider. The resistor divider consists of R_{EOL1} (R6 and R7 in Figure 3 on page 6) and R_{EOL2}.

a. Fixed output and dimming down to 10 %

b. Deep dimming <10 %

Fig 16. The EOL pin application with DC blocking capacitor C12 sensing
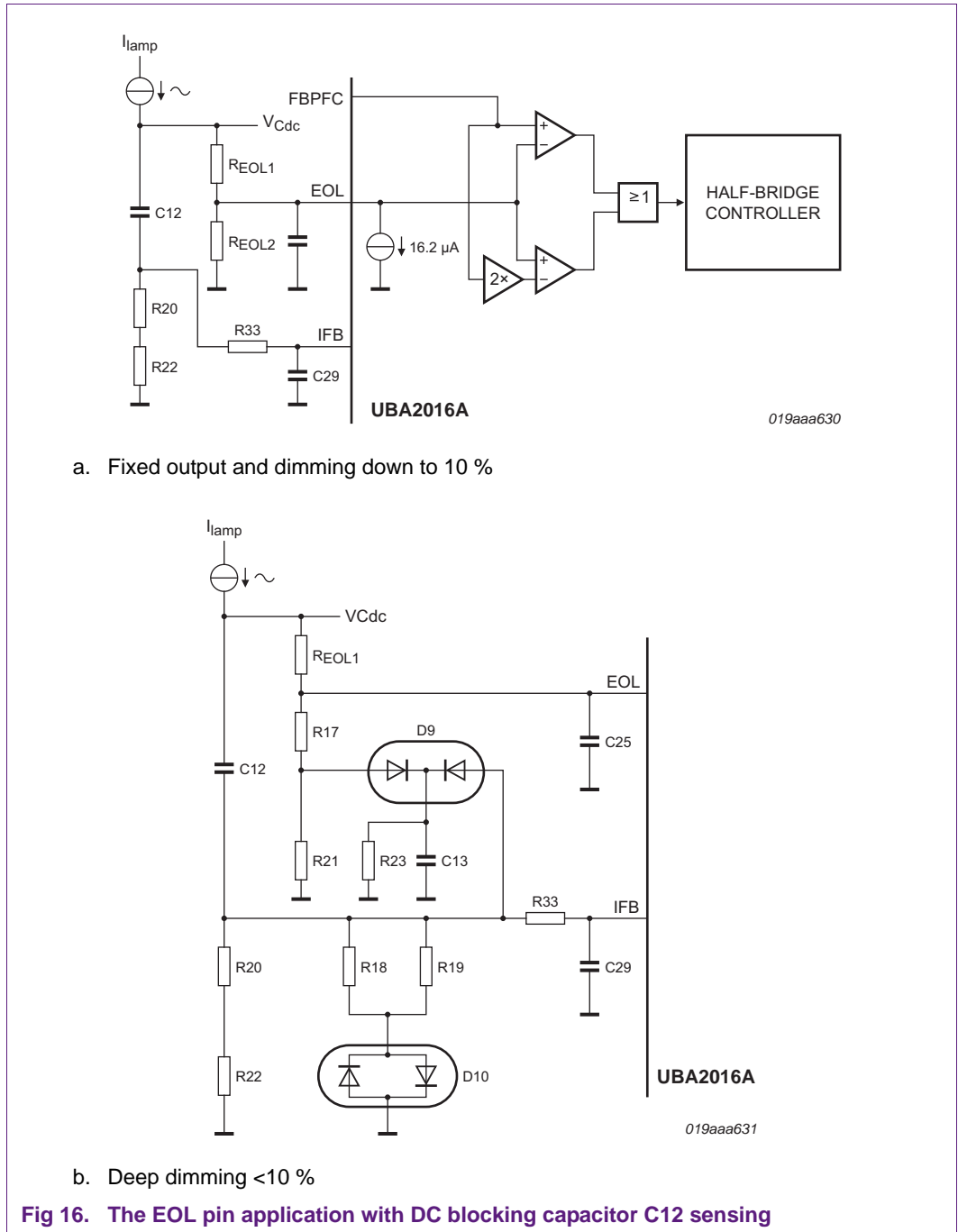
In deep dimming application, the voltage on the DC blocking capacitor shifts if a DC current through the lamp is used for canceling striation. A compensation circuit (D9, R23, C13, R21) shown in Figure 16b can be used when V_{C12} rises when dimming is below 10 % of the nominal lamp current.

AN10958

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Application note **Rev. 2 — 9 August 2012** **19 of 56**

3.3.1 Calculation of the resistor divider R_{EOL1} and R_{EOL2}

See Figure 16a.

The voltage at the EOL pin is shown in Equation 15.

$$V_{EOL} = \frac{V_{C12} \times R_{EOL2} - I_{bias(EOL)} \times R_{EOL1} \times R_{EOL2}}{R_{EOL1} + R_{EOL2}} \tag{15}$$

Where $I_{bias(EOL)}$ = 16.2 μA.

The EOL window threshold voltages are: $V_{th(low)(EOL)}$ = 1 × V_{FBPFC}, $V_{th(high)(EOL)}$ = 2 × V_{FBPFC}. Under normal operation, the V_{FBPFC} voltage is 1.27 V as shown in Equation 16.

$$V_{EOL(window)(range)} = (V_{th(high)(EOL)} - V_{th(low)(EOL)}) = V_{FBPFC} = 1.27\,V \tag{16}$$

Equation 17 calculates the EOL window center voltage.

$$V_{EOL(window)(center)} = \frac{V_{th(high)(EOL)} + V_{th(low)(EOL)}}{2} = 1.91\,V \tag{17}$$

Equation 18 calculates the required ratio between R_{EOL1} and R_{EOL2}.

$$\frac{R_{EOL1}}{R_{EOL2}} = \frac{2 \times P_{EOL} - V_{EOL(window)(range)} \times I_{lamp}}{V_{EOL(window)(range)} \times I_{lamp}} \tag{18}$$

Where P_{EOL} is the maximum power dissipated asymmetrically.

The absolute values for R_{EOL1} and R_{EOL2} center the voltage in the EOL window, calculated with Equation 19 and Equation 20.

$$R_{EOL1} = \frac{V_{EOL(window)(range)} \times I_{lamp} \times VBUS}{\dfrac{2 - 2 \times V_{EOL(window)(center)}}{V_{EOL(window)(range)} \times I_{lamp} \times I_{bias(EOL)}}} \tag{19}$$

$$R_{EOL2} = \frac{V_{EOL(window)(range)} \times I_{lamp} \times VBUS}{\dfrac{2 - 2 \times V_{EOL(window)(center)}}{V_{EOL(window)(range)} \times I_{lamp} - 2 \times P_{EOL} \times I_{bias(EOL)}}} \tag{20}$$

Table 5.   Calculated values for R_{EOL1} and R_{EOL2} for the EOL pin application

Lamp	VBUS (V)	P_{EOL} (W)	I_{lamp} (mA)	R_{EOL1} (MΩ)	R_{EOL2} (kΩ)
T5HE14W; T5HE21W; T5HE28W; T5HE35W	432	7.5	170	7.99	176
T5HO24W			300	10.4	411
T5HO39W			340	10.7	485
T5HO49W			260	9.90	338
T5HO54W			460	11.5	711
T5HO80W			555	11.8	896

AN10958

Application note **Rev. 2 — 9 August 2012** **20 of 56**

Use 1 % resistors such as the MRS type from Vishay BC Components for the EOL divider. The PFC output voltage must have 1 % accuracy because the voltage on the DC blocking capacitor is 0.5 times the bus voltage.

3.4 VFB pin: lamp voltage feedback, overvoltage detection, open/short protection

The advantage of lamp voltage feedback is that it limits voltage stress on the half-bridge components such as NMOST, inductor and capacitors. The lamp voltage feedback signal can be derived from the LC tank voltage. The dedicated voltage feedback pin is advantageous in multilamp applications because the IC regulates on the maximum voltage of both lamps.

When a lamp is removed or breaks in burn state, an immediate shutdown is activated when the shutdown threshold $V_{th(ovextra)(VFB)}$ = 3.35 V is reached. As a result, the excessive voltage is only briefly on the half-bridge resonant node.

3.4.1 Lamp voltage regulation

In preheat state and ignition state, when the VFB voltage is > $V_{th(ov)(VFB)}$ = 2.5 V, the switching frequency is increased (lowering the voltage on the resonant tank) and the fault timer starts. This feature protects the ballast under no lamp conditions. The IC tries again to ignite the lamp. If after the second time the lamp still does not ignite, the IC enters the standby state.

3.4.2 Overvoltage protection

In any state, when the VFB voltage is > $V_{th(ovextra)(VFB)}$ = 3.35 V, the controller enters Stop state immediately. This mechanism prevents excessive component stress when the lamp is removed while the actual switching frequency is below the unloaded resonant frequency.

3.4.3 EOL protection symmetrical lamp aging

Fluorescent lamps age over time and as a result the lamp voltage can increase. The VFB voltage is compared with threshold $V_{th(oveol)(VFB)}$. When the threshold is exceeded, the slow fault timer is started. When designing the VFB circuit, remain below the minimum $V_{th(oveol)(VFB)}$ value to ensure that the protection is not triggered.

A dimmed lamp has a higher lamp voltage than nominal. However, the higher lamp voltage caused by dimming must not trigger the symmetrical EOL protection. Therefore, the threshold for symmetrical EOL detection increases when the DIM pin voltage is lowered. The relation between $V_{th(oveol)(VFB)}$ and V_{DIM} is shown in Figure 17.

When V_{DIM} < 250 mV the symmetrical EOL protection is disabled.

(1) Maximum value.

(2) Typical value.

(3) Minimum value.

Fig 17. $V_{th(oveol)(VFB)}$ as a function of V_{DIM}
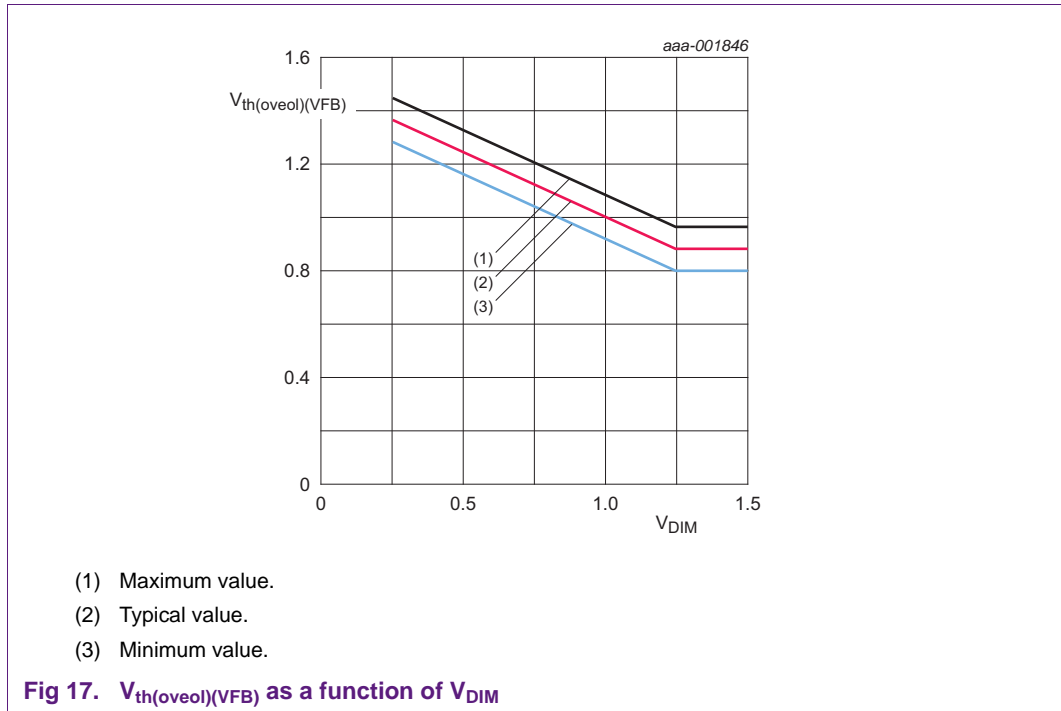
3.4.4 Open/short-circuit protection

When the VFB voltage is < $V_{th(osp)(VFB)}$ = 80 mV, the switching frequency is increased and the fault timer is started. $I_{bias(VFB)}$ pulls down the VFB pin when the pin is open.

3.4.5 Circuit diagrams for one and two LC tanks

3.4.5.1 Series resonant VFB circuit

Refer to Figure 18. HV capacitor C7 senses the lamp voltage on the resonant node of the LC tank. The current through the HV capacitor C7 is fed through the capacitor C8 and the voltage is divided. The diode clamps the voltage to −600 mV. A 2nd divider made up with resistors R10 and R11 divide the voltage to the appropriate level at the VFB pin. The capacitor C31 at the VFB pin lowers the ripple on the VFB voltage.

Do not make C31 too large or else the response time on overvoltage ($V_{th(ovextra)(VFB)}$ = 3.35 V) is slow. R_{bias} is used to lift the VFB voltage slightly > $V_{th(OSP)(VFB)}$ to enable start-up.

Typical values for a the VFB pin application are:

R10 = 100 kΩ, R11 = 5.6 kΩ, C7 = 100 pF, C8 = 1.5 nF, C31 = 10 nF and D8 = BAS101S.

AN10958

Application note **Rev. 2 — 9 August 2012** **22 of 56**
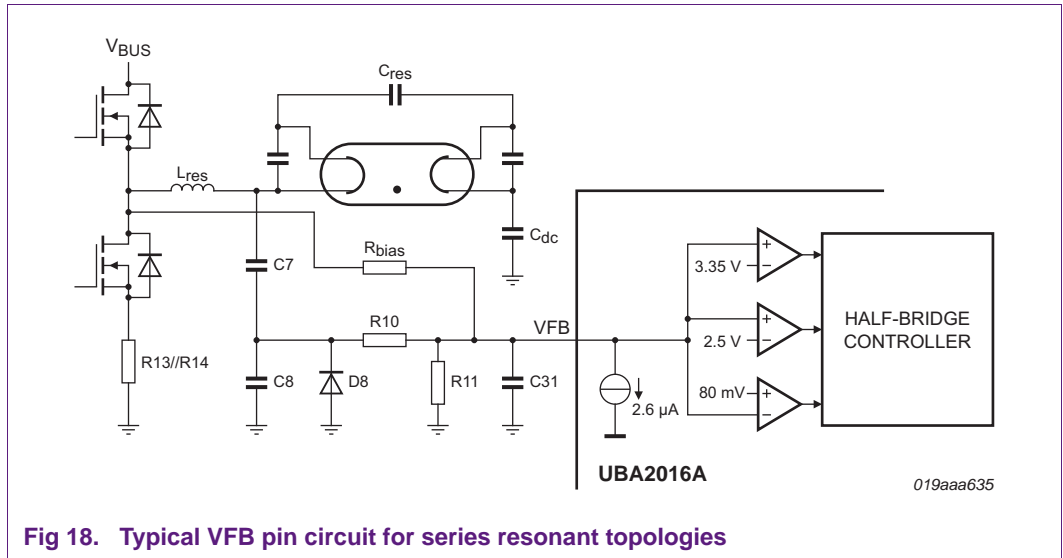
Fig 18. Typical VFB pin circuit for series resonant topologies

3.4.5.2 Inductive heating VFB circuit

In indicative heating topologies, the VFB circuit (with two LC tanks) shown in Figure 19 can be used. The resonance capacitors sense the lamp voltage and no additional HV capacitor is needed. The capacitor C2 in Figure 19 divides the lamp voltage to a lower level. R2 and R3 divided it to a lower level and provide an RC filter with capacitor C3.
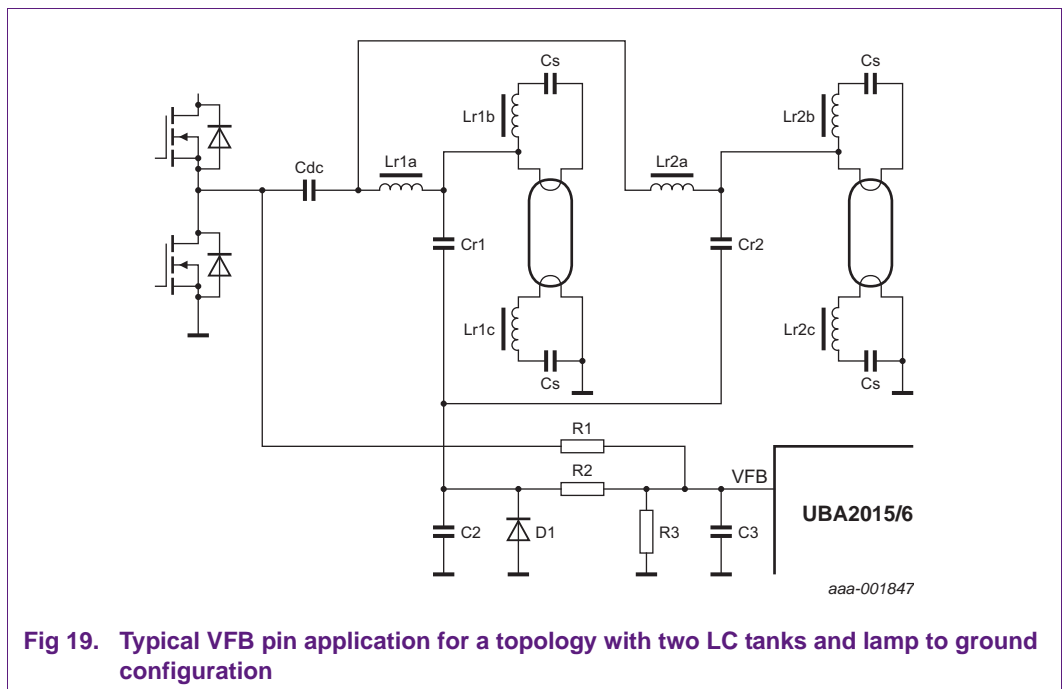
Fig 19. Typical VFB pin application for a topology with two LC tanks and lamp to ground configuration

Functionality of the VFB circuit components:

- R1: offset for open/short protection
- Cr1/Cr2: resonance capacitors
- C2: capacitive divider capacitor
- D1: diode clamp to ground
- R2/R3: resistor divider and discharge time of capacitor C2
- C3: Filter capacitor

3.4.5.3 Constraints of the VFB circuit

Start-up (and all other states): The voltage must be higher than 120 mV to satisfy the open/short protection. Set the voltage using resistor R1.

Ignition: The maximum voltage on the resonant tank (lamp voltage) is regulated to 2.5 V on the VFB pin.

Normal operation: The voltage on the VFB must remain under 800 mV to satisfy the symmetrical EOL protection.

Table 6. VFB conditions

Operating state	VFB > 120 mV ($V_{th(osp)(VFB)max}$)	VFB = 2.5 V ($V_{th(ov)(VFB)typ}$)	VFB < 800 mV ($V_{th(oveol)(VFB)min}$)
start-up	yes	yes	-
preheat	yes	yes	-
ignition	yes	yes	-
nominal	yes	yes	yes

When a large value capacitor for C2 is chosen, it is possible to make a DC shift with the clamping diode. The DC shift can help to find better matching of the voltage levels during ignition and operation.

3.4.5.4 Dimming constraints

Make sure that the VFB voltage remains under the overvoltage EOL threshold $V_{th(oveol)(VFB)}$ under all conditions. The $V_{th(oveol)(VFB)}$ depends on the DIM pin voltage level as shown in Section 3.4.3.

3.4.5.5 Circuit definition and verification

Starting point for the circuit design is that the divider capacitor C2 which must be at least 10x bigger than the Cr1 (+Cr2 if any). To minimize the costs of capacitor C2, keep the voltage < 100 V across the diode.

To verify the solution by simulation, the circuit shown in Figure 20 can be used.

AN10958

Application note Rev. 2 — 9 August 2012 **24 of 56**
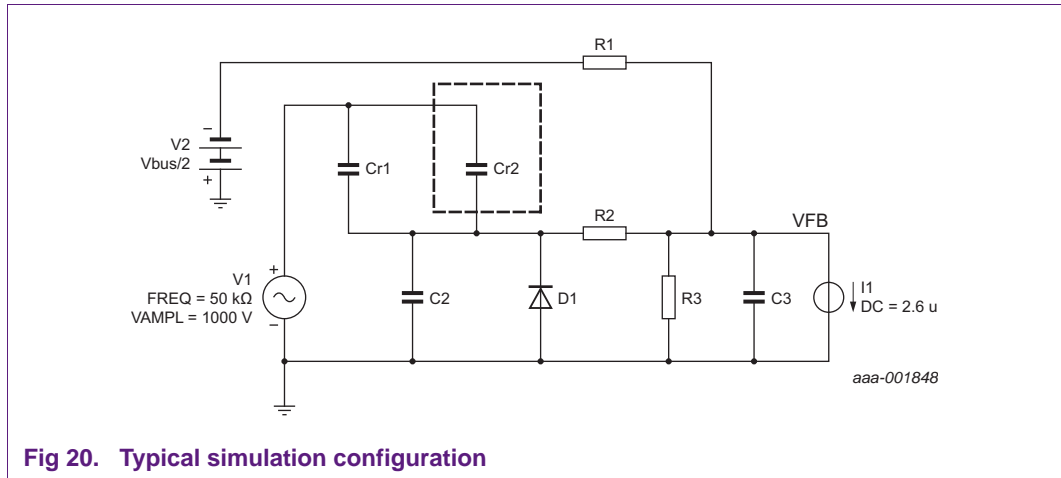
Fig 20. Typical simulation configuration

In Figure 20, V_{AMPL} is the LC tank voltage. Check the Ignition state and operating states. During dimming, the lamp voltage increases while dimming and whether the VFB voltage remains under the dynamic $V_{th(oveol)(VFB)}$ threshold.

Cr2 is the resonant capacitor of the 2nd resonant tank; it can be omitted when verifying one LC tank circuits.

3.4.5.6 Calculation of the VFB pin components

Equation 21 calculates the value of C8. The value of C7 is fixed C7 = 100 pF.

$$C8 = \left(C7 \times \frac{1 - V_R \times \dfrac{1 - margin}{2 \times V_{max} - VBUS}}{V_R \times (1 - margin)} \right) \times 2 \times V_{max} - VBUS \tag{21}$$

The time constant = C8 × (R10 + R11) determines the value of R10.

Where margin = 0.3 and is a constant. V_{max} is the worst case ignition voltage. V_R is the maximum reverse voltage of the clamp diode. A diode with a V_R of 300 V or higher requires sufficient voltage at start-up to satisfy $V_{th(osp)(VFB)}$. Equation 22 calculates the value of R11.

$$R11 = 2 \times R10 \times \frac{V_{reg}}{(2 \times V_{max} - VBUS) \times C7} \times \frac{C7 + C8}{1 - 2 \times \dfrac{V_{reg}}{(2 \times V_{max} - VBUS) \times C7} \times (C7 + C8)} \tag{22}$$

Capacitor C31 filters noise on the VFB PCB track. C31 must not be too high to enable the IC to react quickly on lamp removal when the switching frequency is near the resonant frequency of the LC tank. A time-constant of 100 ns is advised. The value of C31 is $C21 \times R11 = 100\ ns$.

3.5 IREF pin: IC reference current

A 33 kΩ resistor (R34) connects the IREF pin to ground reference.

3.6 CIFB pin: input for the internal VCO, time-constant of the lamp current control loop, ignition frequency ramp-down speed after preheat

3.6.1 VCO input

When the CIFB pin is 0 V, the half-bridge switching frequency is at f_{high}.

When CIFB is at $V_{high(CIFB)}$ = 3.0 V, the half-bridge switching frequency is at f_{low}.

3.6.2 Lamp current control

The average voltage on the IFB pin controls the half-bridge frequency. If the IFB pin is not used, the switching frequency in Burn state is f_{low}.

Since the CIFB pin is the output of the error amplifier, the capacitance on the CIFB pin determines the speed/frequency response of the control loop.
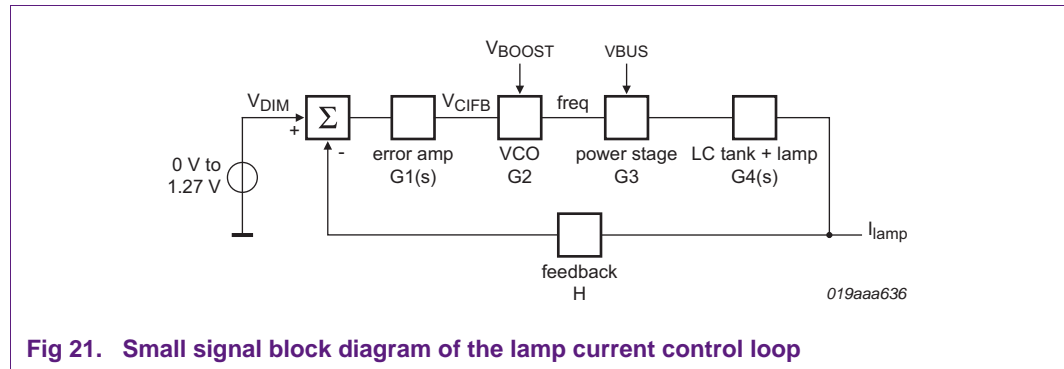
Fig 21. Small signal block diagram of the lamp current control loop

Figure 22a shows the transfer of the error amplifier with the CIFB compensation network. This transfer is equal to G1(s) in Figure 21.

AN10958

Application note **Rev. 2 — 9 August 2012** **26 of 56**

a. The CIFB pin application

b. Small signal transfer (gain versus frequency)

(1) C26, C21 and R35.

(2) C26 (C21 and R35 not mounted).

Fig 22. Frequency response of error amplifier plus CIFB network
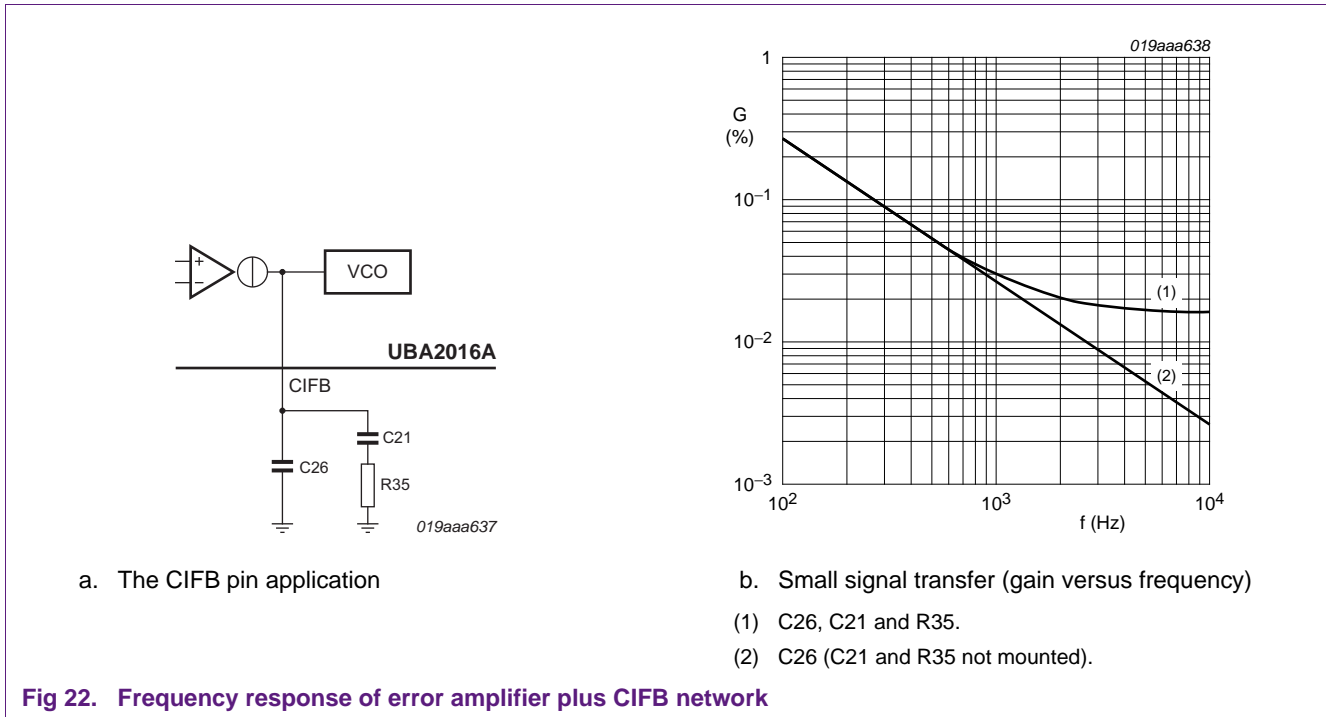
Typical values for the CIFB network are:

Non-dimmable ballasts: C26 = 100 nF; C21 = reserved; R35 = reserved;

Dimmable ballasts: C26 = 3.3 nF; C21 = 100 nF; R35 = 1 kΩ.

During deep dimming, the lamp discharge column is close to extinguishing and the time-constant of the lamp is small. The control loop has to be fast enough to prevent the lamp from extinguishing. Therefore, for a dimmable ballast, add C21 and R35 to increase the gain and speed of the control loop.

3.7 CF pin: timing capacitor of oscillator

The oscillator frequency is twice the operating frequency of the half-bridge. To guarantee a 50 % duty cycle, the half-bridge operates at half the oscillator frequency. Capacitor C27 sets the frequency range of the half-bridge controller in the internal relaxation oscillator. Equation 23 calculates the value of C27.

$$C27 = \frac{I_{cf}}{2 \times f_{low} \times V_{th(cf)}} \tag{23}$$

Where I_{cf} = 43 µA; $V_{th(cf)}$ = 2.5 V.

The maximum switching frequency (f_{high}) is a fixed ratio: $f_{high} = f_{low} \times 2.4$.

A typical value for C27 is 220 pF, results in an f_{low} of 39 kHz and hence an f_{high} of 94 kHz; see Figure 23.

If C27 is a ceramic capacitor, use an NP0 or C0G dielectric, for high accuracy and temperature independency. Without lamp current control, use an accurate capacitor to obtain an accurate switching frequency.
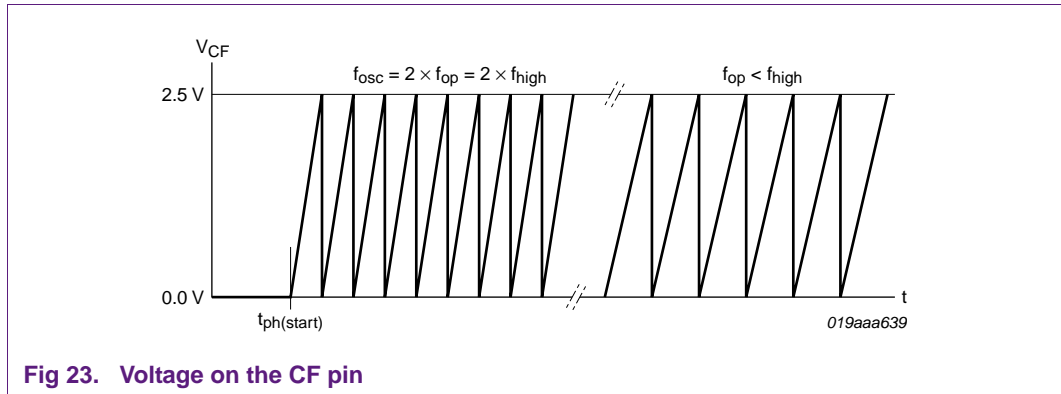
Fig 23. Voltage on the CF pin

A current source charges capacitor C27 until the threshold of 2.5 V is reached then C27 is discharged during 300 ns. The IC regulates the amount of charge current and therefore the switching frequency.

3.8 CPT pin: preheat timer, fault timer, open/short protection

The capacitor on the CPT pin sets the preheat and fault time duration. Equation 24 calculates the preheat time relation to CPT capacitor.

$$C30 = \frac{t_{ph}}{CPT_{constant}}$$

(24)

Where $CPT_{constant} = 10 \times 10^6$.

A typical value for C30 is 100 nF which gives a preheat time $t_{to(ph)}$ of 1 s.

When C30 is a ceramic capacitor, use an X7R dielectric. The X7R capacitance decreases when a DC voltage is applied, therefore the voltage rating must be 50 V even though a lower voltage is applied.

3.8.1 Preheat timer

The preheat timer counts 8 times to charge capacitor C30 to 3.7 V with a current of 2.7 μA. The discharge current of 11 μA is applied until the voltage on C30 reaches 1.0 V (see Figure 24). The charge and discharge currents are unequal in the preheat state. The preheat-time/fault time ratio can be programmed (between 3.35 and 10.1) using an external resistor as described in the data sheet (Ref. 1).
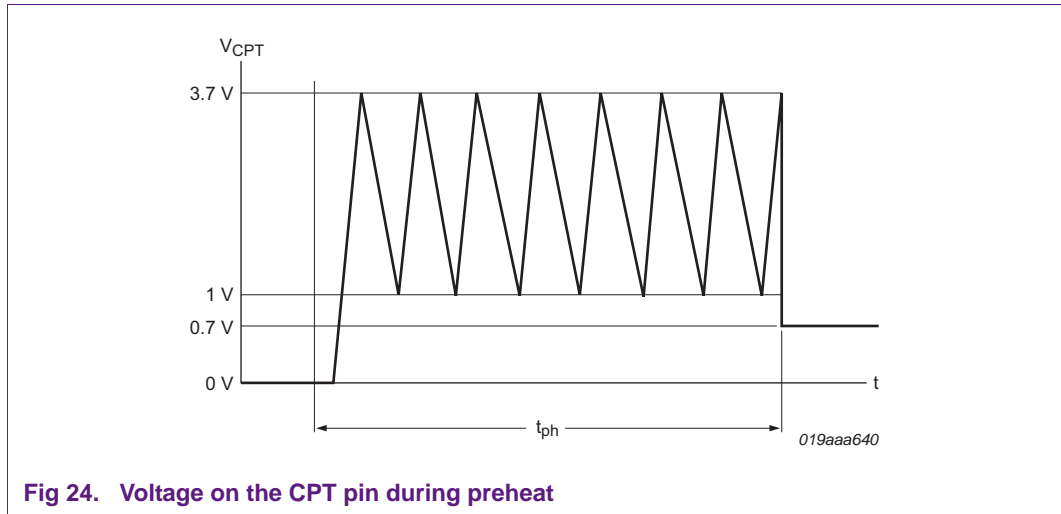
Fig 24. Voltage on the CPT pin during preheat

3.8.1.1 Fault timer

The fault timer provides a delay between fault detection and shutdown. The fault time duration is one fifth of the preheat time. The fault timer uses a charge and discharge time of 23.5 μA.

Since both timers use the same pin, the fault timer takes priority over the preheat timer. The preheat timer restarts after a fault has cleared.

3.8.1.2 Open/short protection

When the CPT pin is < $V_{th(scp)(CPT)}$ = 120 mV, the controller does not sweep the frequency down to the preheat frequency but continues switching at f_{high}. This protection prevents endless preheating if a short or open circuit production fault occurs on this pin.

When the CPT pin is < $V_{th(scp)(CPT)}$ while the IC is in any oscillating state, the controller increases the switching frequency to f_{high} with a time-constant of approximately 7 ms. The CIFB pin can be shorted to ground in case a shorter time-constant is needed.

The open/short protection on the CPT pin allows an (optional) external protection circuit to switch the operating frequency to f_{high}. At f_{high} the power in the LC tank is minimal and the voltage stress on the half-bridge components is minimal.

3.9 DIM pin: reduces lamp current control set point, reduces the lamp-on-detection threshold

3.9.1 Lamp current regulation

The controller regulates the frequency such that the average voltage on the IFB pin during Burn state equals the DC voltage on the DIM pin.

The lamp current regulation level is equal to the voltage at the DIM pin. Internally the maximum regulation level is clamped to $V_{reg(IFB)}$ = 1.27 V. During the start-up cycle (Preheat and Ignition state) the minimum regulation level is clamped to 500 mV. In Normal state, use a minimum level of 150 mV for better accuracy and also to prevent detection of false ignition (lamp-on detection) using the IFB pin.

AN10958

Application note **Rev. 2 — 9 August 2012** **29 of 56**

3.9.1.1 Lamp-on detection

The lamp-on detection limits the visible flash when the ballast is switched on while the ballast control input is at a deep dim level. Section 3.2.1 describes how the DIM voltage is used for the lamp-on detection.

3.9.1.2 Chapter 3.9.1.2 Symmetrical aging

Dimmable ballast only: the lamp voltage increases when the lamps are dimmed. The symmetrical aging threshold $V_{th(oveol)(VFB)}$ is increased as function of the DIM voltage to avoid triggering the symmetrical aging function. In the burn state, the VFB pin senses the symmetrical aging. Section 3.4.3 describes the relationship between the DIM voltage and the symmetrical aging threshold.
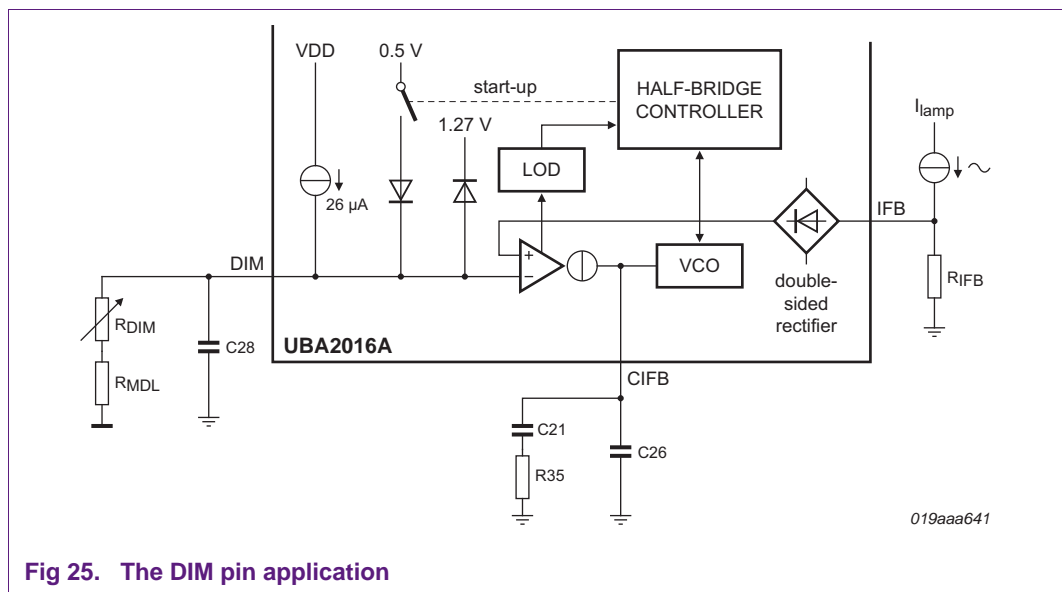
Fig 25. The DIM pin application

The DIM pin requires a capacitor C28 of 10 nF to ground. The internal current source $I_{bias(DIM)}$ charges C28 to the maximum voltage (see Figure 25).

If dimming is required, decreasing voltage on the DIM pin reduces the lamp current. A resistor or a voltage source that can sink at least 25 µA of current is sufficient.

R_{DIM} in Figure 25 is used to set the voltage, R_{MDL} is used to set an accurate minimum dim level.

3.10 BOOST pin: increase lamp current control set point

The UBA2016A has a boost function that is intended to shorten the run-up time of the lamp. Boosting is useful for amalgam lamps or outdoor applications (see Figure 26).

AN10958

Application note **Rev. 2 — 9 August 2012** **30 of 56**
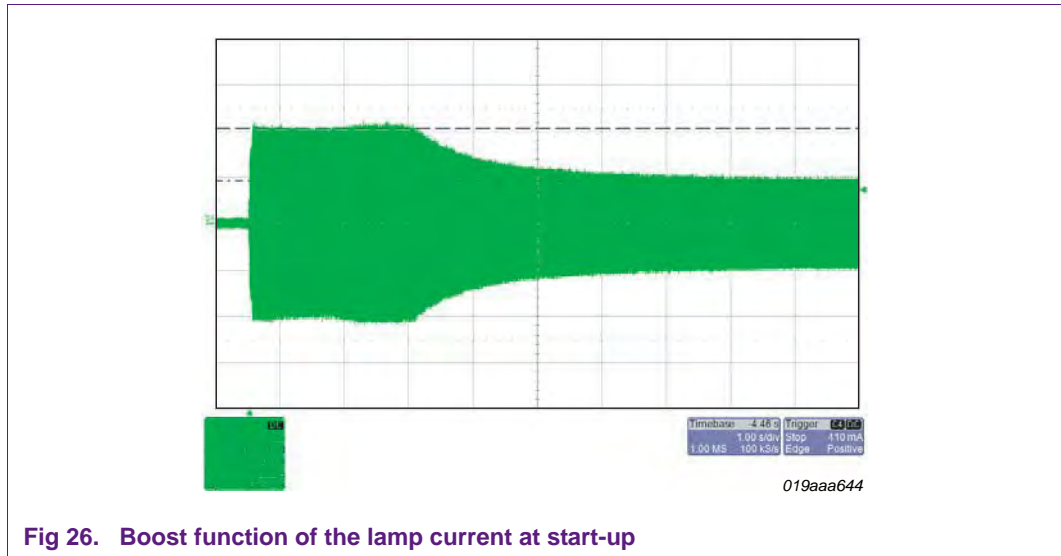
Fig 26. **Boost function of the lamp current at start-up**

The lamp current is increased as a function of the current that flows into the BOOST pin. Figure 27b shows the RMS lamp current versus the BOOST pin current; in this case a non-linear lamp current sense circuit Figure 12b is used.

During the boost time, the minimum operating frequency f_{low} is reduced to 50 %. The BOOST pin current increases the light output that is more than nominal. Control using the DIM pin does not reduce the minimum operating frequency.

When not needed, connect the BOOST pin to ground. Consider using the UBA2015 which has a fixed frequency preheat function instead of the boost function.

a. The BOOST pin components

b. The BOOST pin current as a function of lamp current

Fig 27. BOOST application
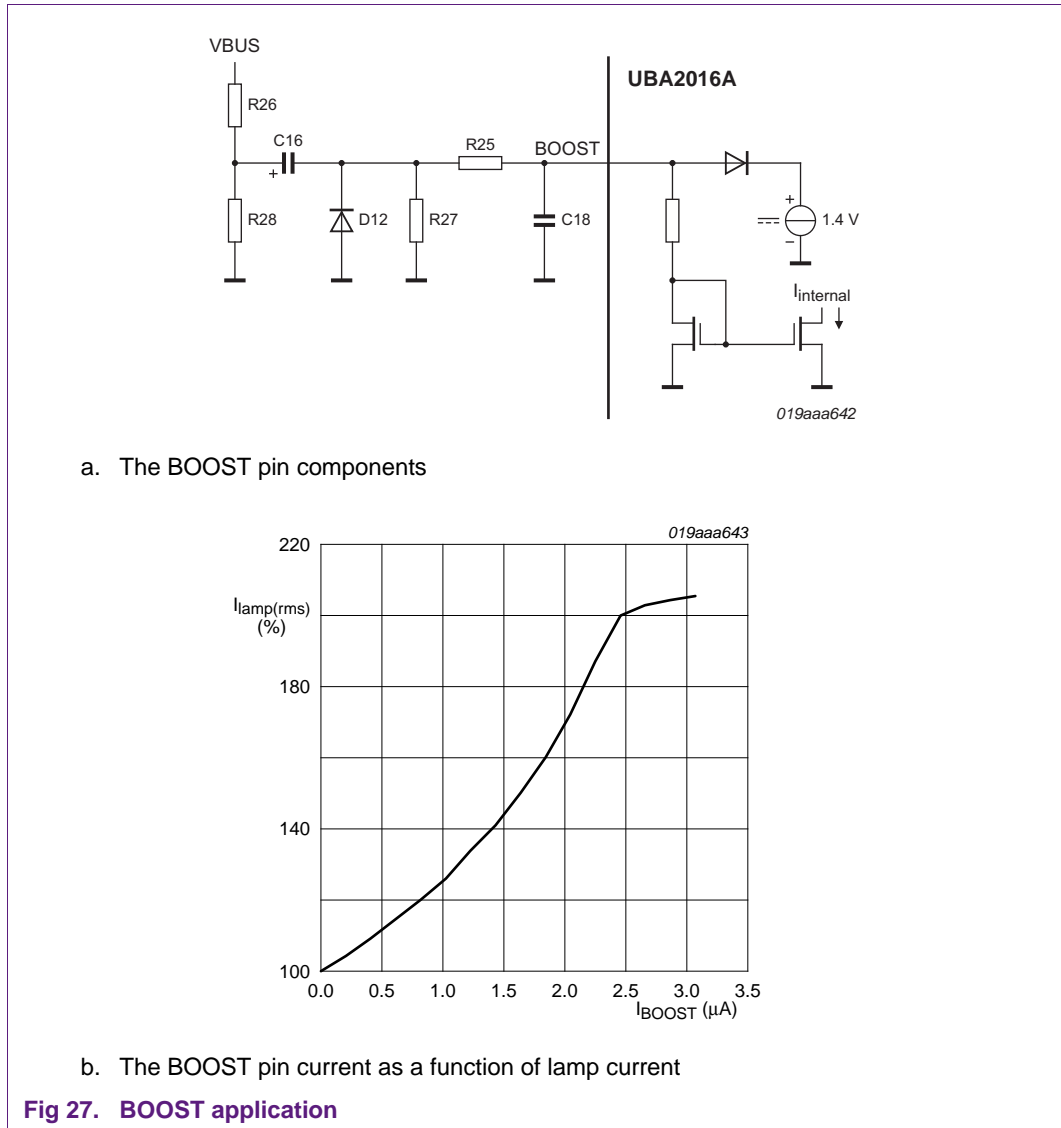
Refer to Figure 27a. Typical values for the boost network are:

R25 = 10 kΩ; R26 = 2.2 MΩ; R27 = 470 kΩ; R28 = 47 kΩ; C16 = 10 μF; C18 = 10 nF; D12 = PMBD914.

The boost time is equal to the discharge time of capacitor C16 minus the preheat time; R27 is in the circuit to discharge C16 completely. C18 makes the input less sensitive to noise.

The boost voltage must not exceed the limiting value of +2.5 V:

Calculate R26, R28.

The BOOST pin current must not exceed 100 μA when D12 is in forward mode:

Calculate R25: 10 kΩ is sufficient in most cases.

The half-bridge circuit must support the boost function. Therefore the following two rules apply:

$$V_{BUS} > 8 \times f_{bst} \times L_{res} \times SQRT(3) \tag{25}$$

$$f_{low(bst)} > \frac{1}{pi \times SQRT \times L_{res} \times Cdc} \tag{26}$$

The first rule (Equation 25) ensures that the lamp current can be reached. The second rule (Equation 26) ensures that the half-bridge switching node is not operated in capacitive mode.

3.11 PH/EN: fixed frequency preheat, enable/disable, burn state indication output

A resistor from the PH/EN pin to ground (UBA2015 sets the frequency during preheat. The preheat frequency is shown as a function of $R_{PH/EN}$ for CF = 180 pF, 200 pF and 220 pF.

(1) CF = 180 pF.
(2) CF = 200 pF.
(3) CF = 220 pF.

Fig 28. Preheat frequency as a function of R_PH/EN
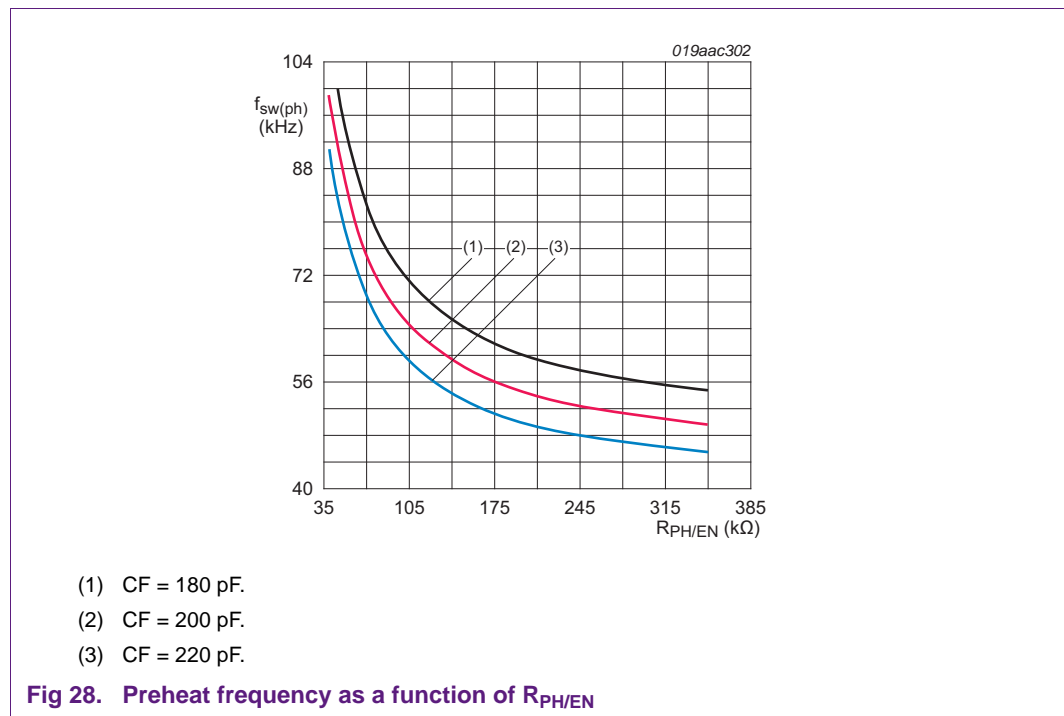
The controller can be disabled by pulling the PH/EN pin < 250 mV with a transistor. The sink current must be at least $I_{O(clamp)max(PH/EN)}$ = 160 μA. The enable/disable feature is useful for power management or additional protection that needs a fast shutdown.

AN10958

Application note **Rev. 2 — 9 August 2012** **33 of 56**
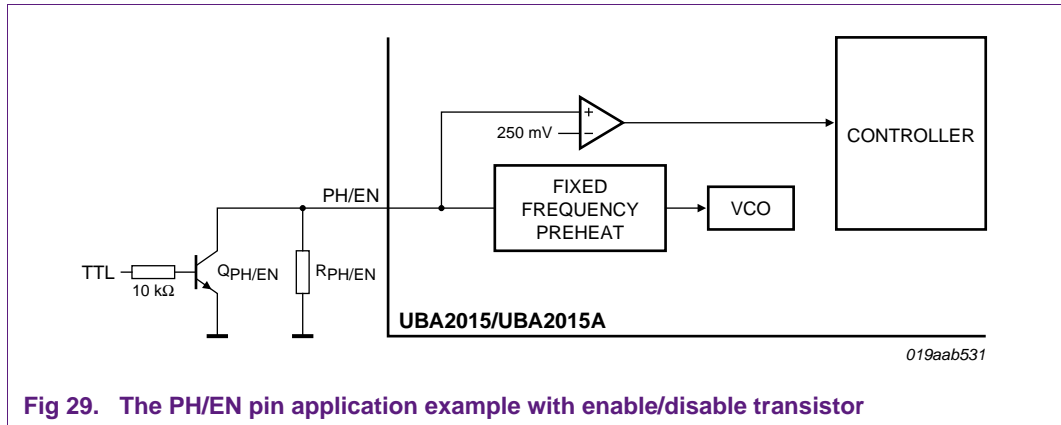
Fig 29. The PH/EN pin application example with enable/disable transistor

The PH/EN pin indicates when the burn state is entered. This function can be used to operate a switch in the half-bridge circuit to change the LC tank between preheat and burn state.

In preheat and ignition state the output voltage is 1.84 V. In burn state the output voltage is 1.27 V.

3.12 FBPFC pin: PFC voltage feedback, overvoltage protection, overcurrent protection, open/short-circuit protection

The brownout functionality is assigned to the COMPPFC pin (see Section 3.13).

3.12.1 PFC voltage feedback

The PFC controller is always active when the half-bridge is active. The half-bridge switching frequency is kept at $f_{high(HB)}$ until the voltage on the FBPFC pin is > $V_{th(VPFCok)(FBPFC)}$ = 1.0 V.

The voltage on the FBPFC pin connects to the error amplifier of the PFC control loop. The FBPFC pin is connected to the PFC output voltage VBUS and it is compared with an internal voltage of $V_{reg(FBPFC)}$ = 1.27 V.

3.12.1.1 Overvoltage protection

The FBPFC voltage is compared with an internal voltage of $V_{th(ov)(FBPFC)}$ = 1.39 V, internally, leading edge blanking is applied at the rise of GPFC. If V_{FBPFC} > 1.39 V then, GPFC is immediately set to LOW and kept LOW while V_{FBPFC} is > 1.39 V.

3.12.1.2 Overcurrent protection

The PFC current sense is connected to the FBPFC pin using a diode to prevent damage to the PFC NMOST when coil saturation/overcurrent occurs.

The negative temperature coefficient of the diode forward voltage (almost) compensates for the maximum flux density (B_{max}) of the PFC inductor. Typically a diode such as PMBD914 or 1N4148 is preferred. Do not use a Schottky diode because of its high leakage current properties.

3.12.1.3 Open/Short Protection (OSP)

When the FBPFC pin voltage is < $V_{th(osp)(FBPFC)}$ = 250 mV, the PFC gate drive is disabled.

The internal bias current sink of $I_{bias(FBPFC)}$ = 5 µA ensures that V_{FBPFC} is LOW when the pin is left open.
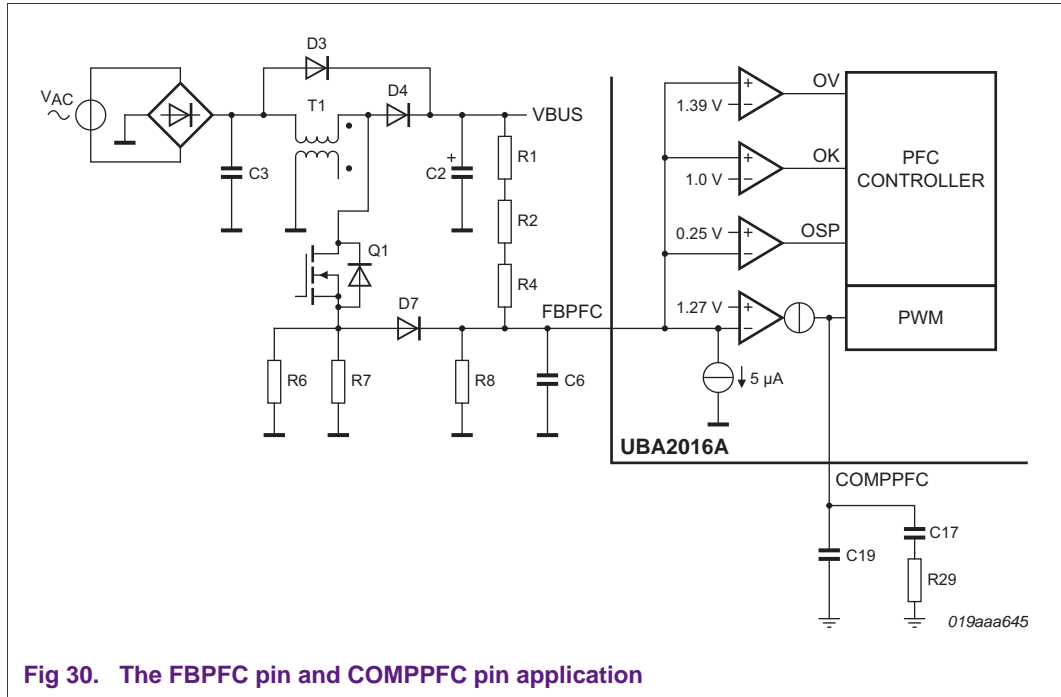
Fig 30. The FBPFC pin and COMPPFC pin application

Typical values for the pin applications: C6 = 47 pF; R8 = 3.3 kΩ.

There is a leading-edge blanking of $t_{leb(FBPFC)}$ = 330 ns on the FBPFC pin.
$t_{leb} = C6 \times R8 < 330\ ns$.

To prevent noise being injected into the feedback loop, ensure R8 ≤ 3.3 kΩ.

Calculate the sum of R1, R2, and R4 for the correct output voltage using Equation 27:

$$(R1 + R2 + R4) = R8 \times \frac{(V_{BUS} - V_{reg(FBPFC)})}{(V_{reg(FBPFC)} + I_{bias(FBPFC)} \times R8)}$$

(27)

Use the same type of 1 % resistors for R1, R2, R4 and R8 for an accurate bus voltage and accurate voltage on the DC blocking capacitor. The voltage of the DC blocking capacitor is used for lamp end-of-life detection.

Calculate the value of R6 and R7 in parallel for the correct PFC overcurrent protection using Equation 28.

$$R(6//7) = \frac{1.27 + 0.6}{I_{PFC(peak)} \times 1.1}$$

(28)

3.12.1.4 Layout rules

Place capacitor C6 close to transistor Q1 to keep the switching noise local to Q1.

AN10958

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Application note **Rev. 2 — 9 August 2012** **35 of 56**

3.13 COMPPFC pin: PFC voltage control loop compensation network, input of on-time modulator

A COMPPFC pin application is shown in <u>Figure 30</u>. The typical values are:

C19 = 100 nF; C17 = 470 nF; R29 = 82 kΩ.

3.13.1 Compensation network

The compensation network has a unity gain in the PFC control loop at 20 Hz. It is a trade-off between Power Factor and transient behavior. A lower bandwidth leads to a better Power Factor but the transient behavior is less. A higher bandwidth leads to a better transient behavior but the Power Factor is less.

The components C17 and R29 are added to have maximum phase margin at the unity gain frequency.

3.13.1.1 On-time modulator input

The voltage on the COMPPFC pin determines the on-time of the PFC gate drive signal. A low voltage results in a low on-time, a high voltage (equal to $V_{high(COMPPFC)}$ = 3.0 V) results in a maximum on-time of 28 µs.

3.13.1.2 Brownout undervoltage

If a brownout or undervoltage occurs, the COMPPFC voltage increases and therefore also the on-time. However, when the COMPPFC voltage reaches 3.0 V the on-time does not increase. Furthermore, a signal is sent to the lamp controller to reduce the lamp power by increasing the half-bridge switching frequency. Avoid the 3 V limit during the preheat and ignition states because the controller increases the half-bridge switching frequency.

3.14 AUXPFC pin: demagnetization detection, THD waveshaper, open pin protection
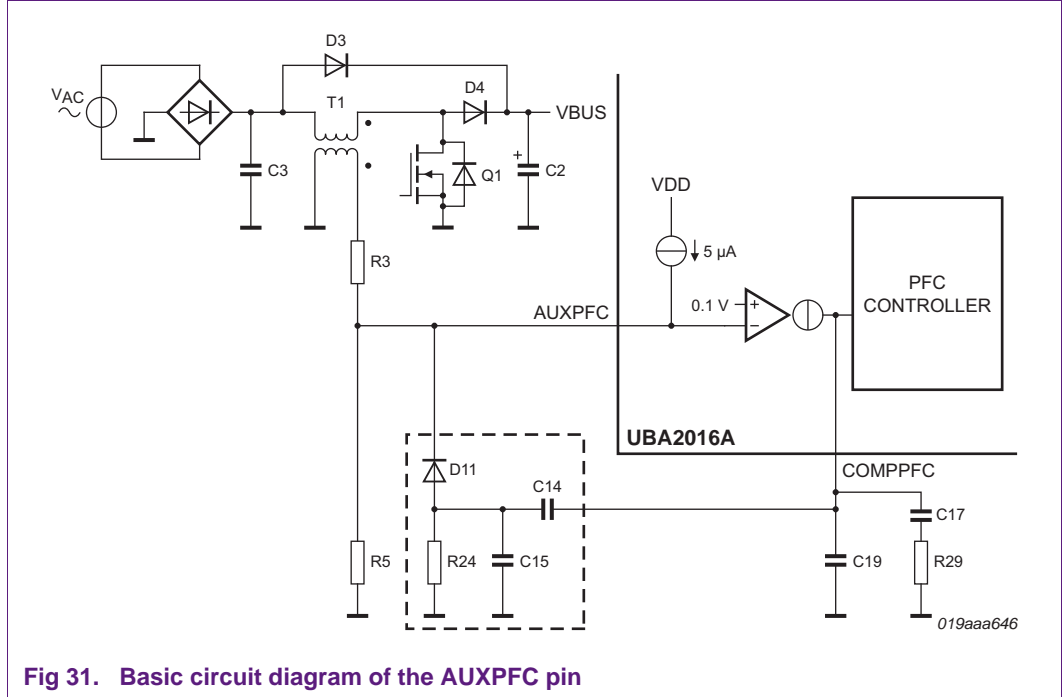
Fig 31. Basic circuit diagram of the AUXPFC pin

Typical values of the application shown in Figure 31:

R3 = 10 kΩ; R5 = reserved; R24 = 10 kΩ; D11 = PMBD914; C15 = 100 nF; C14 = 4.7 nF.

3.14.1 PFC auxiliary winding

Add a 10 kΩ series resistor (R3) to AUXPFC to protect the IC against a too high voltage, for example during lightning surge events.

The number of turns of the auxiliary winding on the PFC coil and the maximum voltage across the PFC inductor can be calculated.

The PFC output voltage at overvoltage protection VBUS$_{(ov)}$ determines the maximum voltage across the PFC primary winding as shown in Equation 29.

$$VBUS_{(ov)} = \frac{VBUS \times V_{th(ov)(FBPFC)}}{V_{th(reg)(FBPFC)}} = VBUS \times 1.1 \tag{29}$$

It is important to maintain demagnetization detection even at low ringing amplitudes. The voltage at the AUXPFC pin to 8.1 V (absolute maximum rating minus 10 %).

$$Np = \frac{Ns \times VBUS_{(ov)}}{V_{AUXPFC(max)} \times 0.9} = \frac{Ns \times VBUS_{(ov)}}{0.81} \tag{30}$$

A resistor divider is placed when the number of auxiliary turns are too high.

3.14.1.1 THD wave shaper circuit

To reach a THD performance better than 25 % THD, the on-time of the PFC is modulated. With the waveshaper circuit, a THD < 8 % can be reached over a large input voltage range. The modulation increases the on-time when the absolute mains voltage decreases. The AUXPFC signal can be used as a signal source. After peak rectifying and filtering, the signal is injected into the COMPPFC pin capacitor.

A short description of the THD waveshaper circuit:

- D11 rectifies the negative peak of the V_{AUXPFC};
- R24 and C15 buffer the rectified signal with the correct time-constant
- C14 injects the compensation current into the COMPPFC pin. The capacitance determines the amount of compensation

The time-constant of R24 and C15 is $R24 \times C15 > 1\ ms$.

Determine the best value for C14 by measurement.

3.15 GPFC pin: PFC gate driver

Place a series resistor in track to the gate of the MOSFET. A typical value for this resistor is 22 Ω.

The strong switch-off capability ensures that the external MOSFETs are not switched on due to the current through the gate-drain capacitance of the external MOSFET.

a. Sink and source currents   b. Gate drive resonant components

Fig 32. PFC and half-bridge MOSFET driver diagram
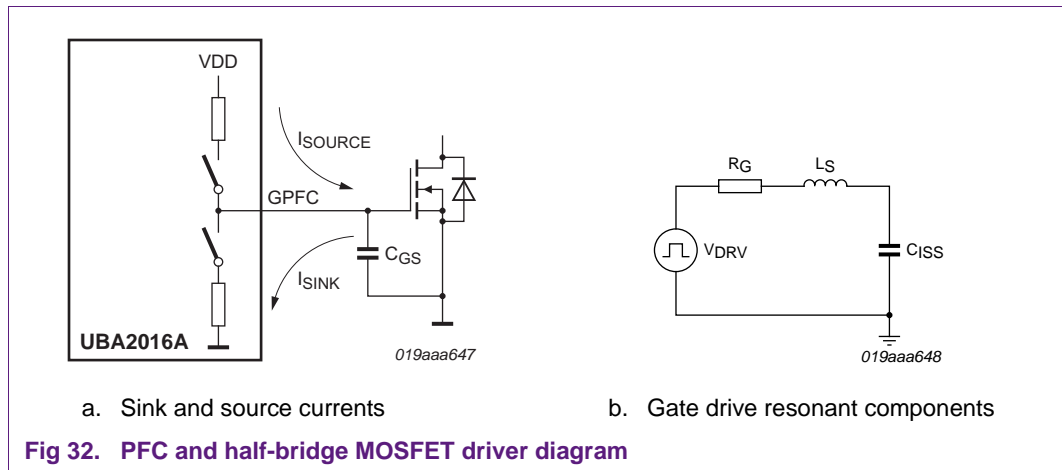
The IC MOSFET drivers capability is specified at the most interesting area (where the external MOSFETs are in the linear region).

I_{SOURCE} = −90 mA at V_{GS} = 4 V

R_{SINK} = 16 Ω at V_{GS} = 2 V

The sink resistance of 16 Ω is useful for damping the oscillation that can occur at the NMOST gate when the NMOST is switched off. In Figure 32b, L_S is the total inductance (track and source), C_{ISS} is the input capacitance of the NMOST as specified in the NMOST data sheet and R_G is the total series resistance (of the driver and of the NMOST).

Damping factor ξ of this series $R_G L_S C_{ISS}$ circuit is shown in Equation 31.

$$\zeta = R_G \times \frac{SQRT \times \left(\frac{C_{ISS}}{L_S}\right)}{2} \tag{31}$$

ξ must be greater than 0.5 (ideally >1) for sufficient damping.

3.15.1 VDD supply load

The major part of the power consumption from supply VDD is the gate drive. The amount of energy needed is linear to the switching frequency. Equation 32 the relationship between gate-charge and PFC switching and VDD supply current.

$$\Delta I_{VDD(PFC)} = Q_{g(PFC)} \times f_{PFC} \tag{32}$$

Where $Q_{g(PFC)}$ is the total gate charge as specified in the NMOST data sheet.

There is also gate charge needed for the two half-bridge NMOSTs which are not synchronized to PFC switching.

The GPFC track contains large current spikes; ensure that next to the GPFC track a low-ohmic return ground is present in the layout. The track width determines the inductance per cm, therefore use wide tracks for gate drive signals in case large NMOSTs are used. The ground track next to the signal track also reduces the inductance per cm.

3.16 GND pin: IC ground reference

The GND pin is the reference ground for the IC. Isolate the small signal ground and the large signal (gate drive currents, half-bridge switching currents and PFC switching currents) in the PCB layout.

3.17 VDD pin: IC supply and gate-drive supply

The application diagram for the VDD pin is shown in Figure 34.

Refer to Figure 33. At power-on, the VDD supply determines when the IC starts oscillating. Initially, the start-up current is charging the VDD capacitor. The VDD voltage rises and passes the threshold $V_{rst(VDD)}$ = 4.2 V. When the reset level is passed, the gate drive of the low side switch is equal to VDD. This voltage charges the floating supply capacitor via the internal bootstrap diode.

(1) Time t0: start charging VDD capacitor.

(2) Time t3: start oscillation, VDD takeover supply active.

(3) Time t4: preheat timer end.

(4) Time t5: lamp-on detected, transition to burn state.

Fig 33. Normal start-up behavior
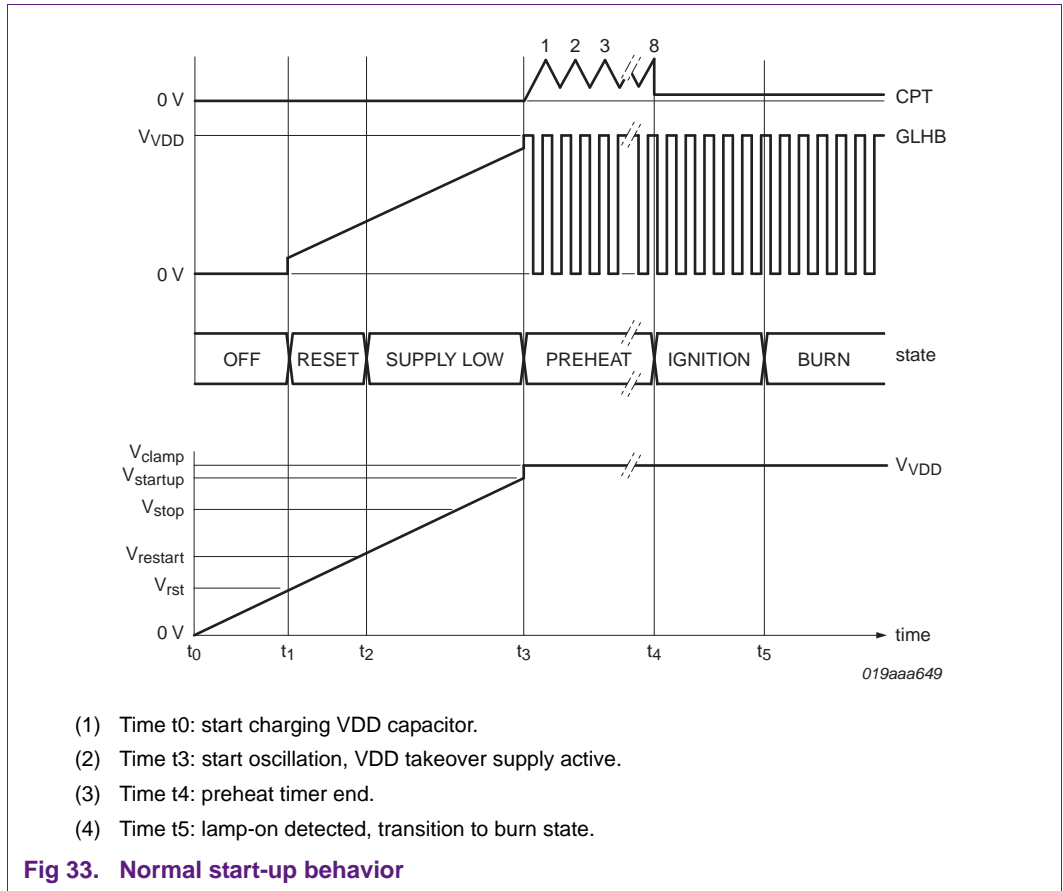
At the moment V_{VDD} passes the threshold $V_{startup(VDD)} = 12.4$ V, the gate drivers become active and Preheat state is entered. In Preheat state, capacitor C20 in the VDD takeover supply must deliver the energy to the IC and gate drivers.

Capacitor C20 is part of the dV/dt supply that connects to the half-bridge switching node SHHB. On each rising edge of the SHHB node a current is fed through C20 and diode D13b to the buffer capacitor C23. C20 determines the amount of current.

When C20 has a high value (> 470 pF), replace D13a by a 14 V Zener diode (1N5244) to keep within the V_{DD} pin voltage limits.

AN10958

Application note **Rev. 2 — 9 August 2012** **40 of 56**
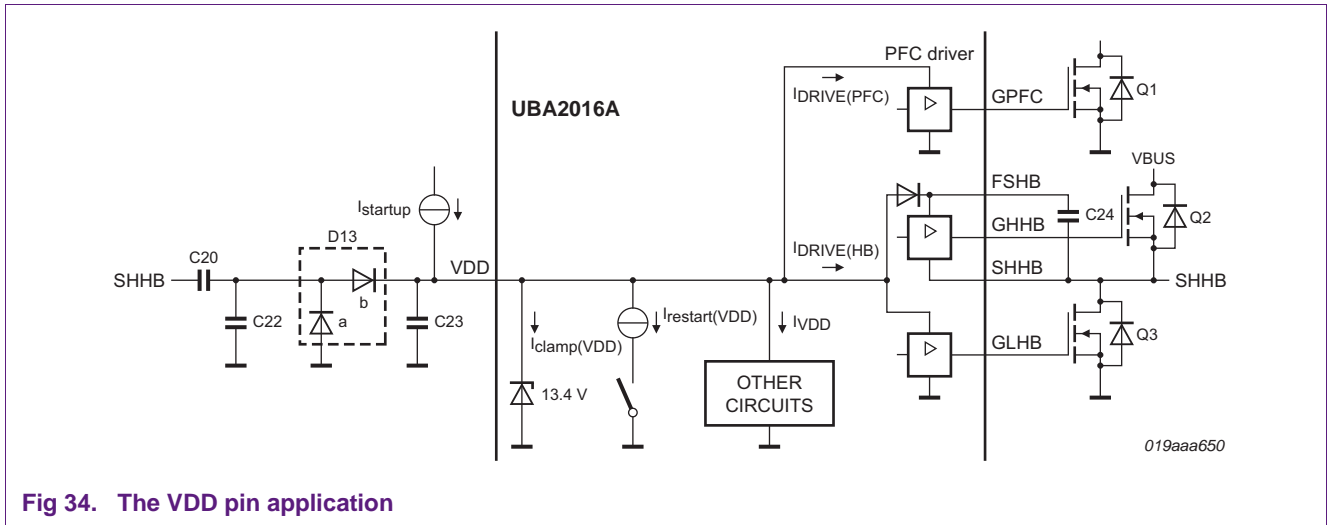
Fig 34. The VDD pin application

The VDD current consumption depends on the state of the IC.

- Stop (standby), Reset and Supply LOW state: The current consumption is 240 μA_{typ}.

- Preheat, Ignition and Burn state: Both PFC and HBC are switching. The MOSFET drivers are dominant in current consumption. Initially the VDD current comes from the VDD buffer capacitor C23 but the dV/dt supply circuit takes over. The current consumption (excluding the MOSFET driver) is 1.7 mA (typ). For typical FETs in a 35 W application the VDD current is 10 mA.

- Auto-restart state: The current consumption is 1.1 mA (typ). This current overrules the current $I_{startup}$ and the VDD capacitor is discharged. This state is used for multiple ignition attempts.

3.17.1 dV/dt capacitor

The VDD supply current is mostly determined by the NMOST types and internal drivers, a small part (only 1.7 mA) is needed for internal circuitry.

Equation 33 calculates capacitor C20.

$$C20 \ = \ 1.3 \times \frac{(2 \times Q_{g(HB)} + Q_{g(PFC)} + I_{VDD}/f_{low(HB)})}{VBUS} \qquad (33)$$

Factor 1.3 is a margin; $Q_{g(HB)}$ and $Q_{g(PFC)}$ are the total gate charges of the HB and PFC NMOST; VBUS is the bus voltage, I_{VDD} = 1.7 mA and $f_{low(HB)}$ = 40 kHz or 20 kHz in case of boost.

The calculated value is the minimum value for capacitor C20, a typical value is 330 pF. The margin in the formula depends on the tolerances in the design. Take care not to exceed maximum current $I_{clamp(VDD)}$ = 25 mA of the internal clamp.

AN10958

Application note **Rev. 2 — 9 August 2012** **41 of 56**

3.17.1.1 Buffer capacitor

A buffer capacitor C23 is required at the VDD pin. Current peaks can be localized by placing an SMD ceramic capacitor at position C23, close to the IC. The value of C23 is approximately 100 times larger than the total gate capacitance of all MOSFETs to prevent significant voltage drop during the discharge time of C23. Equation 34 calculates the value of C23.

$$C23 > \pm 100 \times (2 \times C_{iss(HB)} + C_{iss(PFC)}) \tag{34}$$

A typical capacitor for C23 is a 470 nF, 0805, 50 V, X7R ceramic type.

3.17.1.2 Start-up bleeder resistor

This resistor connects to the PFC output bus voltage or the Double-Sided Rectified (DSR) mains. The bus capacitor holds the bus voltage and is only slowly discharged by the bleeder resistor, so DSR mains connection is preferred. The DSR mains connection results in a shorter off-time in a power-on-off-on cycle.

The start-up current must be sufficient to supply the $I_{standby(VDD)}$ = 240 μA. The start-up current must be lower than $I_{restart(VDD)min}$ = 850 μA otherwise the IC cannot leave the Auto-restart state. Equation 35 calculates the start-up current.

$$I_{startup} = 1.2 \times I_{standby(VDD)} \tag{35}$$

The ballast mains start voltage $V_{ac(start)}$ must be < $V_{ac(min)}$ RMS as shown in Equation 36.

$$V_{ac(start)} = 0.9 \times V_{ac(min)} \tag{36}$$

The start-up bleeder resistor R31 determines the start-up current ($I_{startup}$).

$$R31 = \frac{SQRT(2) \times V_{ac(start)}}{I_{startup}} \tag{37}$$

3.18 GLHB pin: Low-side half-bridge gate-driver

The application for this pin is identical to the GPFC pin (see Section 3.15 on page 38).

The GLHB is 12 V in standby state to pre-charge the floating supply capacitor on the FSHB pin. Note this when designing a ballast that must detect the hot-side filament of the lamp.

Connect the gate of the lower half-bridge MOSFET to the GLHB pin using a small series resistor to prevent oscillation caused by parasitics. Oscillations increase stress on the MOSFETs. Do not use a too high resistor value to prevent switching the MOSFET on via its Miller capacitance.

3.19 SHHB pin: hard switching, capacitive mode, ground of high-side driver, source of the dV/dt supply

In normal operation, the half-bridge is Zero-Voltage-Switching (ZVS), which means that the SHHB circuit node has commuted before the NMOST switches on. The SHHB node capacitance is charged or discharged by the current of the half-bridge inductance; the impedance of the half-bridge circuit is "inductive". However, at low operating frequencies (overpower) or sudden removal/damage of the load (lamp) the impedance of the half-bridge circuit can become capacitive. Capacitive means that there is no commutation current to charge and discharge de SHHB node.

3.19.1 Hard switching

ZVS is assumed if the voltage step on the SHHB node is below 30 V.
When the voltage step on the SHHB node is above 100 V then hard switching is assumed.

3.19.2 Capacitive mode

Capacitive mode protection is triggered when the voltage rise during the non-overlap time of the low-to-high transition of the SHHB node remains under $V_{th(cm)(SHHB)} = 30$ V/μs.

If the slope of the voltage rise is > 30 V/μs, then hard switching or ZVS can be assumed.

3.20 FSHB pin: supply for high-side driver

Connect the FSHB pin to the SHHB pin using capacitor C24. The capacitor must hold the charge for the internal high-side driver. The supply structure is shown in Figure 34 on page 41.

When SHHB is switched to GND current flows via the bootstrap internal diode and high-voltage switch into C24. The high-side driver is supplied from this capacitor when SHHB is above GND. The voltage drop across the internal diode and high-voltage switch is $V_{Fd(bs)} = 1.5$ V.

A typical value for C24 is 100 nF which is sufficient for most applications.

3.21 GHHB pin: High-side half-bridge gate driver

The application for this pin is identical to the GPFC pin (see Section 3.15 on page 38).

Connect the gate of the higher half-bridge MOSFET to the GHHB pin use a small series resistor to prevent oscillation caused by parasitics.

4. Application description

4.1 Power supply

The power supply to the IC includes several functions:

- Clamping by the internal clamping diode
- Restart internal current source
- Supply of the IC drivers function
- Supply of the IC controller function blocks

4.1.1 IC supply structure overview

The VDD pin is the power supply pin. Internally the supply pin is clamped to 13.4 V by the integrated clamp and excessive VDD current ($I_{clamp(VDD)}$) is removed. The 13.4 V is used for the internal circuitry and for the integrated MOSFET drivers. An integrated bootstrap diode supplies the GHHB driver.

The VDD pin connects to an external buffer capacitor which can be charged from one of several sources:

- Charge current $I_{startup}$ from the bus voltage
- A dV/dt supply connected to the half-bridge
- Auxiliary supply from a winding on the half-bridge transformer
- External DC supply from a standby supply

4.1.2 Start-up

It is possible to restart after a relamp action without a ballast power cycle of the ballast when the start-up current is fed through the lamp filament at restart.

4.1.3 Restart

To provide multiple ignition attempts, the Auto-restart state is implemented. In the auto-restart state, the IC is not oscillating and there is an extra current ($I_{restart(VDD)}$ = 1.1 mA) drawn from VDD. When $I_{restart(VDD)}$ is larger than $I_{startup}$, a restart is triggered when the VDD < $V_{restart(VDD)}$ = 6.2 V. The restart timing also depends on C23.

4.1.4 Stop

The IC stops operating when the VDD voltage < $V_{stop(VDD)}$ to prevent unreliable switching of the half-bridge and PFC circuit. The IC enters Supply-low state.

4.2 Choice of the VBUS voltage

In order for the PFC step-up converter to work correctly, the bus voltage must be higher than the maximum input voltage.

$$V_{BUS} > 1.125 \times \sqrt{2} \times V_{ac(max)} \tag{38}$$

At the lowest HB switching frequency the bus voltage must be sufficient to reach the required lamp current with an HB inductance.

$$V_{BUS} > \sqrt{3} \times 8 \times f_{hb(min)} \times L_{hb(res)} \times I_{lamp(max)} \tag{39}$$

At the nominal HB switching frequency, the bus voltage must be sufficiently high to support the required lamp voltage.

$$V_{BUS} > \frac{V_{lamp(nom)} \times pi}{\sqrt{2}} \tag{40}$$

Equation 38,Equation 39 and Equation 40 provide the minimum value requirements for VBUS.

4.3 PFC stage design

The $t_{off(low)}$ parameter limits the maximum switching frequency $f_{high(PFC)}$. The minimum switching frequency $f_{low(PFC)}$ is a design parameter. Keep $f_{low(PFC)}$ above the audible range for humans and animals (30 kHz) during normal operation.

Normal operating voltage range: $V_{ac(rms)(min)}$ to $V_{ac(rms)(max)}$.

Nominal power: PF > 0.9 and $f_{low(PFC)}$ > 30 kHz.

The inductance L_{PFC} can be calculated for a certain $f_{low(PFC)}$ as shown in Equation 41.

$$L_{PFC} = \frac{V_{ac(rms)(max)}^2 \times (VBUS - \sqrt{2} \times V_{ac(rms)(max)})}{2 \times f_{low(PFC)} \times \frac{P_{lamp}}{\eta} \times V_{BUS}} \tag{41}$$

Remark: If the boost function is used over the complete input voltage range, the P_{lamp} must be the maximum lamp power during boost.

Equation 42 shows the calculation of the maximum peak current $I_{pk(max)(PFC)}$ of the PFC inductor operating in critical conduction mode.

$$I_{pk(max)(PFC)} = \frac{2 \times \sqrt{2} \times \frac{P_{lamp}}{\eta}}{V_{ac(rms)(min)}} \tag{42}$$

Application requirements: Efficiency η = 0.9; P_{lamp} = 49 W; $V_{ac(rms)(min)}$ = 180 V to give:
$$I_{pk(max)(PFC)} = 856 \; mA$$

Valley-detection needs additional ringing time within every switching-cycle. The ringing time adds short periods while no power is transferred to the PFC output. The PFC controller compensates for the ringing with a slightly higher peak current. A rule of thumb is that the peak current in a boundary condition mode, PFC with valley skipping is a maximum of 10 % higher than the calculated peak current in boundary conduction mode as shown in Equation 43.

$$I_{LPFC(sat)} = 1.1 \times I_{pk(max)(PFC)} \tag{43}$$

The RMS current in the PFC inductor.

AN10958

Application note Rev. 2 — 9 August 2012 **45 of 56**

$$I_{LPFC(rms)} = 2 \times \frac{P_{lamp}}{SQRT(3) \times V_{ac(min)} \times \eta} \tag{44}$$

Once the inductance L_{PFC} and saturation current $I_{pk(max)(PFC)}$ are known, the PFC inductor can be designed. The design requirements must include the following:

- Inductance
- Saturation current at maximum operating temperature
- Maximum RMS current to determine the temperature increase
- Switching node close to core for low EMI
- Winding ratio primary: auxiliary

The winding ratio calculation is described in and shown as: $(Np)/(Ns) = 0.11 \times V_{BUS}$.

The low frequency output voltage peak-to-peak ripple:

$$V_{BUS(pk-pk)} = \frac{P_{lamp}}{2 \times \pi \times f_{ac} \times V_{BUS} \times C_{BUS}} \tag{45}$$

Where $V_{BUS(pk-pk)}$ is chosen to be from 10 % to 15 % of V_{BUS}.

Once the ripple currents are measured in the application for certain capacitor values, the capacitor manufacturer can help support life-time calculations.

Suggested capacitor series for ballast applications are: Rubycon BX series, Nippon KXG and Panasonic EB type A.

4.4 Half-bridge circuit

The basic half-bridge circuit consists of an LC tank. Before the lamp is ignited, the LC tank is not damped and the voltage across the lamp strongly depends on the switching frequency. Electrode heating is applied while the lamp voltage is below the ignition voltage and the switching frequency is above the resonant frequency. After preheating, the lamp is ignited by sweeping the switching frequency down towards the resonant frequency. After ignition (Burn state), the lamp acts as a resistive load on the LC tank. The inductor limits the current though the lamp.

There are several topologies for heating the lamp electrodes. The conventional and inductive heating is addressed in the following sections.

4.4.1 Conventional heating

See Figure 35. In Preheat state, the half-bridge current flows through C_{DC}, C_{res} and the electrodes of the lamp (except a small amount which flows through C electrode). Once the lamp is ignited, the half-bridge current also flows through the lamp and the resonant tank (Lres Cres) is damped.

This type of circuit is used when lamp current control is not required. The half-bridge controller controls the switching frequency.

L_{res}: limits the lamp current in normal operation.

C_{res}: generates the ignition voltage.

$C_{electrode}$: reduces the electrode current in nominal operation.

R_{SLHB}: limits the half-bridge current during preheat and sets the saturation current.

Fig 35. The SLHB pin and conventional heating
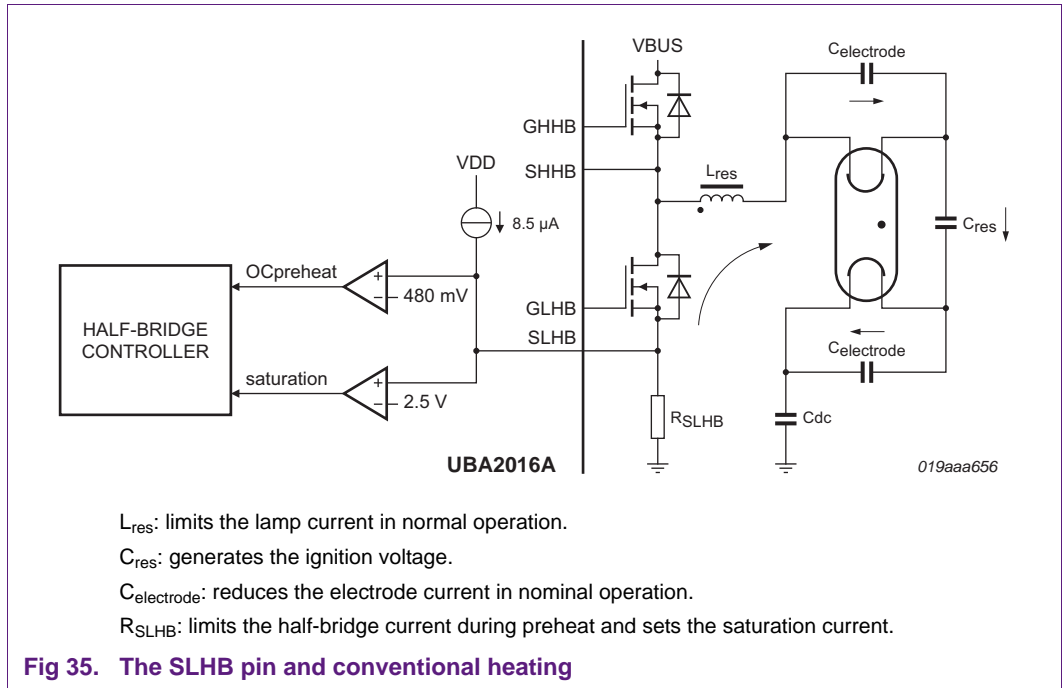
4.4.2 Inductive mode heating

See Figure 36. In Preheat state, the half-bridge current flows through L_{res} and the electrodes of the lamp (no current flows through C_{DC}). Once the lamp is ignited, the half-bridge current also flows through the lamp and the resonant tank ($L_{res}C_{res}$) is damped. The current though the C_{DC} capacitor is equal to the lamp current, as a result the lamp current can easily be measured.

This type of circuit is used if lamp current control is required, such as dimming.

L_{res}: inductor coupled to L_{sec}, limits the lamp current in normal operation.

C_{res}: generates the ignition voltage.

$C_{electrode}$: reduces the electrode current in nominal operation.

L_{sec}: inductor coupled to L_{res}, determines the amount of electrode current.

R_{SLHB}: limits the half-bridge current during preheat and sets the saturation current.

Fig 36. The SLHB pin and inductive heating

4.4.3 Half-bridge current control

Saturation regulation level is a fixed ratio (5×) to the preheat regulation level. The saturation level must support worst case (cold and old lamp) ignition voltages.

If the default application (factor 5) is selected, the preheat current through the half-bridge is: $I_{worstcase(ignition)} < 5 \times I_{ph}$; see Figure 37.
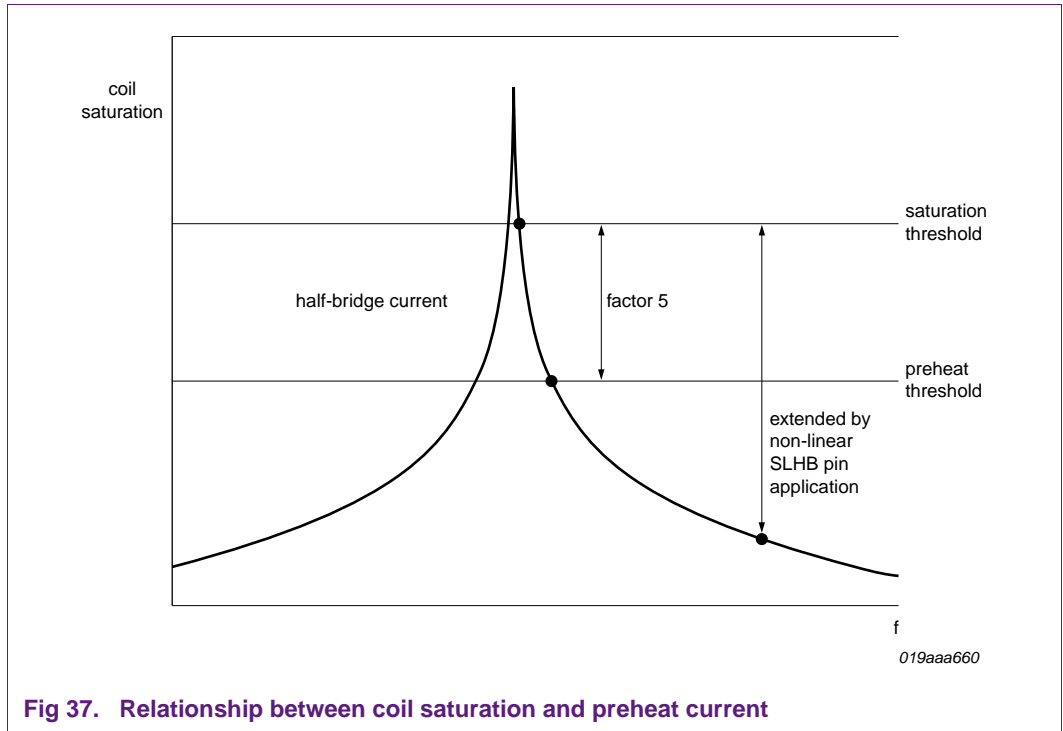
Fig 37. Relationship between coil saturation and preheat current

4.5 Layout guide

Figure 38 is an application example of a dual-layer PCB where the component-side layer tracks are Gray and the soldering-side tracks are Red, Blue and Cyan. The Blue track is the ground plane, a part of which is used as a small signal ground. This small signal ground is highlighted in Cyan. This ground is used for the components listed after Figure 38 to minimize the pickup of noise in case of deep dimming and ignition. Route the IFB track next to a ground plane or track for this reason.
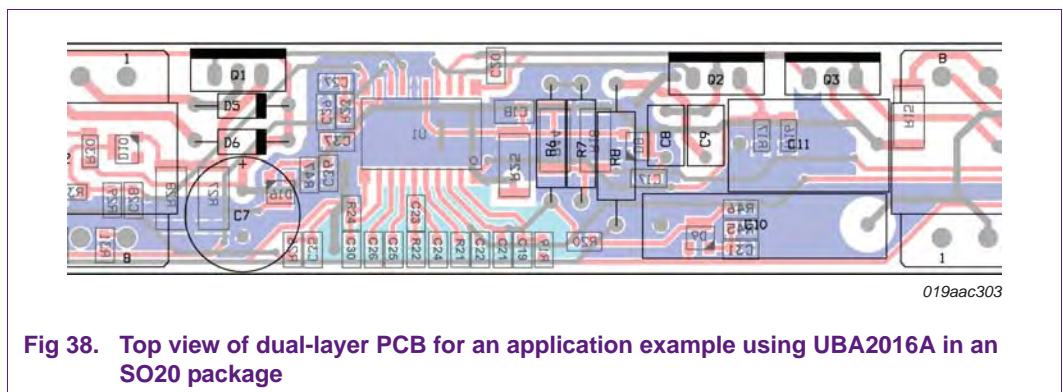
Fig 38. Top view of dual-layer PCB for an application example using UBA2016A in an SO20 package

A separate small signal ground is recommended for the following:

- Pin 2, IFB: C19
- Pin 3, EOL: C21
- Pin 4, VFB: C22
- Pin 5, IREF: R21

- Pin 6, CIFB: R22, C24
- Pin 7, CF: C25
- Pin 8, CPT: C26
- Pin 9, DIM: C30
- Pin 10, BOOST, C30

Figure 39 is an example of an application of a single-layer PCB whose tracks are shown Red, Blue and Cyan. The Blue track is the ground plane, a part of which is used as a small signal ground. The small signal ground is highlighted in Cyan and is used for the following components to minimize the pickup of noise in case of ignition. IFB is connected to ground because the example is a non-dimmable application.
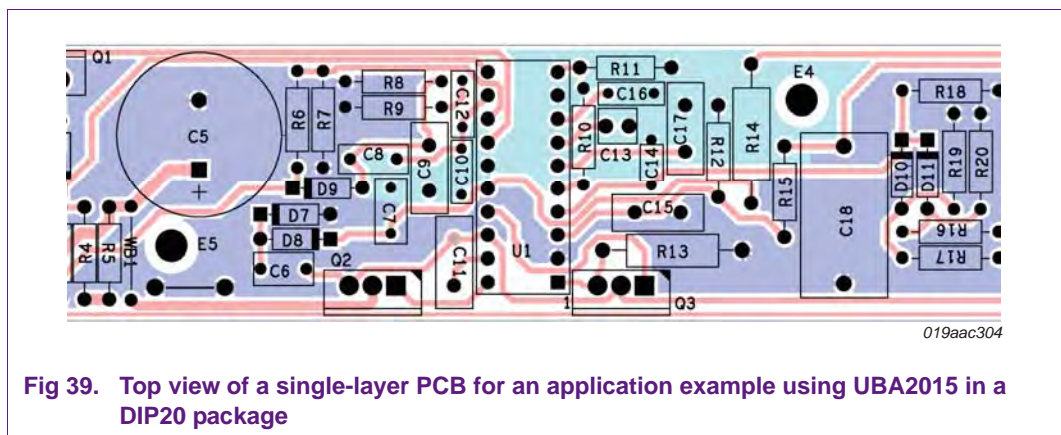
Fig 39. Top view of a single-layer PCB for an application example using UBA2015 in a DIP20 package

A separate small signal ground is recommended for:

- Pin 3, EOL: C15
- Pin 4, VFB: C14
- Pin 5, IREF: R10
- Pin 6, CIFB: C17
- Pin 7, CF: C13
- Pin 8, CPT: C16
- Pin 10, PH/EN, R11
- Pin 15, GND
- Pin 16, VDD: C7

AN10958

Application note **Rev. 2 — 9 August 2012** **50 of 56**

4.6 Tips and tricks

4.6.1 PFC disable

The PFC controller can be disabled using the options shown in Table 7.

Table 7. PFC disable options
Shows the options for disabling the PFC controller for experimental purposes.

Pin connection			PFC mode	PFC behavior
AUXPFC	**COMPPFC**	**FBPFC**		
Open	FBPFC	COMPPFC	disabled	FBPFC regulates to approximate 1.1 V, disabled protection: brownout, FBPFC, OSP, FBPFC, overvoltage, EOL window changes because FBPFC voltage is lower
Open	GND	1.27 V	disabled	FBPFC must be set externally to 1.27 V from bus voltage for normal EOL window, disabled protection: brownout, FBPFC, OSP, FBPFC, overvoltage, EOL window does not change because FBPFC is set to 1.27 V

If COMPFC and FBPFC are interconnected, then the FBPFC voltage regulates to 1.1 V. As a result the EOL pin thresholds change, the EOL bias current is also slight different at V_{EOL} = 1.65 V. Table 8 the new values are shown.

Table 8. EOL characteristics
$V_{fb(PFC)}$ = 1.1 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th(low)EOL}$	low threshold voltage on pin EOL		1	1.1	1.2	V
$V_{th(high)EOL}$	high threshold voltage on pin EOL		2	2.25	2.5	V
$I_{bias(EOL)}$	bias current on pin EOL	V_{EOL} = 1.65 V	15.4	16.2	17	µA

As the FBPFC/COMPFC node has a high–impedance, it could pick up noise. Therefore it connect a 10 nF to GND. A typical application is shown in Figure 40.
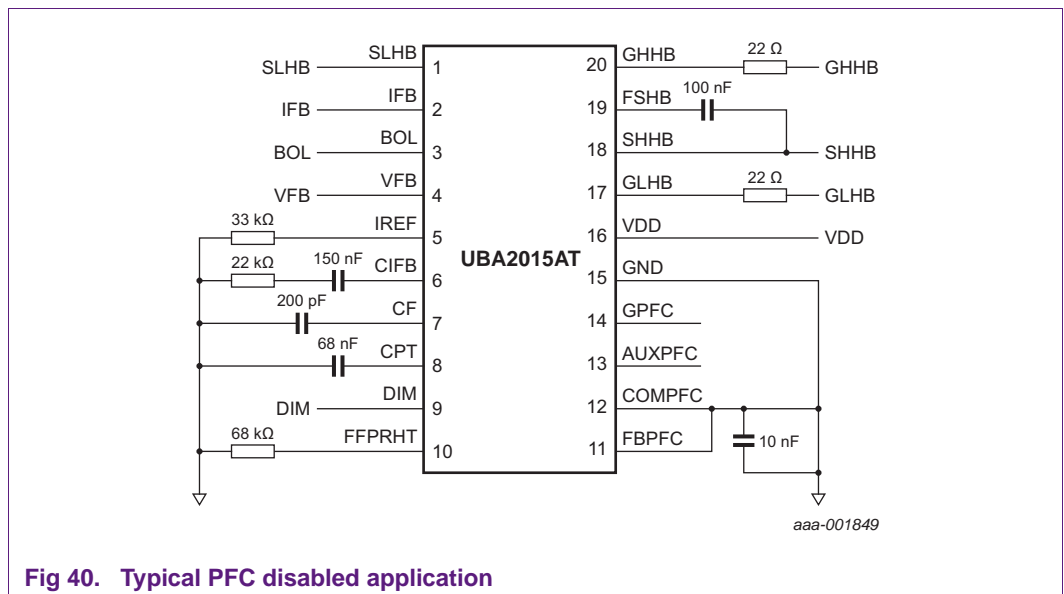
Fig 40. Typical PFC disabled application

AN10958

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Application note **Rev. 2 — 9 August 2012** **51 of 56**

4.7 Power-on of new ballast design

4.7.1 Test 1: check for short-circuits

Apply voltage to the VDD pin via 330 Ω resistor and 20 V laboratory supply.

Start-up the supply from 0 V and monitor the current and voltage on the VDD pin.

The VDD voltage clamps at about 13 V to 14 V. Do not increase VDD above 14 V or permanent damage occurs.

4.7.2 Test 2: check if oscillation stage is reached

Switch VDD supply to 0 V.

Apply 1.27 V to the FBPFC pin to enable switching of the MOSFETs.

Increase VDD until clamping occurs, when using 330 Ω in series, the laboratory supply can be increased to less than 20 V while keeping the internal clamp within specification.

The gate drive signals (PFC and half-bridge) show some activity when the VDD passes the start-up threshold.

4.7.3 Test 3: check half-bridge functionality

Switch VDD and FBPFC to 0 V.

Connect diode to the CPT pin and connect its cathode to ground, to disable the preheat and fault timer.

Apply 1.27 V to the FBPFC pin and 12.9 V to the VDD pin.

Connect a 400 V laboratory supply to the bus capacitor and set the current limit to 200 mA.

Slowly increase the bus voltage from 0 V to between 20 V and 30 V, and monitor the laboratory supply current. Monitor the bus voltage (PFC output voltage) and the source high-side of the half-bridge. Monitor the voltage across the resonant capacitor: the average voltage must be V_{BUS} / 2.

4.7.4 Test 3: check half-bridge functionality

Remove VDD, FBPFC and bus laboratory supply.

Remove diode from the CPT pin.

Connect 400 V, DC laboratory supply to the AC input, and set the current limit to 200 mA.

Slowly increase the laboratory supply voltage from 0 V to between 20 V and 30 V, and monitor the laboratory supply current and the VDD voltage.

Check if PFC starts regulating if the FBPFC voltage > 1.0 V.

4.7.5 VFB disable

Connect a laboratory supply of 500 mV to the VFB pin. Make sure that the lamps are inserted because high voltage can occur in the LC tank.

4.7.6 EOL disable

Connect a laboratory supply of 1.9 V to the EOL pin.

5. Abbreviations

Table 9.   Abbreviations

Acronym	Description
EMI	ElectroMagnetic Interference
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOST	N-channel Metal Oxide Semiconductor Transistor
SMD	Surface-Mounted Device
VCO	Voltage-Controlled Oscillator

6. References

[1] **UBA2016A/15/15A -** 600 V fluorescent lamp driver with PFC, linear dimming and

[2] **UM10359 -** UBA2016AT demo board 1 × 28 W dim and boost user manual

[3] **UM10466 -** UBA2015P reference design 2 × 35 W T5 non-dimmable 230 V(AC) user manual.

[4] **UM10486 -** UBA2015P reference design 2 × 35 W T5 non-dimmable 120 V (AC) user manual.

[5] **UM10438 -** UBA2015AP evaluation board 1 × 35 W T5 dimmable 120 V (AC) user manual.

[6] **UM10440 -** UBA2015AT reference design 2 × 35 W T5 dimmable 230 V (AC) user manual.

[7] **UM10513 -** UBA2015AT reference design 2 × 35 W T5 dimmable 120 V (AC) user manual.

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8. Contents

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