AN10932

120 V high power factor dimmable CFL with UBA2014

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Document information

Info	Content
Keywords	CFL, high power factor, free running PFC, triac, dimmable, UBA2014
Abstract	This application note describes the design of a dimmable Compact Fluorescent Lamp (CFL) with a high power factor for use with the UBA2014

Revision history

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v.2	20110117	third version
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v.1	20101012	initial version

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1. Introduction

This application note describes the design of a dimmable CFL with a high Power Factor (PF) where in practice, a PF greater than 95 % is realized. An 18 W application with the UBA2014 and SPS04N60C3 external MOSFETS is described.

A CFL dimmer which is representative of most dimmers for 120 V mains input applications, is used as the triac wall dimmer. When using other dimmers some component values in the application may need adjusting to ensure dimming compatibility.

The topology is based on a combined free running PFC with resonant half-bridge inverter. OverVoltage Protection (OVP) is required and under voltage lockout (UVLO) is optional for deep dimming.

An external no-lamp detection/protection circuit has been added to the main board for evaluation in a laboratory set-up with different burners. This circuit is not necessary when the lamp ballast and burner are enclosed in a CFL housing.

2. Triac dimming

2.1 Triac dimming circuit

Figure 1 shows the circuit diagram of a triac wall dimmer for 120 V (RMS) mains input.

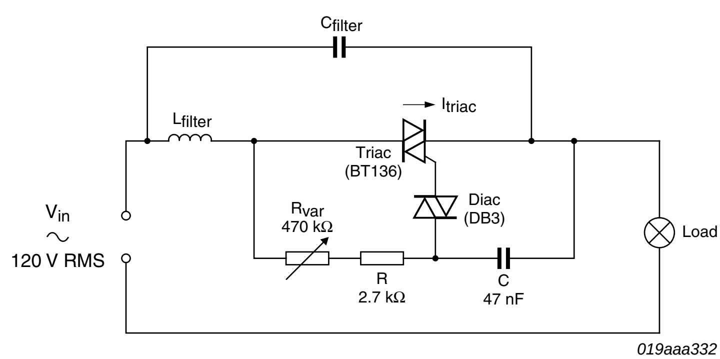


Fig 1. Triac wall dimmer with LC filter

The triac employs forward phase-cut dimming, in which the load (i.e. incandescent lamp, CFL etc.) is energized only during the last portion of each power-line half cycle (α to π and $\alpha + \pi$ to 2 π) as shown in Figure 2.

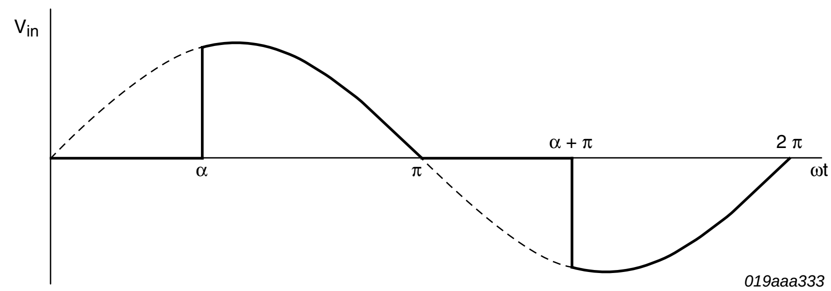


Fig 2. Triac with phase-cut dimming angle α

The capacitor (C = 47 nF) is charged via the combination of a fixed and a variable resistor where the phase-cut dimming angle is set with the variable resistor.

When the resistance is low, the capacitor will be charged more quickly and once the break overvoltage of the diac is reached, the triac fires immediately and current I_{triac} flows. This current continues to flow until I_{triac} drops below its minimum holding current I_H

The triac is a bidirectional device that works in two quadrants as indicated in Figure 3 so the same process is repeated during the negative half cycle.

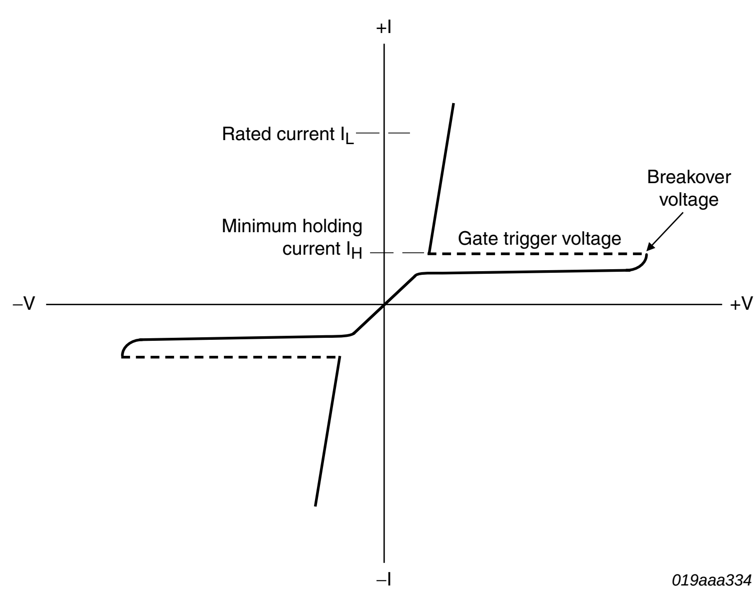


Fig 3. Typical triac V_I characteristics

The L_{filter} and C_{filter} filter in the triac application (or LC filter in CFL application) can produce ringing of the triac current when the triac latches after a step response. The triac ringing current should remain above I_H to keep the triac switched on.

2.2 Triac wall dimmer and CFL ballast with separate PFC

In this application, the load is a CFL ballast (i.e. a half-bridge, resonant tank and lamp) and a separate PFC as indicated in Figure 4.

The PFC maintains triac conduction once the triac current is greater than the minimum hold current I_H where an I_H of 15 mA to 20 mA is sufficient for most triac dimmers.

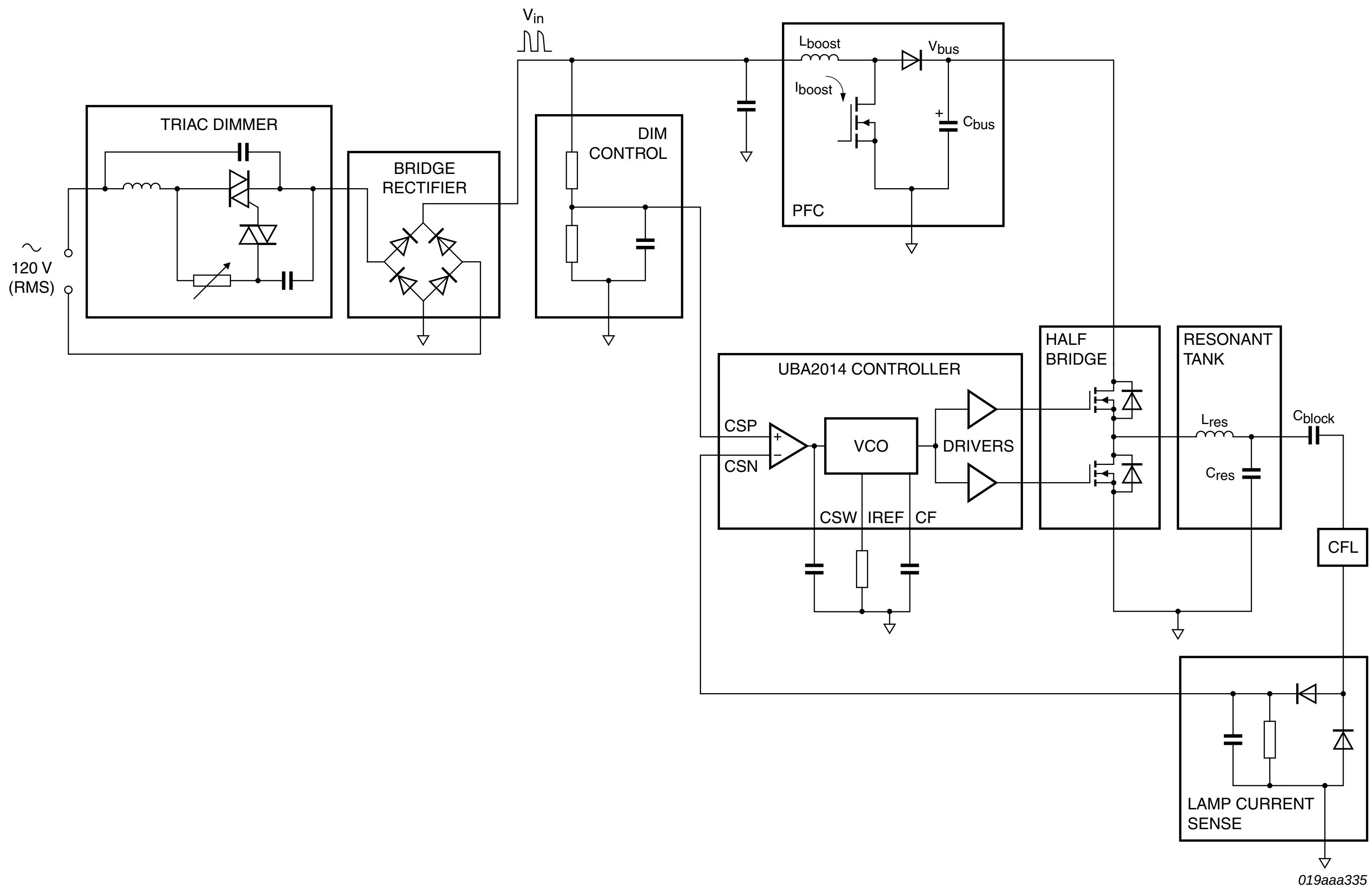
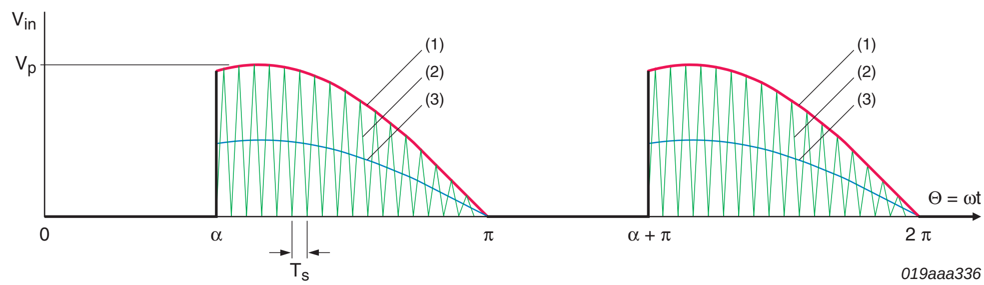


Fig 4. Triac wall dimmer with separate PFC and CFL ballast

Figure 5 shows the triac phase angle (α), input voltage (V_{in}), boost current (I_{boost}) and average boost current ($I_{boost(AV)}$).



(1) V_{in}

(2) I_{boost}

(3) $I_{boost(AV)}$

Fig 5. Input waveforms as function of phase cut angle α

The PFC operates in discontinuous conduction mode (DCM) and the average input boost current follows the input mains voltage which gives a power factor (PF) = 1.

An extra MOSFET is required for this topology and its gate drive is provided either by a separate controller or the lower gate driver of the UBA2014. This extra MOSFET for the PFC can be eliminated by combining the half-bridge MOSFETs for both the PFC and CFL ballast. This is called a combined free running or free-ride PFC.

2.3 Triac wall dimmer and CFL ballast with combined free running PFC

The CFL ballast and combined free running PFC is shown in Figure 6. The half-bridge MOSFETs are used to switch both the resonant tank circuit and the boost circuit. In Section 5 the relevant waveforms are shown (see Figure 20).

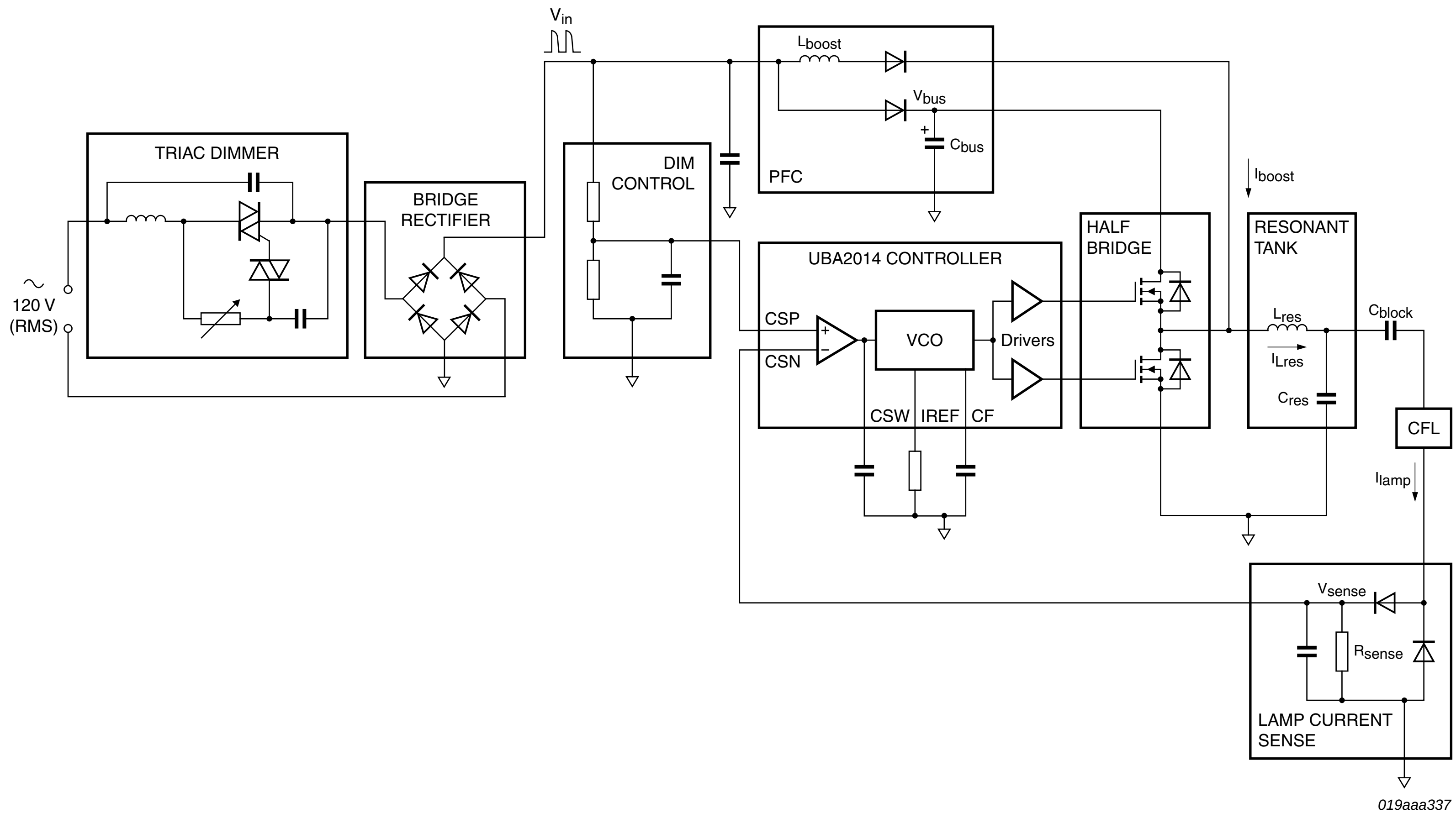


Fig 6. Triac wall dimmer with combined free running PFC and CFL ballast

A diode in series with L_{boost} to the half-bridge ensures that no reverse current flows if the average voltage at the half-bridge (V_{bus} / 2) is greater than the instantaneous voltage at the double rectifier bridge output.

During dimming (i.e. light load operating conditions), the bus voltage (V_{bus}) can increase since the power delivered from the PFC boost can exceed the power used by the CFL burner. To prevent overstress on the MOSFETs and bus capacitance in this situation OverVoltage Protection (OVP) has been implemented.

The dimming control signal for pin CSP is derived from the average of the mains rectified signal. This control signal decreases during dimming and the frequency regulation loop of the UBA2014 simultaneously increases the frequency of the half-bridge so as the voltages on pins CSN and CSP are similar (see Section 3.4).

3. Application design

3.1 UBA2014 block diagram

The block diagram (Figure 7) shows the basic configuration of the high PF dimmable CFL using the UBA2014.

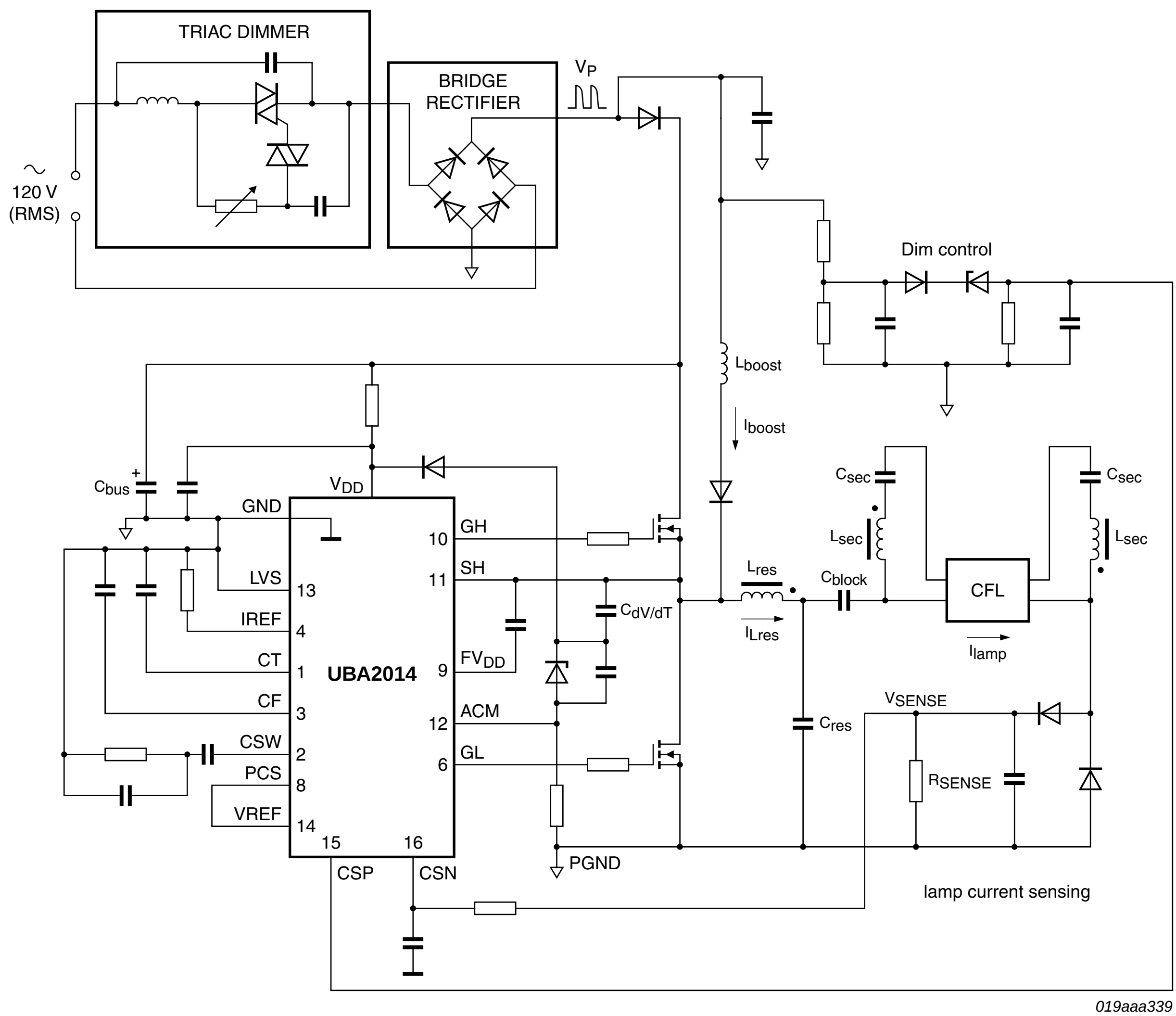


Fig 7. Block diagram of a high power factor dimmable CFL with the UBA2014

3.2 PFC and resonant parameters

The input power delivered by the PFC without dimming ($\alpha = 0$) is:

$$P_{in}(\omega_s) = \frac{(\delta \cdot V_P)^2}{\omega_s \cdot L_{boost}} \cdot \int_{\alpha}^{\pi} \frac{\sin^2(\theta)}{1 - \frac{V_P}{V_{bus}}\sin(\theta)} d\theta \text{ [W]} \quad (1)$$

where V_P = peak input voltage, δ = inverter duty cycle, $T_S = 1 / f_S$ is the half-bridge switching cycle, V_{bus} = bus voltage, L_{boost} = PFC inductor, α = triac firing angle (refer to Figure 5 and Figure 6). The PFC is maintained in DCM operation when:

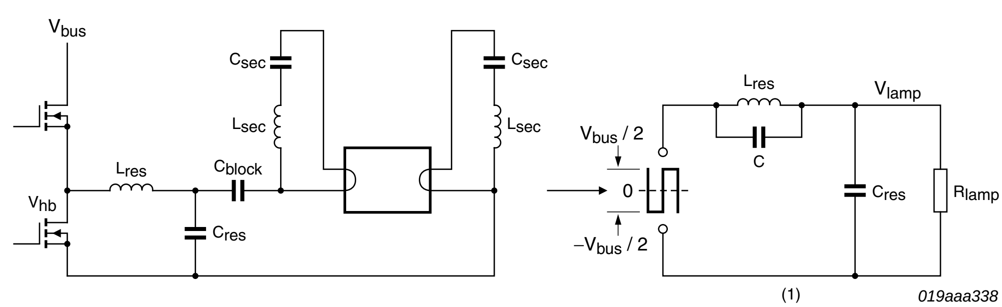
$$\frac{V_{bus}}{V_P} > \frac{1}{1 - \delta} \quad (2)$$

Refer to Ref. 3 for further information on the derivation of P_{in}.

The power delivered to the lamp is:

$$P_{lamp} = \frac{V_{lamp}^2}{\omega_s L_{res}} \sqrt{\left(\frac{\sqrt{2} \cdot V_{bus}}{\pi \cdot V_{lamp}}\right)^2 (1 - \omega_s^2 L_{res} C)^2 - (1 - \omega_s^2 L_{res}(C + C_{res}))^2} \quad (3)$$

where $\omega_S = 2\pi f_S$, V_{lamp} = lamp RMS voltage, L_{res} = resonant inductor, C_{res} = resonant capacitor, C = secondary capacitance of inductive mode heating circuit transferred to primary side. The expression for P_{lamp} in Equation 3 is derived using the equivalent circuit shown in Figure 8.



$$1^{st} \text{ harmonic of } V_{hb} = \frac{\sqrt{2}}{\pi} V_{bus} \text{ (RMS)}$$

(1) $C = 2\frac{L_{sec}}{L_{res}} C_{sec}$ and $R_{lamp} = \frac{V_{lamp}^2}{P_{lamp}}$

Fig 8. Resonant tank equivalent for inductive mode heating

The relationship between the power delivered from the mains and the power delivered to the lamp is given by:

$$P_{lamp} = \eta \cdot P_{in} \quad (4)$$

A realistic value for the efficiency η is 80% (see Ref. 4 for efficiency calculations for this application).

The value for the PFC inductor, L_{boost}, can be calculated using Equation 1 once the values for P_{in}, V_P, δ, T_s, V_{bus} and α are known.

The resonant inductor is the dominating component for the power delivered to the lamp (P_{lamp}), however, the resonant capacitor (C_{res}) also has influence. The current in the MOSFETs increases for larger a C_{res} while for smaller C_{res} the possibility of hard switching increases because the resonant tank is no longer inductive.

An optimum is reached for C_{res} when the MOSFET current is minimized while C_{res} remains large enough so that hard switching does not occur for a given dV/dt capacitance ($C_{dV/dt}$) on the half-bridge node.

Once C_{res} is chosen and P_{lamp}, V_{lamp}, f_s and V_{bus} are known, then L_{res} can be calculated using Equation 3. The value of C is already known from preheat requirements as described in Section 3.3.

The calculations are described in Section 4 on page 23. Table 1 gives practical values of L_{res}, L_{boost} and C_{res} for different CFL powers.

Table 1. L_{res}, L_{boost} and C_{res} values for different CFL powers

Conditions are f_s = ~ 45 kHz, α = 0 (no dimming), V_{bus} = 350 V, V_P = 120, η = 80 %; Note $P_{in} = P_{lamp} / \eta$

P_{in}	L_{boost}	P_{lamp}	V_{lamp}	C_{res}	L_{res}
30 W	2.5 mH	24 W	80 V	5.6 nF	2 mH
25 W	2.75 mH	20 W	110 V	4.7 nF	2.75 mH
22.5 W	3 mH	18 W	100 V	3.9 nF	3 mH
22.5 W	3 mH	18 W	80 V	4.7 nF	2.5 mH
20.5 W	3.5 mH	16.5 W	80 V	4.7 nF	2.75 mH

The instantaneous current in each MOSFET which is $I_{boost} - I_{hb}$ is calculated in Section 5 on page 25 where I_{hb} is the sum of the current through the resonant inductor L_{res} and the current to the dV/dT capacitor. The RMS current is approximately 410 mA. The instantaneous current $I_{boost} - I_{hb}$ together with the $C_{dV/dt}$ capacitor determine the rise time (t_r) or fall time (t_f) of the half-bridge voltage according to Equation 5.

$$\frac{I_{boost} - I_{hb}}{C_{dV/dt}} = \frac{V_{bus}}{t_r, t_f} \qquad (5)$$

Using $C_{dV/dt}$ = 470 pF, t_r and t_f (i.e. rise and fall non-overlap times) remain within specification.

3.3 Inductive mode preheating and electrode currents

Adequate filament preheating is needed to ensure long life operation of the lamp and enables ignition at a lower ignition voltage. The preheat current (I_{ph}) is supplied to the filaments during the preheat period and is set using Equation 6.

$$t_{ph} = 1.8 \cdot \left(\frac{C_{CT}}{330 \cdot 10^{-9}}\right)\left(\frac{R_{IREF}}{33 \cdot 10^{3}}\right) \quad (6)$$

The preheat time is 1.2 s when C_{CT} = 220 nF and R_{IREF} = 33 kΩ.

The preheat frequency (f_{ph}) can be set to f_{max} (i.e. 100 kHz) by connecting pin PCS to V_{REF} = 3 V. It is also possible to set the preheat frequency by measuring the voltage across the PCS resistor between the source and ground of the lower MOSFET (see Figure 18 on page 22). The half-bridge frequency starts at f_{max} and sweeps down until the voltage on the PCS pin reaches the V_{ph} level (defined in the UBA2014T specification). The sweep then stops for the duration of the preheat time (t_{ph}).

During the preheat time the frequency is controlled ensuring the voltage on pin PCS remains constant, implying the half-bridge current is kept constant. The value of this current can be adapted by changing the PCS resistor's value. Care should be taken that the lamp is not ignited during the preheat time. The frequency as a function of time is shown in Figure 9.

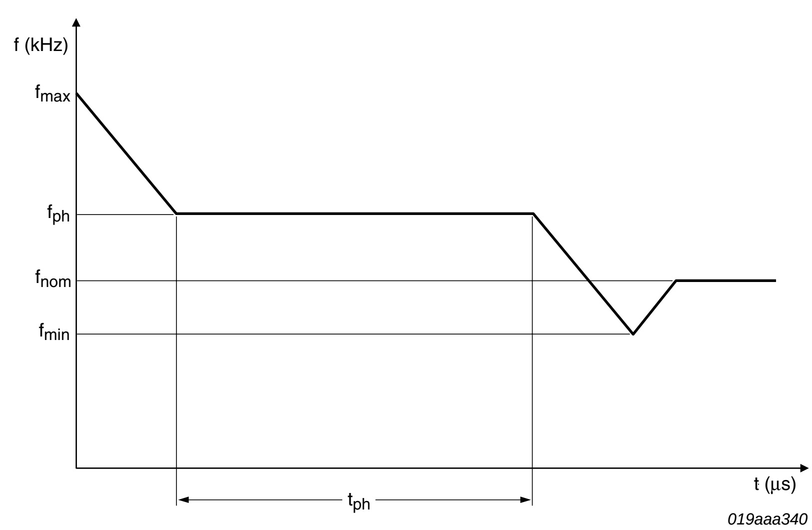


Fig 9. Frequency as a function of time during start up

The relationship of the preheat (filament) current for inductive mode heating is calculated in Section 6 on page 28.

For example: when the half-bridge frequency is 100 kHz and the non-overlap time is 0.5 µs, the RMS filament current is then 0.18 A. Then power dissipated in filament is circa 1.6 W when R_{fil} = 50 Ω. The power supplied to the filament P_{fil} during preheat is given by Equation 7.

$$P_{fil} = f_s \cdot C_{sec} \cdot V_{sec}^2 \quad (7)$$

$$V_{sec} = \frac{V_{pri}}{n} \tag{8}$$

$$n = \sqrt{\frac{L_{res}}{L_{sec}}} = 16 \tag{9}$$

The primary voltage V_{pri} = 350V and for n = 16, the power supplied to the filament is approximately 1.6 W when C_{sec} = 33 nF, L_{res} = 2.75 mH and L_{sec} = 10 μH.

To ensure sufficient filament current is available at the end of the preheat period, the hot to cold ratio of filament resistance should be approximately 5 : 1.

After the preheat period the frequency sweeps down further and the lamp will ignite once the ignition frequency f_{ign} is reached. The lamp can be modeled now as a (negative) resistance where:

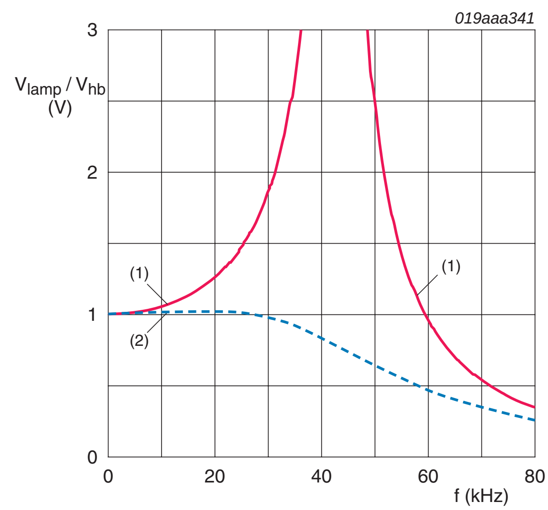
$$R_{lamp} = \frac{V_{lamp}^2}{P_{lamp}} \tag{10}$$

Before ignition, the lamp has a much higher impedance as no-lamp current is flowing. Both characteristics are shown in Figure 10.

The internal VCO frequency (and thus the frequency of the half-bridge) is determined by capacitor C_{CF}, resistor R_{IREF} and the voltage on pin CSW. The minimum frequency calculation is shown in Equation 11 and the maximum frequency calculation is shown in Equation 12.

$$f_{min} = 40.5 \times 10^3 \cdot \left(\frac{100 \times 10^{-12}}{C_{CF}}\right) \cdot \left(\frac{33 \times 10^3}{R_{IREF}}\right) \tag{11}$$

$$f_{max} = 2.5 \times f_{min} \tag{12}$$



(1) Before ignition.

(2) After ignition.

Fig 10. Transfer of resonant tank versus frequency before and after ignition

After lamp ignition, the filaments must be powered adequately to maintain the optimal temperature over the full dimming range. A temperature which is too low will cause sputtering or local hot spots resulting in damage to the filament while excessive temperature will cause evaporation of the filament over a longer period. The SoS (Sum of Squares) is a measure of the amount of heat that should be generated in the filaments and is expressed by Equation 13.

$$SoS = I_{LH}^2 + I_{LL}^2 \quad (13)$$

Figure 11 shows the I_{LL} and I_{LH} direction with waveforms. The filaments are inductively preheated. The SoS should remain within the minimum and maximum settings (specified by the lamp manufacturer). However, remaining as close as possible to the target setting is preferred to ensure long life operation of the lamp. Further information is given in Ref. 2.

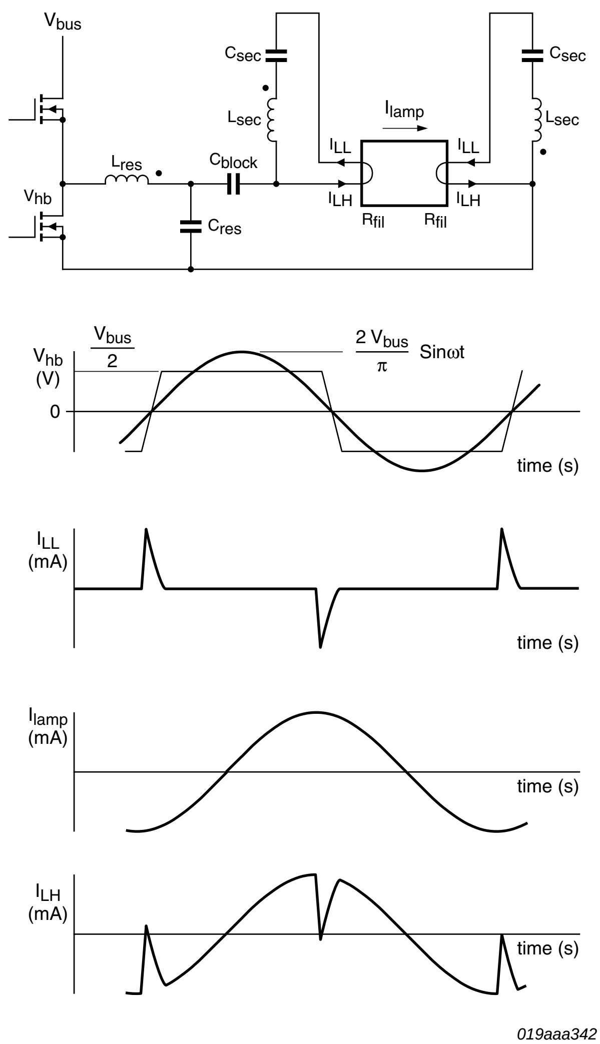


Fig 11. Lamp and filament currents for inductive mode heating

3.4 Dimming using lamp current feedback control loop

Once the lamp is ignited and the frequency of the half-bridge has reached minimum frequency then the internal Average Current Sensor (ACS) on pins CSP and CSN is enabled. The voltage on pin CSN is derived by sensing the lamp current and converting it to voltage using a sense resistor as shown in Figure 12.

The average voltage supplied to pin CSN is shown in Equation 14:

$$V_{CSN} = \frac{\sqrt{2}}{\pi} \cdot I_{lamp(RMS)} \cdot R_{SENSE} \qquad (14)$$

The ripple is reduced by adding a capacitor in parallel with R_{SENSE}.

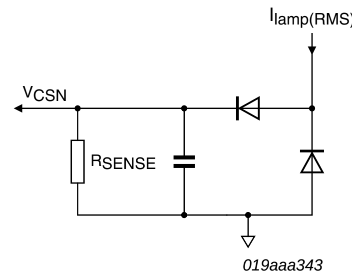


Fig 12. Lamp current sensing

The average voltage on pin CSP is derived from the mains rectified signal (shown in Figure 13) and is used to provide a dimming voltage range of 0 V to 2.2 V on pin CSP for a phase-cut range (α) of 0° to 120°. This voltage (after integrating with C4 and C5) is supplied to pin CSP where:

$$V_{CSP} = \left(\frac{\left(\frac{V_P(1 + \cos\ a)}{\pi} \cdot \frac{R4}{R2 + R4} \right) - V_D - V_z}{\frac{R4 \cdot R2}{R2 + R4} + R5} \right) \cdot R5 \qquad (15)$$

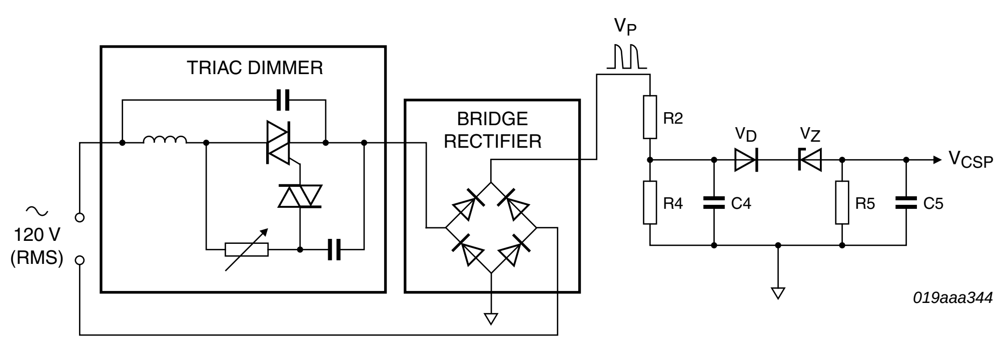


Fig 13. Triac dimming control

The loop regulation is in balance when the average voltage of V_{CSN} is equal to V_{CSP}. During dimming this regulation is achieved using frequency control as follows:

- V_{CSP} decreases
- the voltage on pin CSW decreases
- the frequency of the half-bridge increases
- the lamp current decreases
- the average value of V_{CSN} decreases

Therefore the loop regulation forces the average voltage of V_{CSN} to follow V_{CSP} until balance is reached.

3.5 Supply of the UBA2014 and capacitive mode protection

The UBA2014 starts when the supply voltage V_{DD} exceeds the trigger level $V_{DD(start)}$. The half-bridge begins to switch and the UBA2014 is then supplied using capacitor $C_{dV/dt}$ connected at the half-bridge (see Figure 14).

A larger capacitor is required when more current is needed by the external MOSFETs and the related internal gate which drive the external MOSFETs.

If capacitor $C_{dV/dt}$ is too large, hard switching at higher frequencies can occur because the non-overlap time decreases at higher frequencies (adaptive non-overlap time). A capacitor value of 470 pF is a good compromise between these two situations.

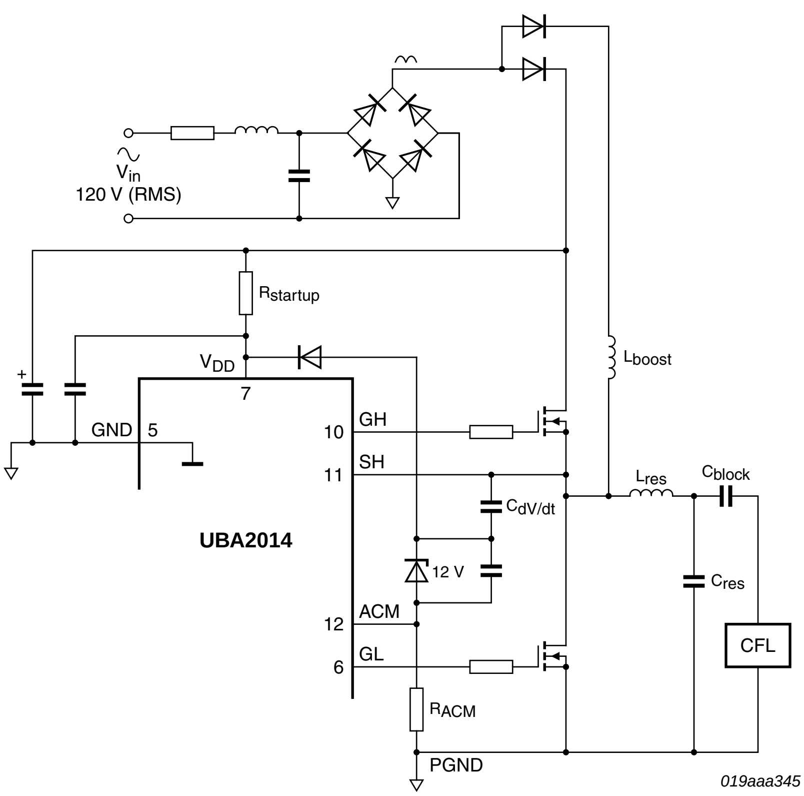


Fig 14. IC supply circuit

The voltage is clamped by a 12 V Zener diode and supplied to V_{DD} using a fast recovery diode. The charging current of capacitor $C_{dV/dt}$ is measured with resistor R_{ACM} and supplied to the UBA2014's capacitive mode detection input pin (pin ACM). Typical waveforms are shown in Figure 15.

If after the preheat state, the voltage across resistor R_{ACM} does not exceed the internal V_{CMD} during the non-overlap time then the internal Capacitive Mode Detection (CMD) circuit assumes capacitive mode operation at the half-bridge and consequently the half-bridge frequency is directly increased to f_{max}.

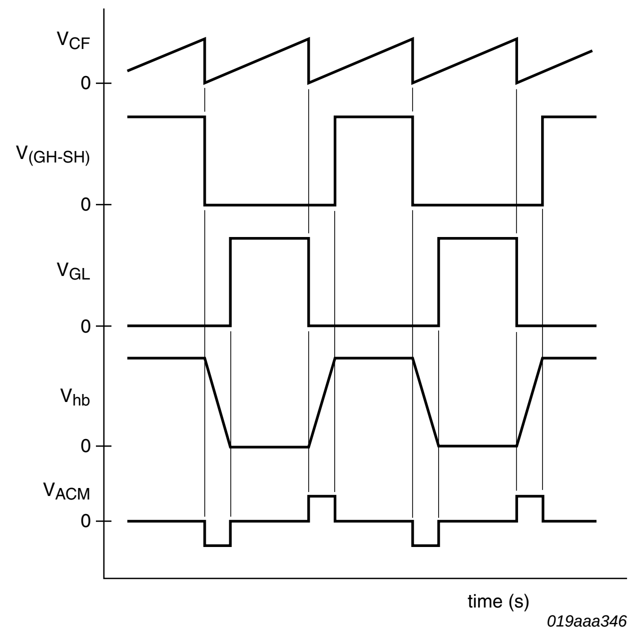


Fig 15. Driver, half-bridge and ACM signal

3.6 Mains input filtering

The boost current through the PFC coil switches at the half-bridge frequency. The RLC filter is used to filter this from the mains to ensure good EMI performance at the half-bridge frequency and harmonics. The inductor is blocking the HF boost current and the capacitor provides a low ohmic path for this current.

The damping of the HF current which is I_{HF} / I_{Vin} is calculated using Equation 16 where L = 4.7 mH, C = 100 nF and R = 10 Ω resulting in a attenuation of more than 60 dB (see Figure 16).

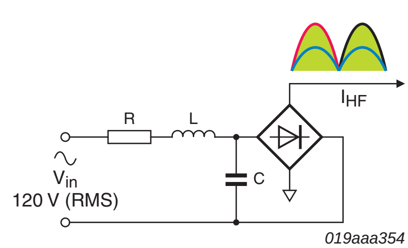


Fig 16. Transfer function input filter circuit

$$G(\omega) = 20log\left[\frac{1}{(1 + \omega^2 \cdot LC)^2 + (\omega \cdot R \cdot C)^2}\right] \quad (16)$$

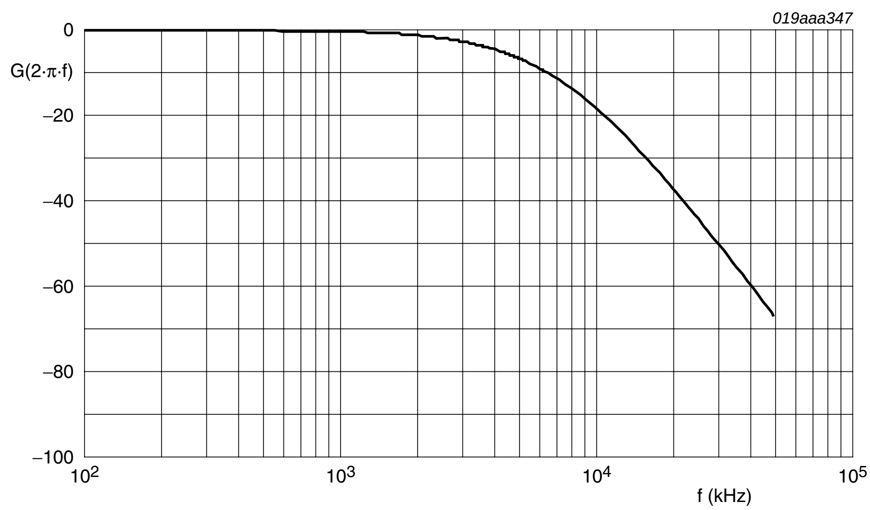


Fig 17. Transfer function input filter graph

The fused resistor R = 10 Ω is to limit/damp the inrush current during start-up and during large steps of input current during triac operation. More information is given in Ref. 1.

3.7 Extra protection circuits

The following sections describe the dedicated protection methods used in this application.

3.7.1 OverVoltage Protection (OVP)

Overvoltage protection (see Figure 18 on page 22) is needed to protect the MOSFETs from voltage transients during step dimming or fast transient dimming. During dimming, the half-bridge frequency increases. When $P_{boost} > P_{lamp}$ then the voltage V_{bus} increases.

The circuit monitors the bus voltage and if $V_{bus} > 400$ V (set by R7 shown in Figure 18), V_{CSN} is reduced by 10 % (set using R9 shown in Figure 18) and the half-bridge frequency decreases resulting in more power being supplied to the lamp and V_{bus} is discharged.

3.7.2 No-lamp protection

During development different CFL lamps can be connected or disconnected to the inverter and resonant tank. It is important to switch off the UBA2014 and application, when the lamp is disconnected to avoid damage to the external MOSFETs or UBA2014's MOSFET drivers.

The circuit monitors the current through the source of the lower MOSFET. If the current is greater than a factor two of the current during ignition (set by source resistors R26, R27 and R41 shown in Figure 18), the UBA2014 is powered down by reducing $V_{DD} < V_{DD(start)}$ using a two transistor latch as shown in Figure 18. The RC time constants R42/C42 and R43/C43 prevent the circuit from latching during fast spikes or disturbances.

Remark: The protection circuit is not necessary when the board is mounted in an integrated CFL housing and consequently, it is not part of the main CFL application.

3.7.3 UVLO

The CFL can be switched off using an extra current in parallel with the lamp for dimming of < 10 %. The current I_C through the UVLO capacitor C21 in Figure 18 is calculated as:

$$I_C = 2\pi \cdot f \cdot C \cdot V \tag{17}$$

At 10 % dimming, I_{lamp} = 20 mA, f = 50 kHz, V_{lamp} = 200 V and C = 220 pF then I_C = 10 mA.

Remark: The capacitor was not mounted in this application because no-lamp flicker was observed during deep dimming of the CFL.

3.8 Schematic diagram of the 18 W high power factor dimmable CFL

The full schematic of the application with a 18 W PL-C 4P CFL is shown in Figure 18. Refer to Ref. 4 for more details.

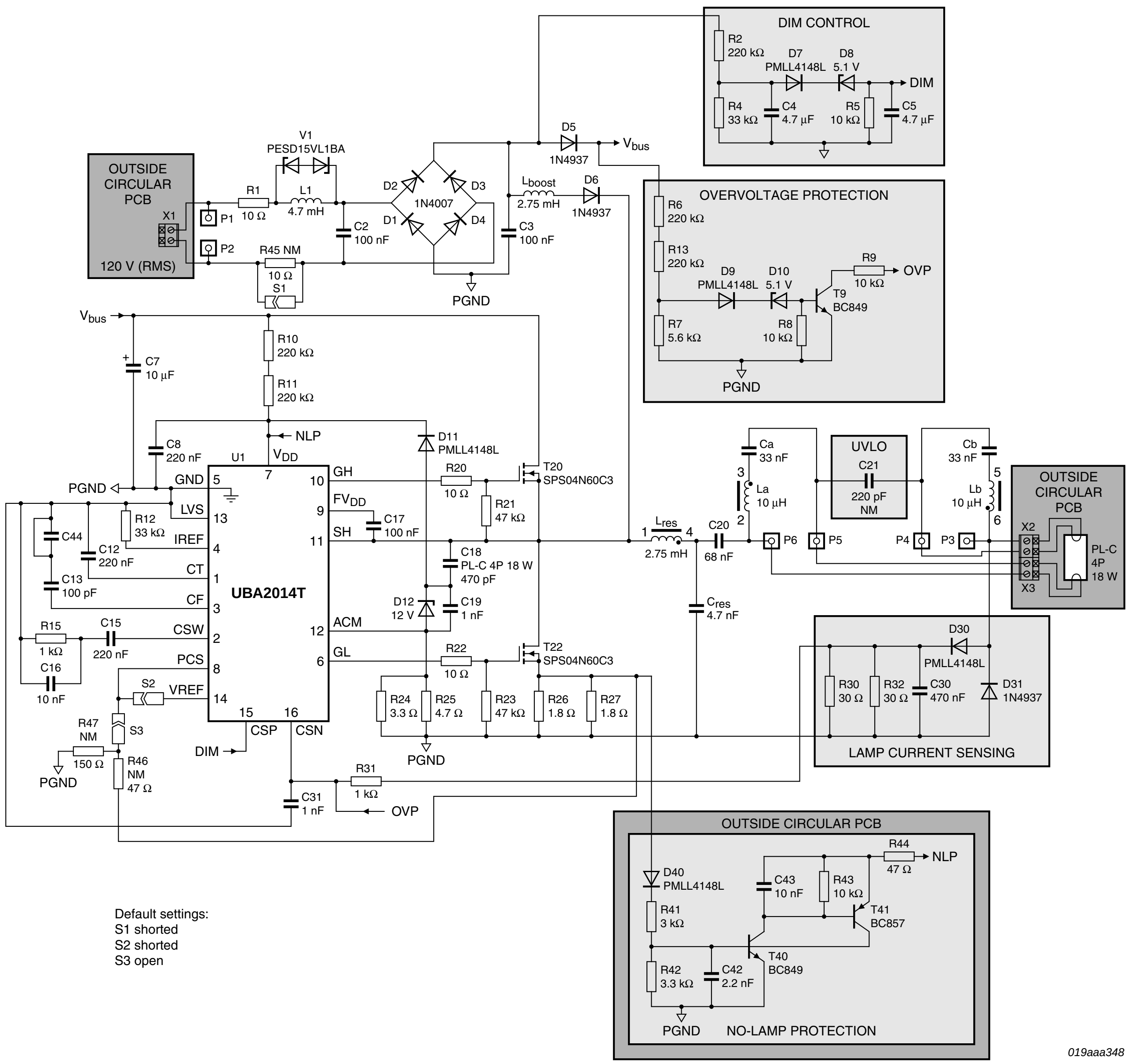


Fig 18. Schematic high power factor dimmable with a 18 W PL-C 4P CFL

4. Appendix 1: Power calculations

The nominal lamp power (no dimming, α=0) is calculated using Equation 20.
The run frequency is f_S = 45 kHz. The nominal mains input voltage V_{in} = 120 V (RMS) and $V_P = 120\sqrt{2} = 170\ [\mathrm{V}]$. The CFL has a RMS lamp voltage of 110 V and the bus voltage V_{bus} = 340 V

$$\frac{V_{bus}}{V_P} = \frac{1}{1-\delta} \tag{18}$$

where δ = 50 %.

To have a P_{lamp} of 20 W then L_{res} = 2.75 mH, C_{res} = 4.7 nF and

$$C = 2 \cdot \frac{L_{\mathrm{sec}}}{L_{res}} \cdot C_{\mathrm{sec}} = 240\ [\mathrm{pF}] \tag{19}$$

where C_{sec} = 33 nF and L_{sec} = 10 uH.

With efficiency η = 80 %, the input power is $P_{in} = P_{lamp} / \eta$ = 25 W.

P_{in} is calculated using Equation 21. With no dimming (α=0), a boost inductor value of L_{boost} = 2.75 mH is necessary to have P_{in} = 25 W.

The lamp power and input power are given in Equation 20 and Equation 21.

$$P_{lamp} = \frac{V_{lamp}^2}{\omega_s L_{res}} \sqrt{\left(\frac{\sqrt{2} \cdot V_{bus}}{\pi \cdot V_{lamp}}\right)^2 (1-\omega_s^2 L_{res} C)^2 - (1-\omega_s^2 L_{res}(C+C_{res}))^2} \tag{20}$$

$$P_{in}(\omega_s) = \frac{(\delta \cdot V_P)^2}{\omega_s \cdot L_{boost}} \cdot \int_{\alpha}^{\pi} \frac{\sin^2(\theta)}{1 - \frac{V_P}{V_{bus}}\sin(\theta)} d\theta\ [\mathrm{W}] \tag{21}$$

During dimming P_{in} changes according to the phase angle α of the triac as shown in Figure 19. The run frequency f_S increases due to the lamp current feedback control loop as explained in Section 3.4 The bus voltage changes based on the difference between P_{in} and P_{lamp}.

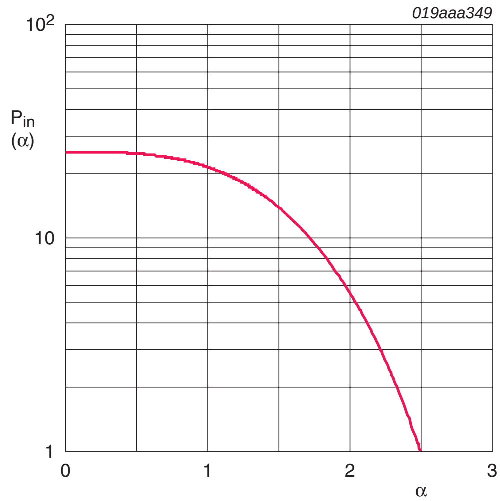


Fig 19. Input power as a function of the phase cut angle

5. Appendix 2: MOSFET current calculations

The MOSFET current calculations were performed using the following parameters: f = 45 kHz, C_{res} = 4.7 nF, R_{lamp} = 574.25 Ω, L_{res} = 2.75 mH, C = 240 pF and V_{bus} = 350 V, L_{boost} = 2.75 mH, δ = 50 %, $C_{dV/dt}$ = 470 pF, n = 0.1 to nmax and nmax = 32.

$$p = (2 \cdot \pi \cdot f) \cdot j \qquad (22)$$

$$T = \frac{1}{f}\ [\mathrm{s}] \qquad (23)$$

The resonant frequency is given in Equation 24.

$$f_{res} = \frac{1}{2 \cdot \pi \cdot (\sqrt{L_{res} \cdot C_{res}})} [\mathrm{Hz}] \qquad (24)$$

$$V_{pk} = 120 \cdot \sqrt{2}\ [\mathrm{V}] \qquad (25)$$

The voltage at the half-bridge is a square wave and represented by Equation 26 where $V_{hb1}(t)$ in Equation 27 is the first harmonic of $V_{hb}(t)$

$$V_{hb}(t) = \frac{V_{bus}}{2} + \frac{2 \cdot V_{bus}}{\pi} \cdot \sum_{n=1}^{nmax} \frac{\sin\left[2 \cdot \pi \cdot (2 \cdot n - 1) \cdot \frac{t}{T}\right]}{(2 \cdot n - 1)}\ [\mathrm{V}] \qquad (26)$$

$$V_{hb1}(t) = \frac{V_{bus}}{2} + \frac{2 \cdot V_{bus}}{\pi} \cdot \sin\left(\frac{2 \cdot \pi \cdot t}{T}\right)\ [\mathrm{V}] \qquad (27)$$

The admittance of the resonant tank, lamp and dV/dT capacitance at the half-bridge is Y(p) and given by Equation 28.

$$Y(p) = \frac{1}{R_{lamp}} \cdot \frac{(p^2 \cdot L_{res} \cdot C + 1) \cdot (p \cdot R_{lamp} \cdot C_{res} + 1)}{p^2 \cdot L_{res} \cdot (C_{res} + C) + p \cdot \frac{L_{res}}{R_{lamp}} + 1} + p \cdot C_{dV/dt} \qquad (28)$$

The current from the half-bridge is $I_{hb}(t)$ is given in Equation 29.

$$I_{hb}(t) = \left[|Y(p)| \cdot \left(\frac{2 \cdot V_{bus}}{\pi} \cdot \sin\left(\frac{2 \cdot \pi \cdot t}{T} + \arg(Y(p))\right)\right)\right]\ [\mathrm{A}] \qquad (29)$$

The boost current I_{boost} and MOSFET current is given in Equation 30 and Equation 31.

$$I_{boost}(t) = \frac{V_{pk} \cdot \delta \cdot T}{2 \cdot L_{boost}} + \frac{V_{pk} \cdot \delta \cdot T}{2 \cdot L_{boost}} \cdot \left[\frac{8}{\pi^2} \cdot \sum_{n=1}^{nmax} \left[\frac{\cos\frac{2 \cdot \pi \cdot (2n-1) \cdot t}{T}}{(2n-1)^2}\right]\right]\ [\mathrm{A}] \qquad (30)$$

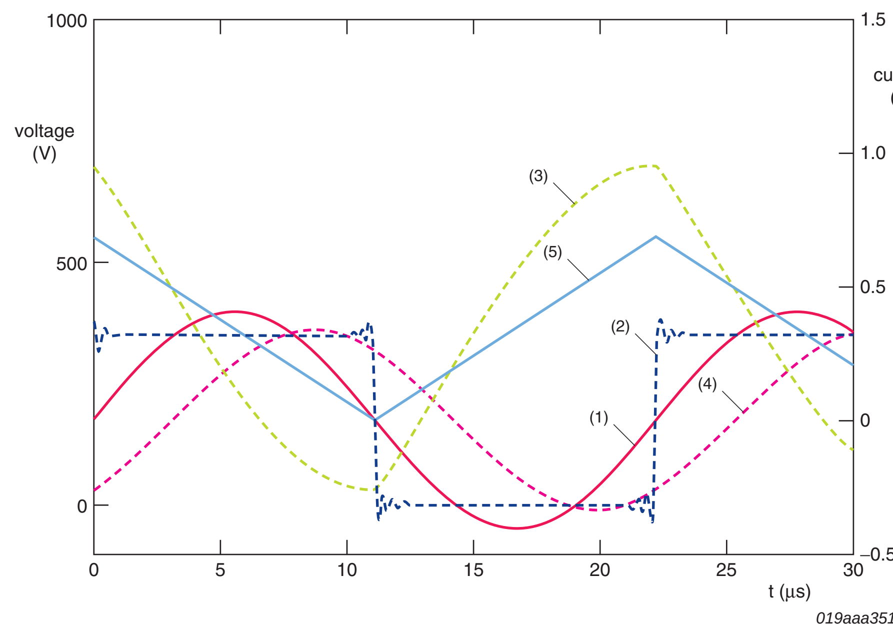
$$I_{fet(RMS)}(t) = \sqrt{\frac{1}{T} \cdot \int_0^T \left[\frac{2}{\pi} \cdot (I_{boost}(t)) - I_{hb}(t)\right]^2 dt}\ [\mathrm{A}] \qquad (31)$$

The calculated RMS MOSFET current amounts 408 mA.

When calculating the current in the MOSFETs, the average boost current over a line cycle is considered which is shown in Equation 32.

$$\frac{2}{\pi} \cdot (I_{boost}(t)) \tag{32}$$

In addition, $I_{hb}(t)$ is subtracted from $I_{boost}(t)$ because $I_{hb}(t)$ is the current flowing out of $V_{hb}(t)$ node. $V_{hb1}(t)$ is the first harmonic of the $V_{hb}(t)$.



(1) $V_{hb1}(t)$

(2) $V_{hb}(t)$

(3) $I_{hb}(t) + I_{boost}(t)$

(4) $I_{hb}(t)$

(5) $I_{boost}(t)$

Fig 20. Voltage and currents at half-bridge

In order to calculate the rise and fall times of the half-bridge voltage, the instantaneous boost current I_{boost} and the instantaneous bridge current I_{hb} at $\frac{T}{2}$ and T are calculated as shown in equations below:

$$I_{hb}\left(\frac{T}{2}\right) = 0.262 \text{ [A]} \tag{33}$$

$$I_{hb}(T) = -0.262 \text{ [A]} \tag{34}$$

$$I_{boost}\left(\frac{T}{2}\right) = 2.171 \text{ [mA]} \tag{35}$$

$$I_{boost}(T) = 0.684 \text{ [A]} \tag{36}$$

$$It_f = I_{boost}\left(\frac{T}{2}\right) + I_{hb}\left(\frac{T}{2}\right) = 0.264 \text{ [mA]} \tag{37}$$

$$It_r = I_{boost}(T) + I_{hb}(T) = 0.421 \text{ [mA]} \quad (38)$$

t_r is the time needed for the half-bridge voltage to rise from the minimum value to the maximum value. The rise and fall times are given in Equation 39 and Equation 40 with $C_{dV/dt}$ = 470 pF and V_{bus} = 350 V, t_f = 622. ns and t_r = 390 ns.

$$t_f = \frac{C_{dV/dt}}{It_f} \cdot V_{bus} \quad (39)$$

$$t_r = \frac{C_{dV/dt}}{It_r} \cdot V_{bus} \quad (40)$$

The specified UBA2014 rise and fall times: minimum t_f = 0.68 μs and t_r = 0.75 μs.

6. Appendix 3 Inductive mode preheat calculations

The inductive mode preheat calculations were performed with the following parameters: t_r is the time needed for the half-bridge voltage to rise from the minimum value to the maximum value. V_{bus} is 350 V, T_{hb} is 10 μs, t_r = 0.5 μs, f_{hb} = 100 kHz and m = 1 to 80.

$$f_{hb} = \frac{1}{T_{hb}} = 100\ [\mathrm{kHz}] \tag{41}$$

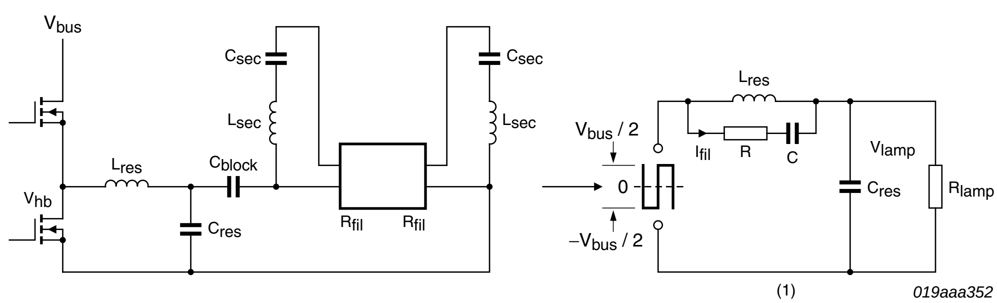
$$\gamma = \frac{t_r}{T_{hb}} \cdot \pi = 0.157 \tag{42}$$

$$t = 0, 0.001 \cdot T_{hb} \ldots 2 \cdot T_{hb} \tag{43}$$

The half-bridge voltage is represented by Equation 44 and Equation 45.

$$V_{hb\_f}(m) = j\frac{V_{bus}}{2 \cdot \pi \cdot \gamma} \cdot \frac{(-1)^m - 1}{m^2} \cdot sin(m \cdot \gamma) \tag{44}$$

$$V_{hb\_f}(t) = 2 \cdot Re\left[\sum_m (v_{hb\_f}(m) \cdot e^{j \cdot 2 \cdot \pi \cdot f_{hb} \cdot m \cdot t})\right] \tag{45}$$



(1) $C = 2\frac{L_{\mathrm{sec}}}{L_{res}}C_{\mathrm{sec}}$, $R = \frac{1}{2}\frac{L_{res}}{L_{\mathrm{sec}}}R_{fil}$ and $R_{lamp} = \frac{V_{lamp}^2}{P_{lamp}}$

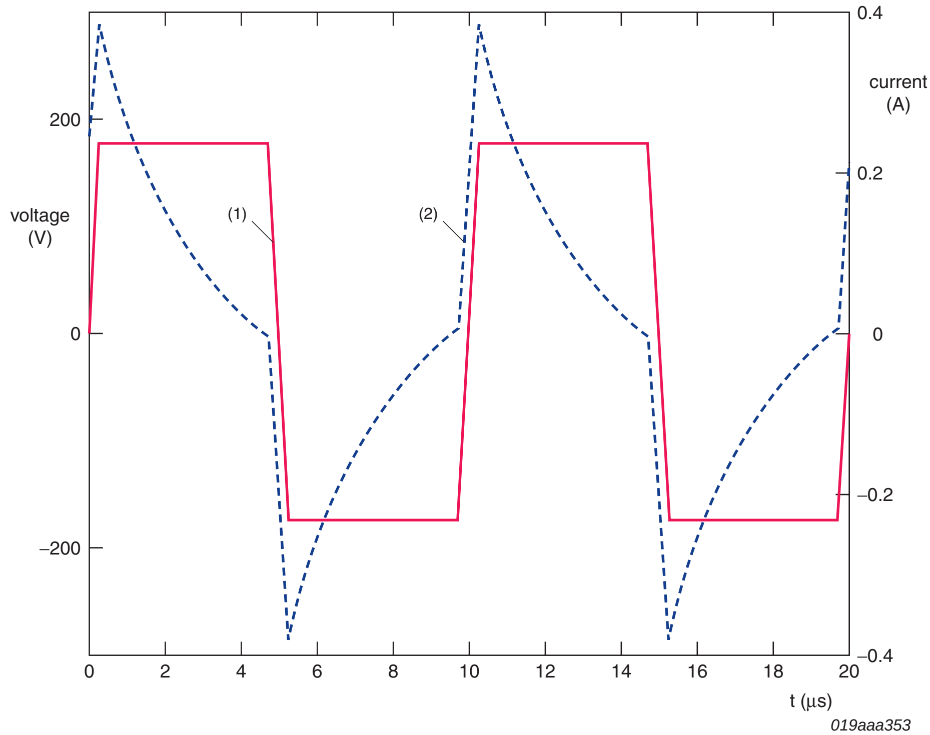
Fig 21. Inductive mode preheating

The current through the filament is given by Equation 46 using values of L_{sec} = 10 μH, C_{res} = 4.7 nF, C_{sec} = 33 nF and R_{fil} = 50 Ω.

$$I_{fil\_f}(m) = \frac{-(m \cdot \omega_{hb})^2 \cdot L_{res} \cdot C_{res} \cdot \sqrt{\frac{L_{\mathrm{sec}}}{L_{res}}}}{j \cdot 2 \cdot m \cdot \omega_{hb} \cdot L_{\mathrm{sec}} + R_{fil} + \frac{1}{j \cdot m \cdot \omega_{hb} \cdot C_{\mathrm{sec}}} - (m \cdot \omega_{hb})^2 \cdot L_{res} \cdot C_{res} \cdot R_{fil} + j \cdot m \cdot \omega_{hb} \cdot L_{res} \cdot \frac{C_{res}}{C_{\mathrm{sec}}}} \cdot v_{hb\_f}(m) \tag{46}$$

$$I_{fil(RMS)f} = \sqrt{2 \cdot \left[\sum_m (|I_{fil\_f}(m)|)^2\right]} \tag{47}$$

$$I_{fil\_t}(t) = 2 \cdot Re\left[\sum_m (I_{fil\_f}(m) \cdot e^{j \cdot 2 \cdot \pi \cdot f_{hb} \cdot m \cdot t})\right] \quad (48)$$



(1) $V_{hb\_t}(t)$

(2) $I_{fil\_t}(t)$

Fig 22. Half-bridge voltage and filament current as a function of time

7. Abbreviations

Table 2. Abbreviations

Acronym	Description
ACS	Average Current Sensor
CFL	Compact Fluorescent Lamp
CMD	Capacitive Mode Detection
EMI	Electro Magnetic Interference
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
RLC	Resistance, Inductance, Capacitance
SoS	Sum of Squares

8. References

[1] **AN10803 —** Triac dimmable CFL UBA2028/UBA2014

[2] **AN10872 —** TL application with UBA2014 - available on request from your NXP Semiconductors sales person

[3] **Current waveform distortion in power factor correction circuits employing discontinuous mode boost converters —** 1989 IEEE

[4] **UM10409 —** UBA2014 user manual

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10. Figures

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