AN10873

PTN3392 application design reference manual

Rev. 1.1 — 17 November 2016 Application note

Document information

Info	Content
Keywords	PTN3392, DisplayPort, VGA, dongle, display adapter
Abstract	This application note provides information to enable customers to design a full DisplayPort to VGA adapter solution using NXP's PTN3392 DP-VGA adapter IC. The application design guidelines given in this document focus on optimum cost, size and low component count while achieving best interoperability, signal integrity, EMI and RFI as well as compliance to applicable standards. A full PCB design file implementing mentioned guidelines and suitable for use by customers to make a manufacturable dongle is available upon request.

Revision history

Rev	Date	Description
v.1.1	20161117	released to public
v.1	20101220	application note; initial release

Contact information

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1. Introduction

This application note provides information to enable customers to design a full DisplayPort to VGA adapter solution using NXP's PTN3392 DP-VGA adapter IC. The application recommendations given in this document focus on optimum cost, size and low component count and provides critical layout and design guidelines to achieve best interoperability, signal integrity, EMI and RFI as well as compliance to applicable standards.

In addition to this application note, a full documentation package—including a full PCB design file and detailed BOM—is available which implements the mentioned guidelines in an actual dongle reference design. This dongle reference design is suitable for use by customers and can be readily adopted or minimally modified to make a manufacturable DisplayPort to VGA adapter.

There are two reference designs, DPVGA4M and mDPVGA4M. The mini and regular DP versions have no difference in schematics. The only difference is mechanical.

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a. DPVGA4M

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b. mDPVGA4M

Fig 1. Reference designs DPVGA4M and mDPVGA4M

2. Features

The reference design described in this application note, using the highly integrated PTN3392 DisplayPort to VGA adapter IC, features:

- Small size: 1 inch × 1.25 inch PCB dimensions for mDPVGA4M
- Low component count and BOM
- Compliant to: VSIS 1.2; CISPR22B, DisplayPort v1.1a, IEC61000-4-2
- No external ESD components needed
- Low power consumption, powered from the DisplayPort connector
- Support for Flash over AUX for field re-programmability

3. DisplayPort to VGA adapter schematic

This section details the complete schematic design of a full DisplayPort to VGA adapter solution or ‘dongle’.

3.1 Block diagram overview

This section outlines in block diagram the essential components needed to complete a DP-VGA dongle. A simplified block diagram is shown in Figure 2, and a detailed schematic is shown in Figure 5.

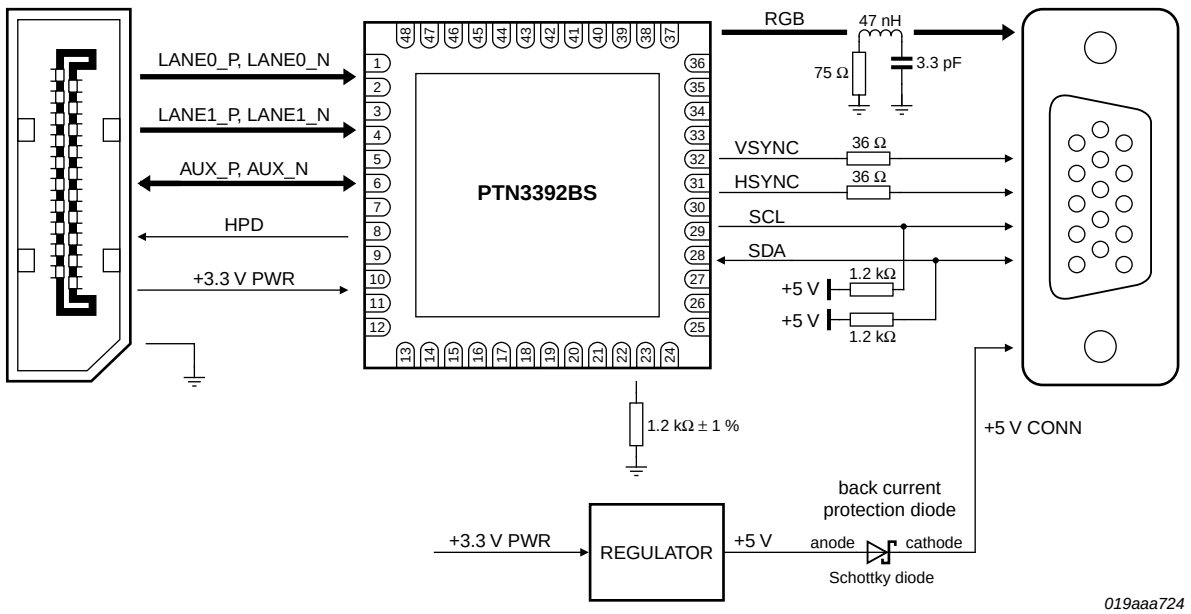


Fig 2. DP-VGA block diagram

3.1.1 DisplayPort connector

Connection to a DisplayPort capable source is provided via either a plug-type DisplayPort connector, or by way of a tethered DisplayPort cable with plug end (also known as ‘pigtail’). The DisplayPort connector encompasses the high-speed serial main link differential signals ML0 and ML1, the AUX (auxiliary) differential pair, an HPD (hardware presence detect or hot-plug detect) single-ended TTL signal, and a 3.3 V power supply DP_PWR. The DisplayPort connector also provides Cable Detect signals to the source to aid the source in correct adapter discovery of DP, HDMI or DVI.

3.1.2 PTN3392 integrated DP to VGA adapter IC

PTN3392 integrates all essential DP to VGA adapter functions in one small IC. This includes a two-lane DisplayPort v1.1a receiver, a high-quality triple VGA video DAC. 1 MHz AUX channel, and Hot Plug Detect (HPD) signal to the source. Supports up to 100 kbit/s I^2C-bus speed, declared in DPCD register.

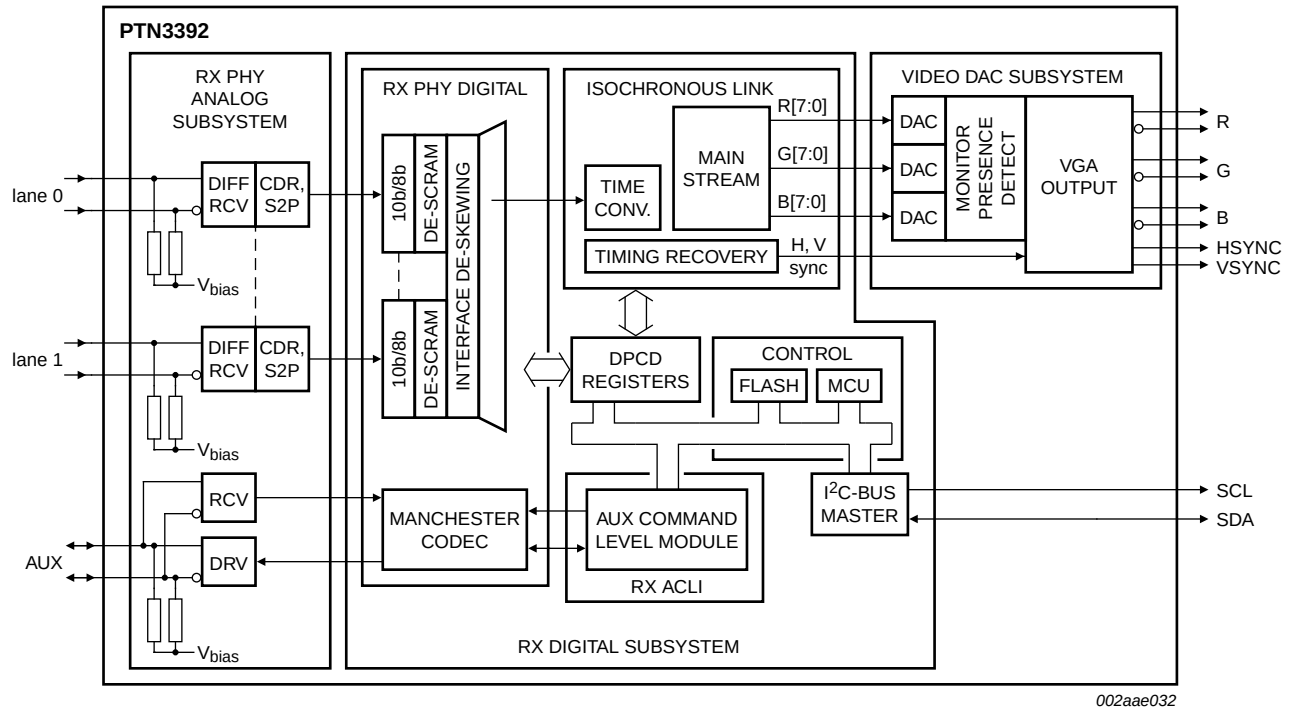


Fig 3. PTN3392 functional block diagram

3.1.3 PTN3392 HVQFN48 package

PTN3392 is packaged in a plastic thermal enhanced thin quad flat package HVQFN48; no leads; 48 terminals; 7 mm × 7 mm × 0.85 mm.

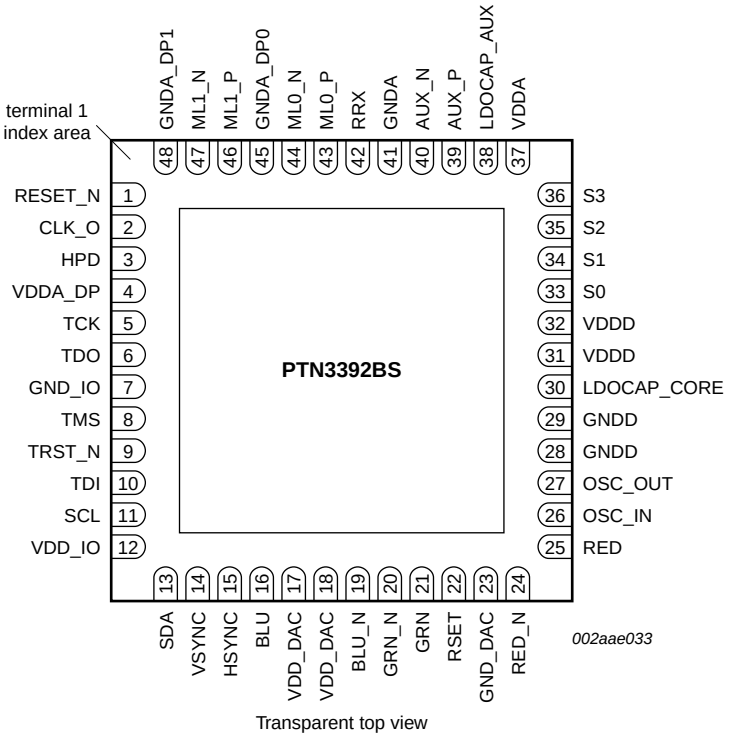


Fig 4. PTN3392 pin configuration for HVQFN48

3.1.4 Power supply to the dongle

The DP_PWR pin of the DisplayPort connector provides all power to the dongle. Nominal voltage is 3.3 V delivered by an active source whenever the dongle is plugged in.

3.1.5 VGA connector

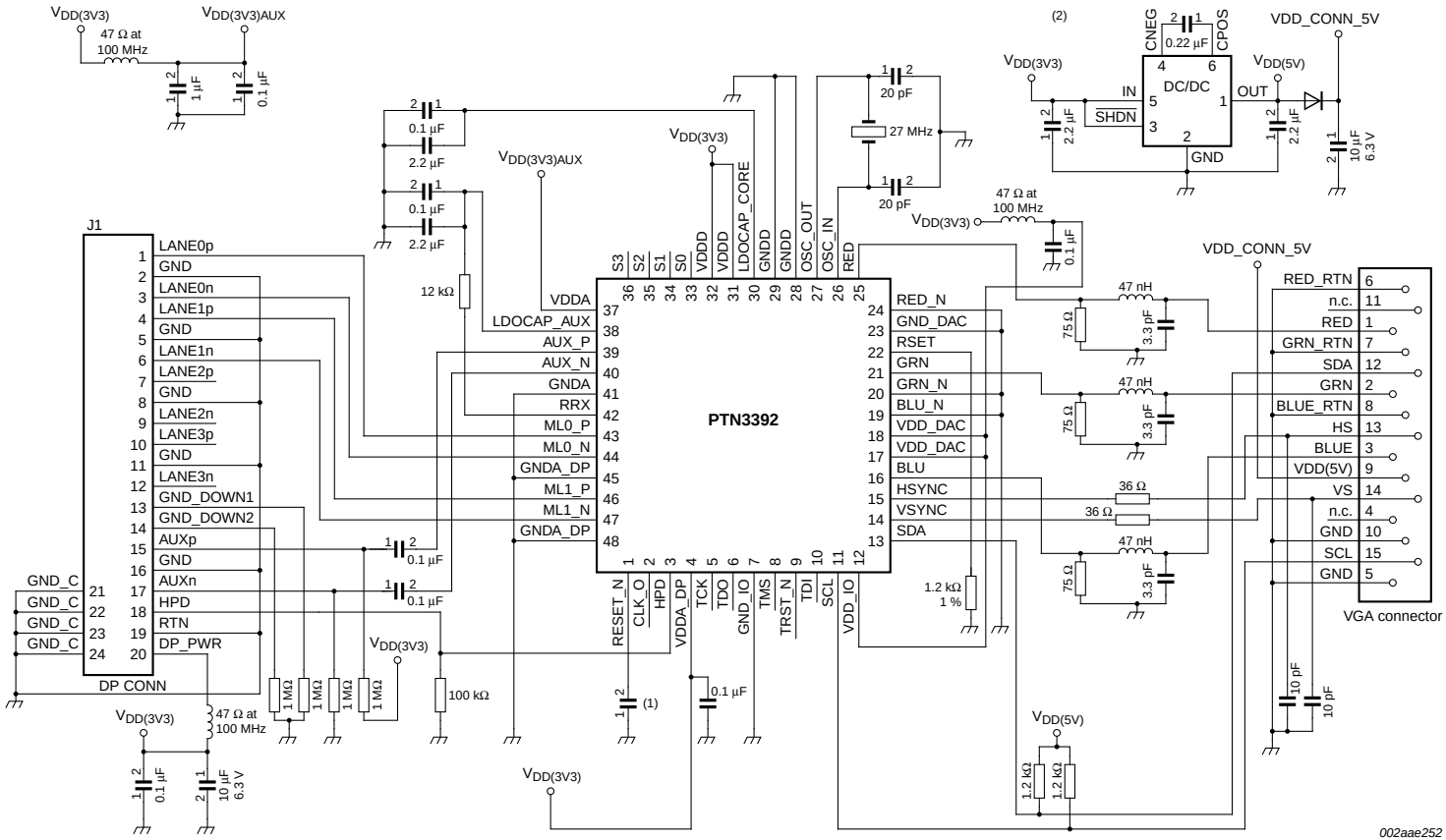
The VGA connector provides the interface to a monitor and attaches to any standard VGA cable. Included in the VGA interface are Red, Green and Blue (RGB) video signals, horizontal (HSYNC) and vertical (VSYNC) synchronization signals, the Direct Display Control (DDC) bus, and a 5 V power supply to power the monitor's EDID and provide for DDC pull-up voltage whenever the monitor is in an unpowered state.

3.1.6 Power supply to the VGA connector

The 5 V power supply to the VGA connector is generated from a regulator on the adapter board, using a filtered 3.3 V as input. It has to be rated for at least 55 mA load current, per VGA specifications.

3.2 Detailed schematic design

DPVGA4M design follows *"VESA DisplayPort Interoperability Guideline Version 1.1a, February 5, 2009"*. This section describes in detail each component subsystem in the DP to VGA adapter reference design.



(1) 1 µF is recommended.

(2) Example of external DC-to-DC regulator.

Fig 5. DPVGA4 schematic

3.2.1 DisplayPort connector

DPVGA4 uses regular 20-pin DP connector that plugs into source-side DP receptacle. This connector is soldered directly on to the PCB. This connector can also be attached to a DP end pigtail cable, cable wires are spread out and solder onto each pin pad.

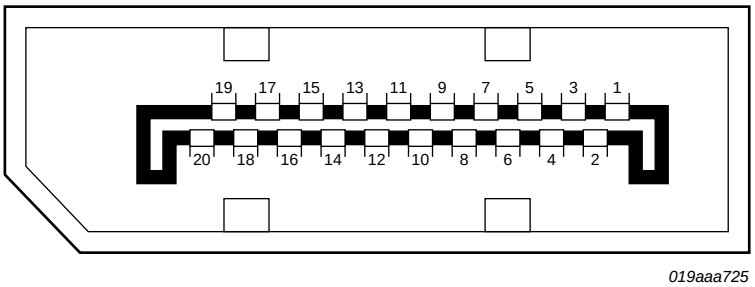


Fig 6. External connector (source-side) on PCB

Table 1. 20-pin DP connector pin list (for source-side connector)

Pin	Symbol	Description
1	ML_Lane 0 (p)	Lane 0 (positive)
2	GND	ground
3	ML_Lane 0 (n)	Lane 0 (negative)
4	ML_Lane 1 (p)	Lane 1 (positive)
5	GND	ground
6	ML_Lane 1 (n)	Lane 1 (negative)
7	ML_Lane 2 (p)	Lane 2 (positive)
8	GND	ground
9	ML_Lane 2 (n)	Lane 2 (negative)
10	ML_Lane 3 (p)	Lane 3 (positive)
11	GND	ground
12	ML_Lane 3 (n)	Lane 3 (negative)
13	CONFIG1	connected to ground[1]
14	CONFIG2	connected to ground[1]
15	AUX CH (p)	Auxiliary Channel (positive)
16	GND	ground
17	AUX CH (n)	Auxiliary Channel (negative)
18	Hot Plug	Hot Plug Detect
19	Return	Return for Power
20	DP_PWR	Power for connector (3.3 V, 500 mA)

[1] Pin 13 and pin 14 may either be directly connected to ground or connected to ground through a pull-down device.

Some laptops use mini-DP connectors to save space.

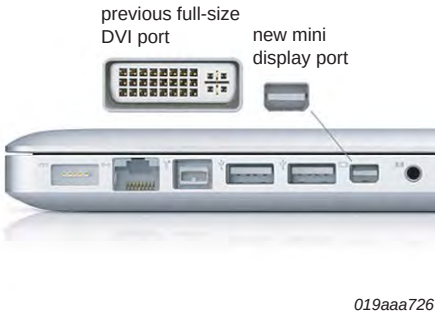


Fig 7. Mini DisplayPort

Table 2. 20-pin mini-DP connector pin list (for source-side connector)

Pin	Symbol	Description
1	GND	ground
2	Hot Plug Detect	Hot Plug Detect
3	ML_Lane 0 (p)	Lane 0 (positive)
4	CONFIG1	CONFIG1
5	ML_Lane 0 (n)	Lane 0 (negative)
6	CONFIG2	CONFIG2
7	GND	ground
8	GND	ground
9	ML_Lane 1 (p)	Lane 1 (positive)
10	ML_Lane 3 (p)	Lane 3 (positive)
11	ML_Lane 1 (n)	Lane 1 (negative)
12	ML_Lane 3 (n)	Lane 3 (negative)
13	GND	ground
14	GND	ground
15	ML_Lane 2 (p)	Lane 2 (positive)
16	AUX CH (p)	Auxiliary Channel (positive)
17	ML_Lane 2 (n)	Lane 2 (negative)
18	AUX CH (n)	Auxiliary Channel (negative)
19	GND	ground
20	DP_PWR	Power for connector

DP to mini-DP adapter is available for interchanging different size DP connectors.

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Fig 8. Mini-DP to DP converter

3.2.2 Power supply

No external power supply is required to power DPVGA dongle.

The DP_PWR pin of the DisplayPort connector provides all power to the dongle. Nominal voltage is 3.3 V delivered by an active source whenever the dongle is plugged in.

A low-pass LC L filter is recommended to remove high frequency components to ensure clean power signal VDD_3V3, and VDD_3V3 power plane.

VDDA_DP, VDD_IO, VDDD1and VDDD2 ties directly to VDD_3V3 plane.

VDD_DAC1 and VDD_DAC2 are used to power video DACs, they require extra clean reference analog power. Separate from VDD_3V3 power tree with an LC filter.

VDDA is a 3.3 V supply voltage to power analog AUX, bias and PLL. Use another LC filter to branch off VDD_3V3 power tree. DPVGA4 power tree example is illustrated in Figure 9.

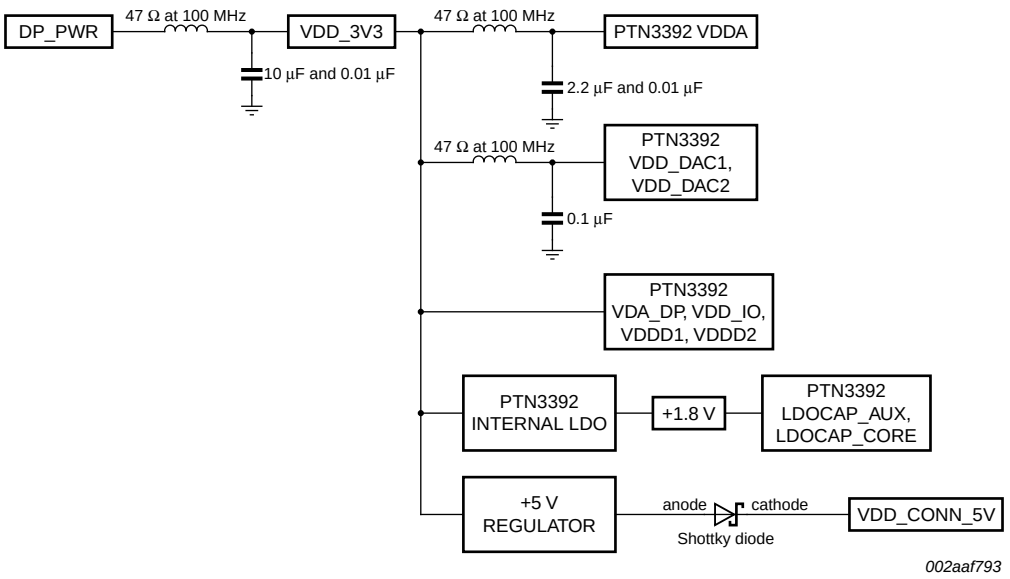


Fig 9. DPVGA4 power tree example

3.2.3 Low EMI emission

Entire DPVGA4M design was simulated in depth (Ref. 3), in the following steps:

1. 3D simulations
   a. Obtain the Transfer function.
   b. Obtain the S11 (S-parameters).
2. Circuit simulations
   a. Insert the S11 information (step 1.b.).
   b. Compute and process the actual signal spectrum.
3. Use Matlab to calculate the actual radiated emission spectrum by multiplying the transfer function (step 1.a.) with the actual signal spectrum (step 2.b.).

Ref. 3 details the simulation results and guidelines for achieving low emissions of the DisplayPort to VGA application.

Pre-Compliance Test was measured following EMC standards and passed.

- CISPR 22: 2005-04; A1: 2005-07; A2: 2006-01
- EN 55022: 2006-09; A1: 2007-10

For information technology equipment, Criterion B is used.

Criterion B states, during application of the transient test, degradation of performance including loss of function is allowed provided that the EUT self-recovers to normal operation after testing without any operator intervention.

"PTN3392 DP-VGA Dongle EMC Test Report" is listed in the reference; it is available upon request.

3.2.4 ESD protection

A crucial element in EMC/ESD immunity is a solid PCB design. Good practices such as decoupling power and I/O lines to ground, voltage and frequency (bandwidth) limiting, wave shaping (edge-rate control), using negative feedback, refresh cycling, WDT, and fault tolerant software—all play collectively an important role in improving EMC and ESD immunity. Refer to Ref. 7 for a guide to designing for ESD.

PTN3392 is designed for 7 kV ESD HBM JEDEC. DPVGA4M with PTN3392 cable adapter has been tested for IEC61000-4-2 ESD stress tests, and passes without external ESD protection devices. Copy of DPVGA4M dongle – IEC testing is listed in Ref. 5 and it is available upon request.

3.2.5 Reset circuitry

No external power-on reset circuitry is needed; this is taken care of automatically by PTN3392. Its RESET_N pin (pin 1) allows for connection of a suitable capacitor to optimally time its internal power-on reset sequence. A capacitor to GND is required, and the recommended value is 1 μF.

3.2.6 Crystal oscillator

The processor is clocked with the on-chip free-running oscillator or from the external 27 MHz crystal oscillator through a PLL. Video clock is generated from the crystal clock and DisplayPort main link with M/N relation transmitted over the link. (The M and N are 24 bit values used for stream clock recovery [Ref. 9].)

External 27 MHz crystal is mainly used for processor and control, the precision of the crystal is not critical, ±50 ppm is good enough.

3.2.7 Bias, reference and tie-off

One external bias resistor to ground is required for video DAC outputs. This resistor sets the reference current which determines the analog output level.

Pin 22 RSET = external bias resistor value

1.2 kΩ ± 1 % is required, because non-linearity increases with larger bias resistors.

Another external 12 kΩ resistor is needed between PTN3392 internal LDOs and BIAS. Connect 12 kΩ resistor to pin 38, LDOCAP_AUX, and pin 42, RRX.

Pin 42 RRX = receiver termination resistance control.

3.2.8 DisplayPort receiver interface

DisplayPort is a digital display interface standard put forth by the Video Electronics Standards Association (VESA) since 2006. There are four differential pairs of data and one differential pair of auxiliary channel for controls. PTN3392 supports either one or two DisplayPort V1.1a lanes.

3.2.8.1 Main Link (ML)

The DisplayPort connector supports 1, 2, or 4 data pairs (lanes) in a Main Link, each with a bit rate of 1.62 Gbit/s or 2.7 Gbit/s, with self-clock and optional audio signals. The video signal path supports 6 to 16 bits per color channel.

The data transmission protocol in DisplayPort is based on micro packets, allowing flexible allocation of available bandwidth, and is extensible for future feature additions. Unlike the separate DVI/HDMI and LVDS standards, DisplayPort supports both external (box-to-box) and internal (laptop LCD panel) display connections, and embeds the clock in the data signal.

Although DisplayPort's signal is not compatible with HDMI or DVI, Dual-mode ports (which are marked with DP++ logo) can use DisplayPort wires to carry HDMI and single-link DVI. Dual-link DVI and analog VGA are supported through powered adapters which perform active conversion.

PTN3392 DPRX-VGA can work with both a pure DisplayPort (DP) source, or a dual-mode DisplayPort (DP++) source. It only supports two-lane DisplayPort. Main links Lane 0 and Lane 1 are used. They are wired directly to corresponding pins on PTN3392.

The PTN3392 supports HBR at 2.7 Gbit/s and RBR at 1.62 Gbit/s per lane.

3.2.8.2 Auxiliary channel (AUX)

A bidirectional half-duplex auxiliary channel carries device management and device control data for the Main Link, such as VESA EDID, MCCS, and DPMS standards.

3.2.9 Hardware Presence Detect (HPD)

The PTN3392 implements two different ways to handle the HPD signal. The HPD behavior is governed by the S0 (pin 33) pin's value after the reset and initialization sequence is completed.

If S0 pin is tied HIGH, HPD is only driven HIGH when a monitor is detected.

If S0 is tied LOW, HPD is driven HIGH irrespective of whether a VGA monitor is detected.

3.2.10 VGA output interface

Figure 10 and Table 3 detail the 15-pin VESA DDC2/E-DDC connector; the diagram's pin numbering is that of a female connector functioning as the graphics adapter output.

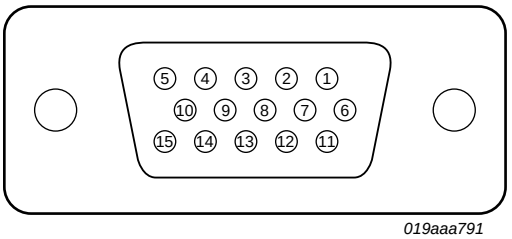


Fig 10. A female DE15 socket (video card side)

Table 3. 15-pin VGA connector pin list

Pin	Symbol	Description
1	RED	red video
2	GREEN	green video
3	BLUE	blue video
4	ID2/RES	formerly Monitor ID bit 2; reserved since E-DDC
5	GND	ground (HSYNC)
6	RED_RTN	red return
7	GREEN_RTN	green return
8	BLUE_RTN	blue return
9	KEY/PWR	formerly key; now +5 V DC
10	GND	ground (VSYNC, DDC)
11	ID0/RES	formerly Monitor ID bit 0; reserved since E-DDC
12	ID1/SDA	formerly Monitor ID bit 1; I^2C-bus data since DDC2
13	HSYNC	horizontal sync
14	VSYNC	vertical sync
15	ID3/SCL	formerly Monitor ID bit 3; I^2C-bus clock since DDC2

3.2.10.1 Red, Green and Blue (RGB) video outputs

The triple 8-bit video DACs output a 700 mV (peak-to-peak) analog video output signal into 37.5 Ω load, as is the case of a doubly terminated 75 Ω cable.

Figure 11 shows an example of VGA dongle application. A 75 Ω termination is used to terminate inside the dongle, and another 75 Ω termination is typically used inside the RGB monitor. The load sensing mechanism assumes this double termination.

The load-sensing circuit is active during the vertical blanking period, so that there will be no disturbance to the screen image caused by the load-sensing circuit.

Please note that because of the wide variety of monitor implementations, this is a best-effort detection method only. It is recommended that the user uses a combination of EDID read from the source and the load-sensing circuit of PTN3392 dongle to decide whether the RGB monitor is connected or not.

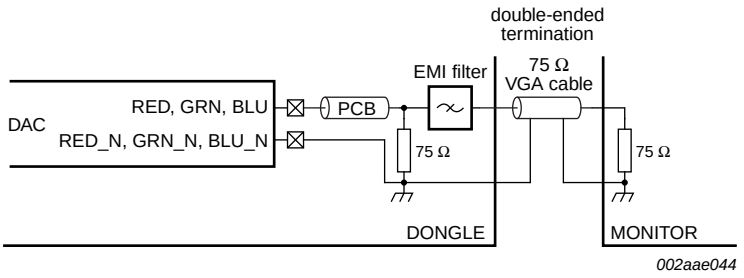


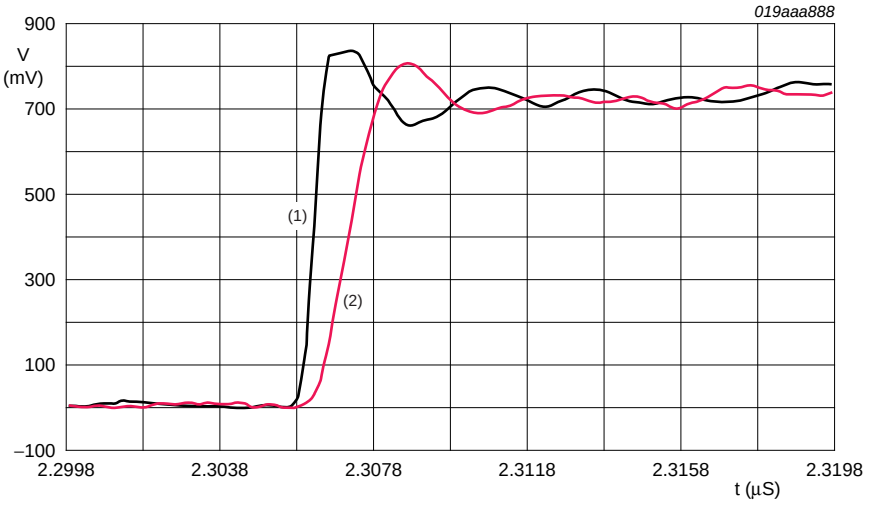
Fig 11. Recommended DAC terminations for PTN3392

Proper RGB filtering gains sufficient EMI margin. Pi (π) filters 0 pF-47 nH-3.3 pF are recommended for RGB outputs to reduce overshoot value, settling time and better rise time. Passing VSIS (Video SIgnal Standard) test is essential for commercial electronics.

The following two waveforms illustrate the rise and fall times are failing on the RGB outputs with 3.3 pF-68 nH-3.3 pF Pi filters. The 1920 × 1200 rise and fall time limits are 1.294 ns. The DPVGA4M dongles are failing by 100 ps to 200 ps. Rise and fall times are slightly different from each other.

The traces marked “(1)” show the rise/fall edges directly at the output of the DAC, before Pi filter. The traces marked “(2)” show the rise/fall edges after the Pi filter. The overshoots have been improved, but the rise/fall time increased slightly, that fail VSIS test.

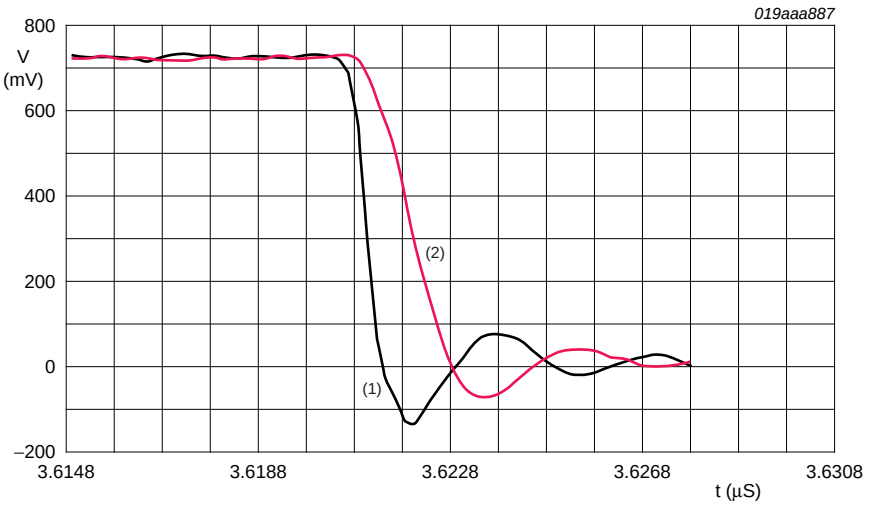
Further simulation based on the existent schematic configuration, including the 75 Ω parallel termination, the recommended Pi filter configuration is 0 pF-47 nH-3.3 pF for RGB output. VSIS tests confirm with passing results.



(1) Rising edge at output of DAC, before Pi filter.

(2) Rising edge after Pi filter.

a. Pi filter rising edge

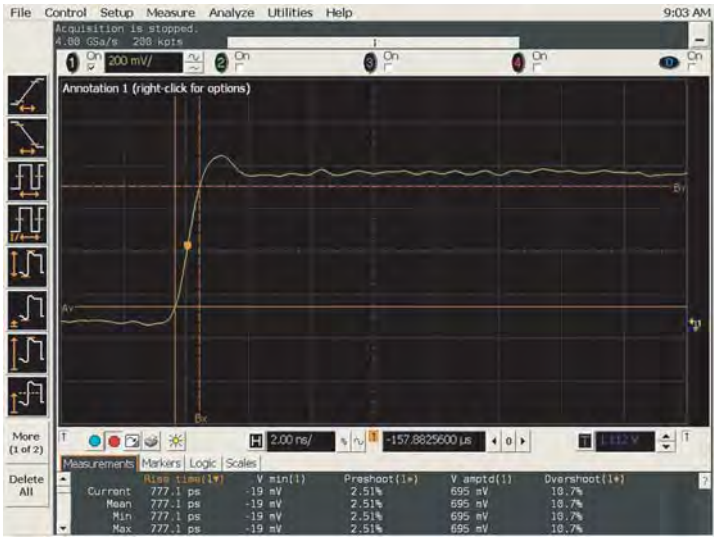


(1) Falling edge at output of DAC, before Pi filter.

(2) Falling edge after Pi filter.

b. Pi filter falling edge

Fig 12. Failing Pi filter rising/falling edges



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a. Pi filter rising edge

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b. Pi filter falling edge

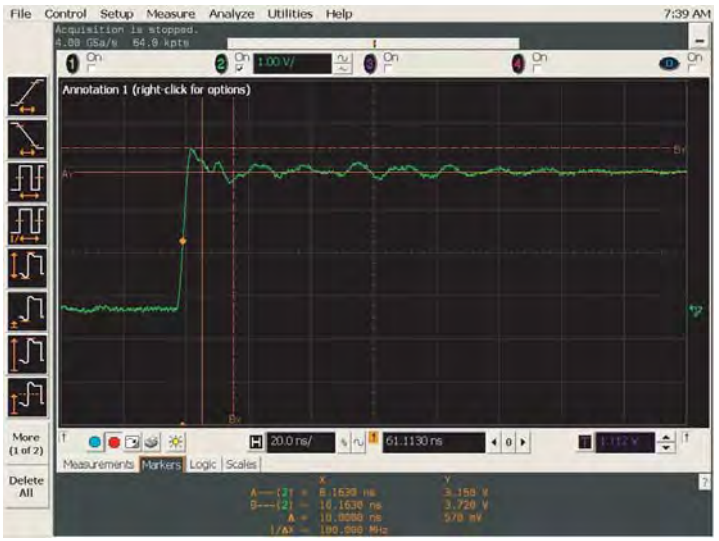
Fig 13. Passing Pi filter rising/falling edges

3.2.10.2 Video synchronization outputs (HSYNC and VSYNC)

The PTN3392 generates the RGB video timing and synchronization signals. The Sync outputs, HSYNC and VSYNC are defined by the VESA VSIS specification as having 2.2 kΩ pull-down resistors within the display. This is not guaranteed, however. Some older monitors may not have any pull-down resistors, and some may even have pull-up resistors. But most modern displays should have around the 2 kΩ pull-down.

Both the polarity and timing of HSYNC and VSYNC are controlled by DisplayPort Main Stream Attributes package.

HSYNC and VSYNC strength are programmable inside PTN3392, they are default to highest setting (111) during initialization. 36 Ω load resistors are recommended to reduce overshoot and undershoot of these two signals.



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a. HSYNC overshoot

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b. HSYNC undershoot

Fig 14. HSYNC overshoot, undershoot

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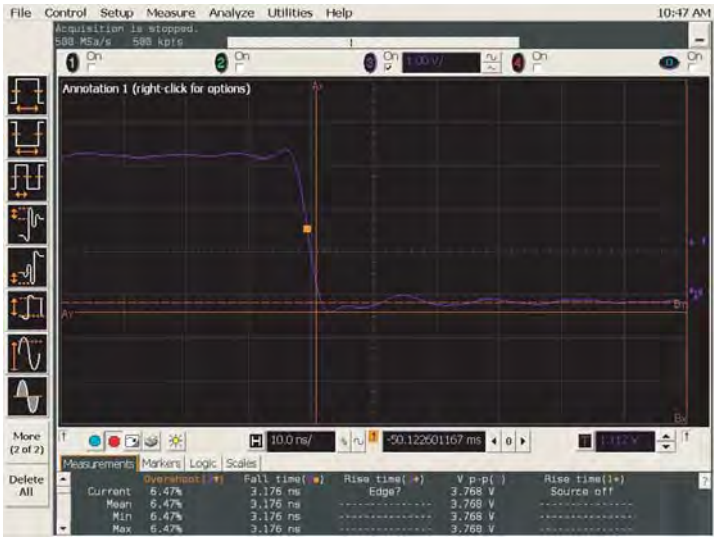
a. VSYNC overshoot



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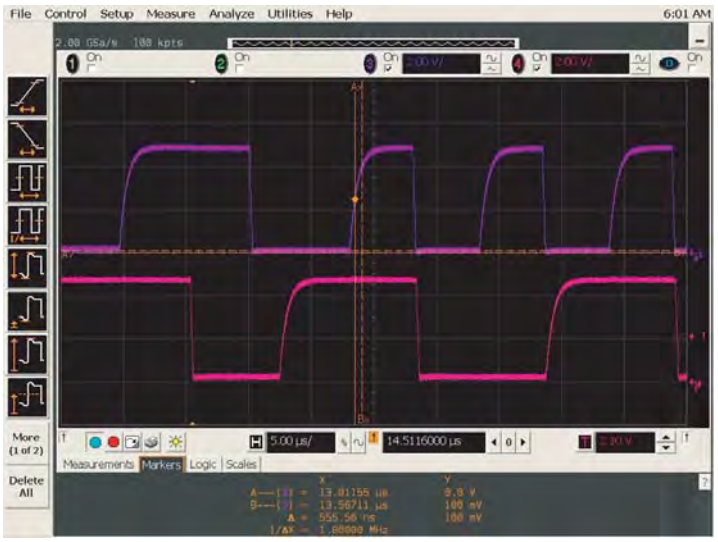
b. VSYNC undershoot

Fig 15. VSYNC overshoot, undershoot

3.2.10.3 Direct Display Control (DDC)

The DDC bus is simply an I^2C-bus. The I^2C-bus standard does not define any protocol above the physical layer. The DDC standard, however, defines a small amount of protocol over the I^2C-bus standard to facilitate accessing the E-EDID memory. The earlier revision of the EDID memory only allowed a single 256-byte block of data. The current revision of the E-EDID standard allow for the EDID to contain up to 32 kBytes of data, partitioned into 256-byte blocks.

Typical VGA cables range from 6 feet to 15 feet, 4.7 kΩ pull-up to 5 V on SCL and SDA lines are suitable. Some applications, such as projector, require cable as long as 100 feet, clock signal badly distorts with 4.7 kΩ pull-ups. Change the pull-ups to 1.2 kΩ to restore the clock to normal pulse. Lab tests show the DP source can still read the sink EDID with 115 feet long VGA cable via DPVGA4M cable adapter.



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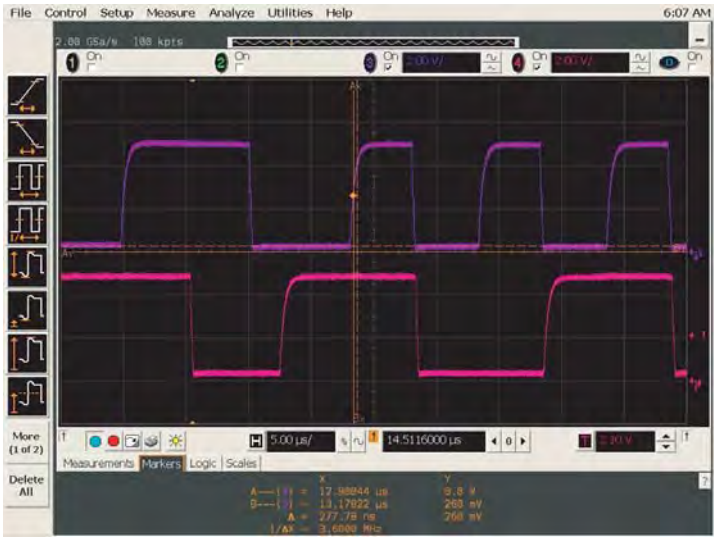
a. 2.2 kΩ pull-up



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b. 1.2 kΩ pull-up

Fig 16. I^2C-bus SCL, SDA with 2.2 kΩ pull-up and 1.2 kΩ pull-up

3.2.11 5 V regulator

The DDC standard defines the DDC +5 V reference that must be delivered to the monitor. The definition states +5 V (± 5 %) with a 50 mA capability and over current protection limiting the maximum current to no more than 1 A.

One 60 mA switched-CAP buck/boost charge pump converter is used on DPVGA4M and mDPVGA4M boards to boost +3.3 V to +5 V for monitor EDID memory read and to pull up SCL and SDA lines.

The charge pump converter produces a regulated, low-ripple output voltage from an unregulated input voltage.

One Schottky barrier diode BAT54 is recommended for back-current protection. The voltage drop across this diode is 0.3 V instead of 0.7 V as other silicon diode, hence does not drop the 5 V output to below its minimum (−5 %) requirement.

4. Layout and design for optimum performance and EMI

This section contains layout and design recommendations that are essential to achieving signal integrity and compliance, good interoperability, and good characteristics for electromagnetic interference (EMI) emission and low EMI susceptibility. Layout and design considerations are discussed per sub-circuit or major interface for clarity.

4.1 Reference plane partitioning and overall supply and grounding

DPVGA4M or mDPVGA4M is a 4-layer, 62 mil ± 10 % thickness, impedance matched PCB. Single-end 59 Ω, differential pair 103 Ω.

Layer 1 — Top signal layer, some ground islands for PTN3392 center pad, between RGB traces and around VGA connector.

Layer 2 — Solid ground plane.

Layer 3 — Split power plane for VDD_3V3 and VDD_5V. Two ground islands for DP traces layout.

Layer 4 — Bottom signal layer. Ground island around VGA connector.

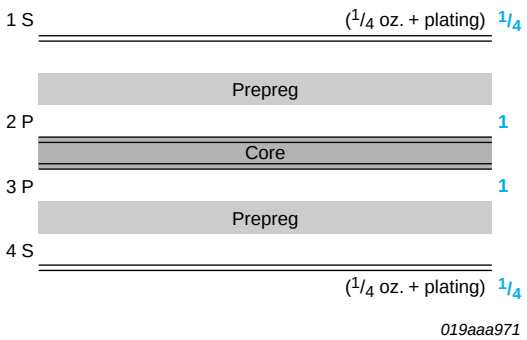

Fig 17. DPVGA4M PCB stack-up

Table 4. DPVGA4M PCB stack-up

	Est. thick.	Single-ended model				Differential model									
		Original L/W	Modified L/W	Reference plane	Calculated impedance	Original L/W	Original space	Modified L/W	Modified space	Reference plane	Calculated impedance				
	1.60	4	4	2	59	5	10	5	10	2	103				
	4.00														
	1.20														
	47.00														
	1.20														
	4.00														
	1.60	4	4	3	59	5	10	5	10	3	103				
Thickness after plating	60.60	not including solder mask			Units			Mils							
Target thickness	62 ± 10 %	over all			Impedance tolerance (SE) ± 10 %				(differential) ± 10 %						

4.2 Power supply filtering and bypass

The main power of DPVGA4 is 3.3 V. Core voltage 1.8 V is generated from internal LDOs, 5 V is boosted with external voltage regulator.

A low ESR (<500 mΩ) 2.2 μF and a 10 nF are recommended for the core voltage and AUX channel voltage. These capacitors should be placed close to these pins, especially the 10 nF.

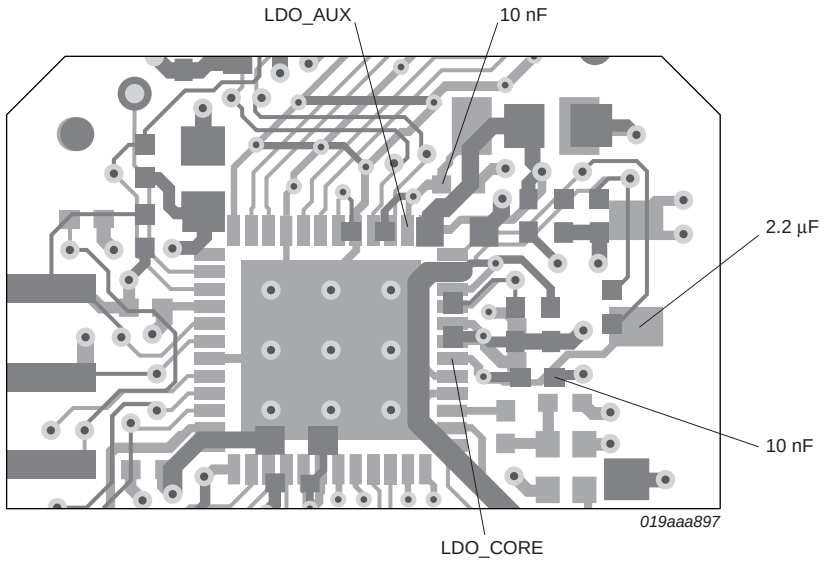

Fig 18. Core and AUX LDO filtering

Use only X5R or X7R type decoupling capacitors, not to use Z5U OR Y5U types. Z5U or Y5U will lose 20 % to 30 % of its capacitance value at high temperature.

Also use 10 nF (103 pF) to help suppress high frequency noise.

Bypass capacitor on 3.3 V power supply pin should be connected to the pin with a wide trace.

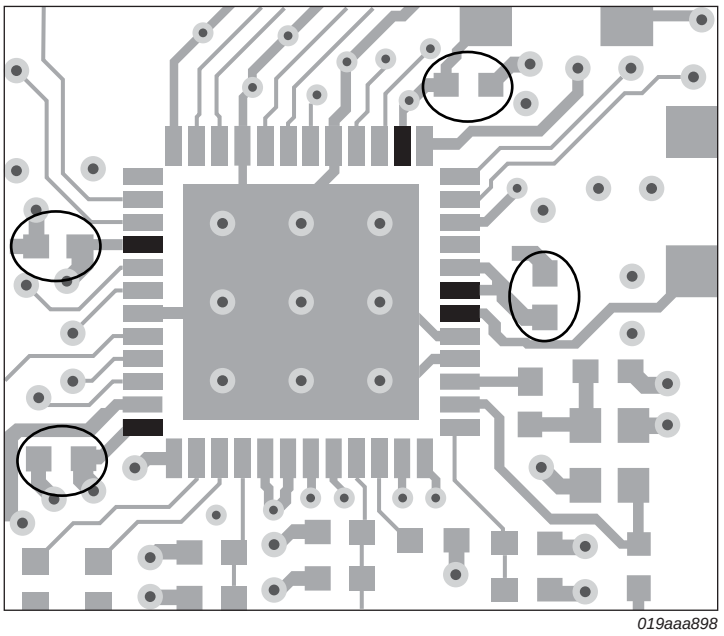

Fig 19. Power supply filtering and bypass layout example

The PTN3392 exposed center pad should be connected to the ground plane as shown in Figure 20.

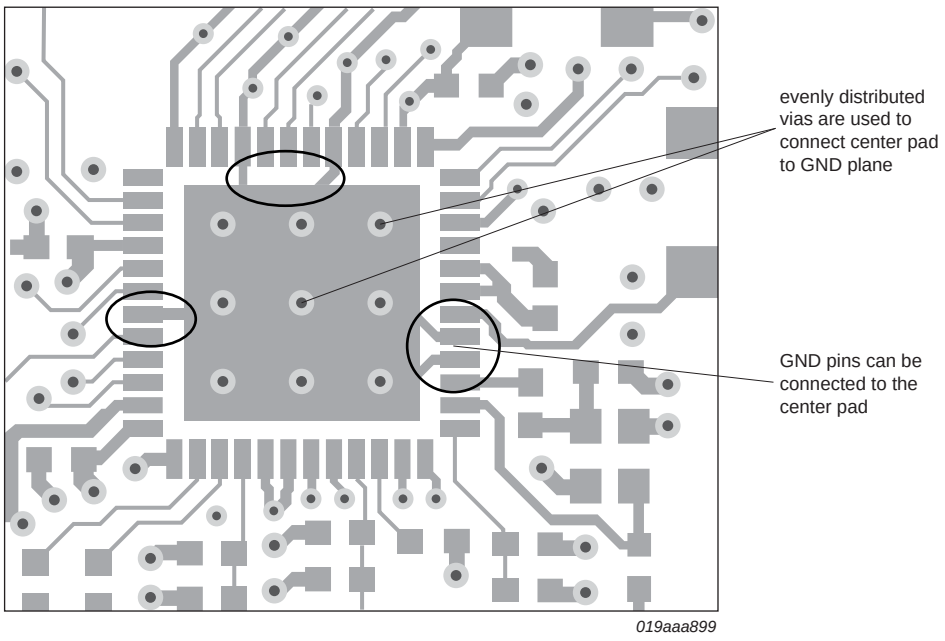

Fig 20. PTN3392 center pad connection

4.3 5 V voltage regulator filtering and bypass

Follow Charge Pump Converter application note to add 2.2 μF for C_{IN} and C_{OUT}, and 0.22 μF for C_{PUMP}.

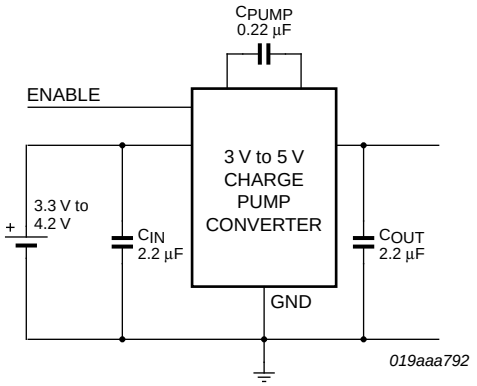

Fig 21. Charge pump converter application

Due to high switch frequency noise, a 10 nF capacitor must be placed at the 5 V output. See schematic detail on Figure 5.

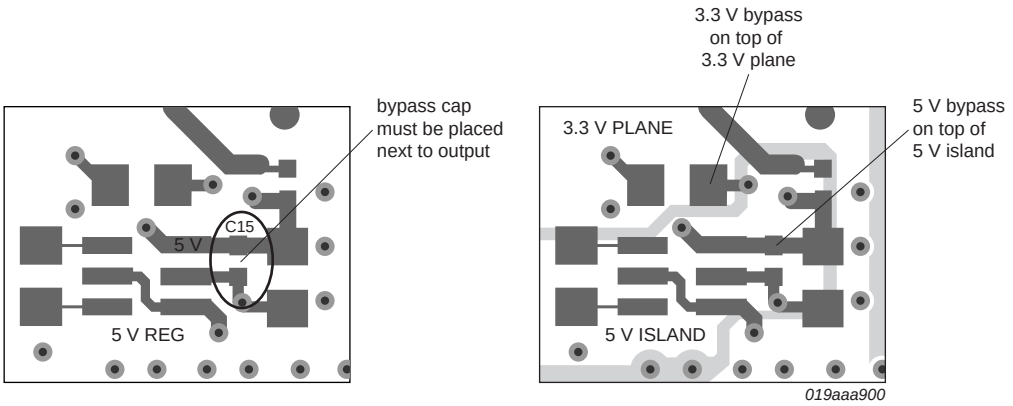

Fig 22. Place 10 nF capacitor next to 5 V output pin

4.4 Crystal oscillator and filter components

A 27 MHz crystal is used to feed the crystal oscillator inside PTN3392. It is connected between OSC_IN and OSC_OUT pins. Depending on the crystal selection, load capacitance varies. Add one 150 Ω series resistor to reduce EMI and crystal's current drive.

Place output capacitor C38 close to OSC_OUT pin; also place oscillator as far away from PCB edge as possible.

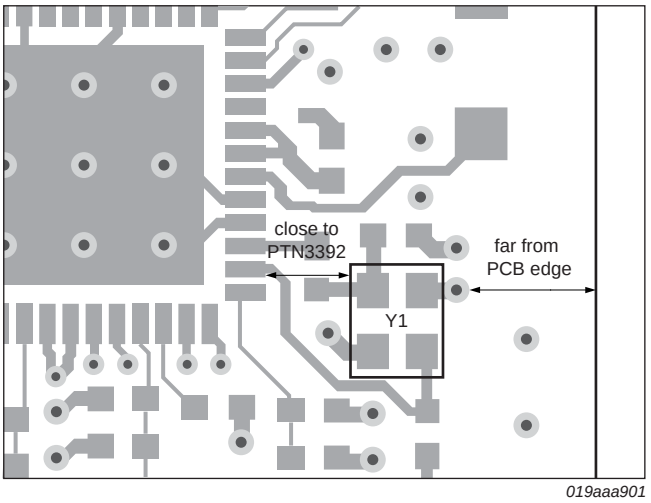

Fig 23. Crystal oscillator and capacitors placement example

4.5 DisplayPort receiver interface

Main differential pairs and AUX channel are routed with 100 Ω impedance. The important parameters to calculate the impedance are:

- PCB thickness
- Distance to ground plane
- Trace width
- Trace spacing
- PCB permittivity

Guard grounds are used to isolate the pair. This helps to eliminate crosstalk between traces. Trace lengths are matched on the same pair.

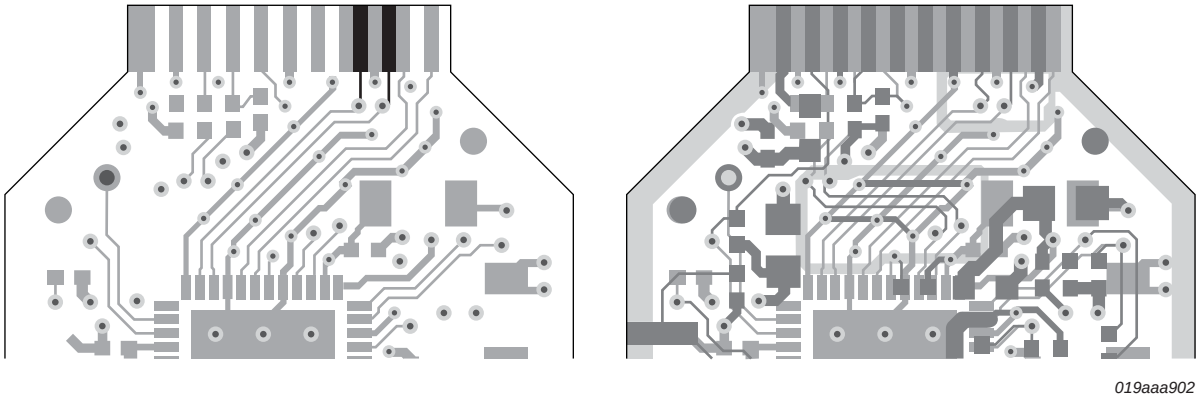

Fig 24. Main video Lane 0, 1 layout example

C18, C19 for AUX pair should be placed close to the DP plug next to pin 15 and pin 17.

When signals change plane, the ground plane needs to move along to keep constant trace impedance. On DPVGA, a ground island is inserted on the V_{CC} plane for this purpose.

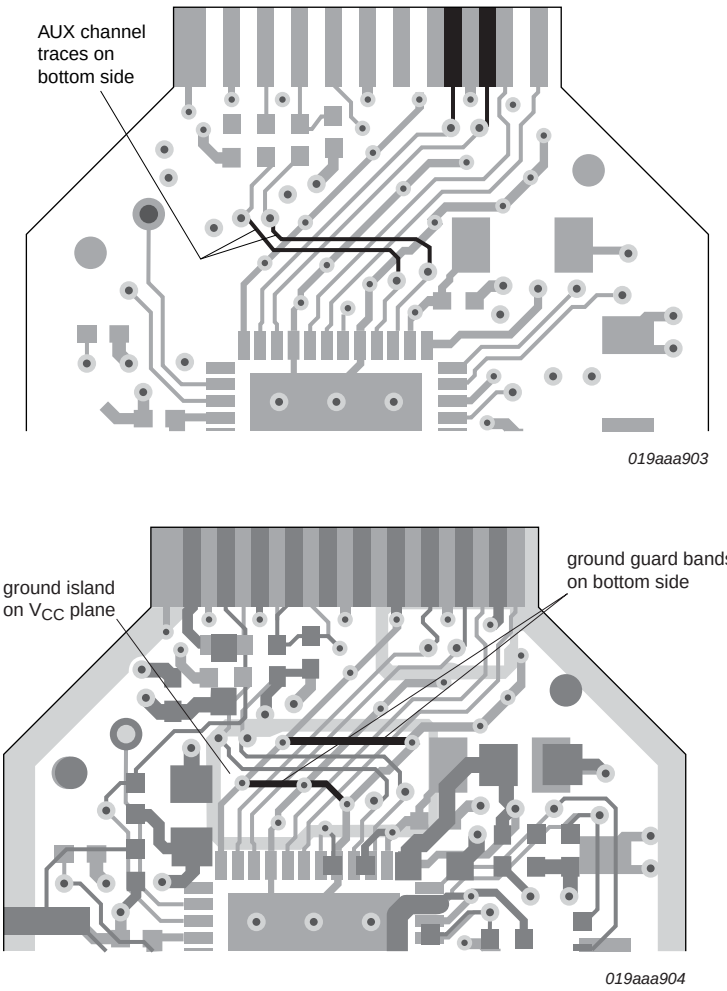

Fig 25. AUX channel layout

Ground pads of the DP plug footprint should be connected directly to ground plane with short traces.

4.6 VGA interface

The following six design guidelines are recommended, and their approximated impacts on the EMI level are listed in Table 5.

Table 5. Design guidelines for VGA connector, PWB to cable junction

Design guideline number	Design guideline description	Approximate impact on EMI decrease
1	Define the second PWB layer as ground plane.	
2	Connect the ground chassis pins of the VGA PWB-connector.	25 dB
3	Use an upper ground plane around VGA connector pins. This design guideline makes no sense when it is not combined with design guideline 4.	
4	Use enough vias to connect the upper ground plane with main ground plane in second PWB layer. Enough means around every 3 mm (stitching).	20 dB
5	Ensure proper connection between PWB-connector chassis and upper ground plane by using contact springs (at least 3 contact points). Emission improvement when either 1 or 3 contacts were used was 10 dB.	10 dB
6	Apply ferrite bead around VGA cable (is already very common for typical cables available from the market)	3 dB

Following the recommended guidelines, all RGB traces on DPVGA4M board are routed with 75 Ω impedance from PTN3392 to VGA connector. Ground fills are used to isolate these traces. Ground fills are connected to ground plane with vias.

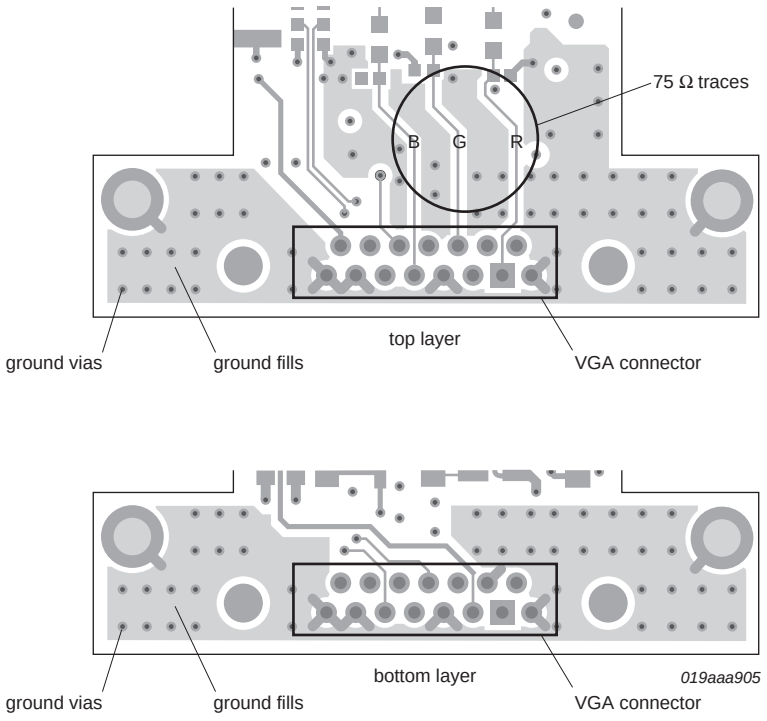

Fig 26. VGA interface layout

Video filter components should be placed symmetrically to optimize for high frequency behavior. Ground terminals should be connected to the ground plane directly with very short traces.

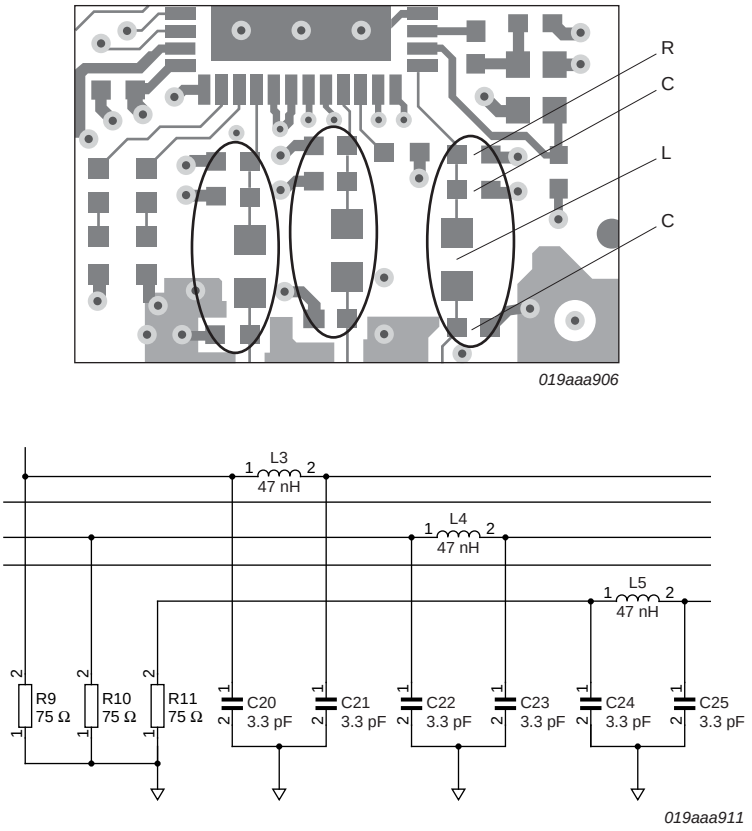

Fig 27. Video filters layout

RGB_N pins on PTN3392 pin 24, pin 20, and pin 19 should be connected directly to ground plane, no via sharing. RSET R8 resistor should be placed close to pin 22, and connect the ground terminal directly to ground plane.

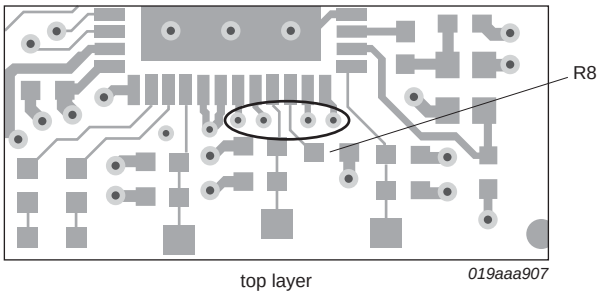

Fig 28. DAC output and current set layout

4.7 General high-speed board design guidelines

DisplayPort requires no new PCB technology. Generally PC system boards are designed with 4-layer FR4 stack-up, with 1080 pre-preg and 47 mil core, and a 0.059-inch nominal thickness.

To minimize loss and jitter, the most important considerations are to design to a target impedance and to keep tolerances small.

A signal pair should avoid discontinuities in the reference plane, such as splits and voids. When a signal changes layers, the ground stitching vias should be placed close to the signal vias. A minimum of 1 to 3 stitching vias per pair of signals is recommended. Never route a trace so that it straddles a plane split. For detail, please refer to *AN10798, "DisplayPort PCB layout guidelines"* (Ref. 6).

5. Abbreviations

Table 6. Abbreviations

Acronym	Description
BOM	Bill Of Materials
DAC	Digital-to-Analog Converter
DDC	Direct Display Control
DP	DisplayPort
DPMS	Display Power Management Signalling (VESA)
DVI	Digital Visual Interface
EDID	Extended Display Identification Data
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
ESR	Equivalent Series Resistance
EUT	Equipment Under Test
HBR	High Bit Rate
HDMI	High Definition Media Interface
HPD	Hardware Presence Detect
HPD	Hot Plug Detect
I^2C-bus	Inter-Integrated Circuit bus
IC	Integrated Circuit
LCD	Liquid Crystal Display
LDO	Low-DropOut regulator
LVDS	Low-Voltage Differential Signalling
MCCS	Monitor Control Command Set (VESA)
PC	Personal Computer
PCB	Printed-Circuit Board
PLL	Phase-Locked Loop
PWB	Printed Wiring Board
RBR	Reduced Bit Rate

Table 6. Abbreviations *...continued*

Acronym	Description
RFI	Radio Frequency Interference
TTL	Transistor-Transistor Logic
VESA	Video Electronics Standards Association
VGA	Video Graphics Array
VSIS	Video SIgnal Standard

6. References

[1] **DisplayPort Interoperability Guideline —** V1_1a, VESA; February 5, 2009

[2] **DisplayPort Interoperability Guideline Adaptor Checklist —** V1, VESA; September 30, 2009

[3] **Guidelines for achieving low emissions (EMI) of the DisplayPort to VGA application —** V1.6; Dr. Nico van Dijk; 1 January 2009

[4] **EMC-10-TRP-2783-401, DP2VGA_Dongle Report —** July 06, 2010

[5] **DPVGA4 IEC Test Summary Report —** Rev 2; April 26 2010

[6] **AN10798, “DisplayPort PCB layout guidelines” —** application note; NXP Semiconductors; www.nxp.com/documents/application_note/AN10798.pdf

[7] **AN10897, “A guide to designing for ESD and EMC” —** Application note; NXP Semiconductors; www.nxp.com/documents/application_note/AN10897.pdf

[8] **PTN3392, 2-lane DisplayPort to VGA adapter IC —** data sheet; NXP Semiconductors; www.nxp.com/documents/data_sheet/PTN3392.pdf

[9] **VESA DisplayPort Standard —** V1.1a, January 11, 2008

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