AN10704

UJA1023 LIN I/O slave with automatic bit rate detection

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founded by Philips

Revision history

Rev	Date	Description
01	20090406	Initial release

Contact information

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AN10704_1

Application note **Rev. 01 — 6 April 2009** **2 of 36**

1. Introduction

The Local Interconnect Network (LIN) is a low-speed, maximum 20 kbit/s, Class-A, serial bus protocol for automotive applications. A LIN sub-bus is primarily intended for modules such as steering wheels, seats, doors, roof and switch panels. Its task is to connect switches, actuators, and sensors into a sub-bus that links to the main bus (e.g. a CAN bus).

The LIN protocol is based on the UART / SCI serial data link format using 8N1-coded byte fields. A LIN network consists of one master node and one or more slave nodes. The medium access is controlled by the master node. An example of a single-master / multiple-slave concept is shown in Figure 1.

The LIN physical layer is derived from the ISO 9141 (see Ref. 3) standard, but contains enhancements designed to meet the particular operational requirements found in an automotive environment, in terns of EMC, ESD, etc. The LIN bus is a single-wire, wired AND bus with a 12 V battery-related recessive level.
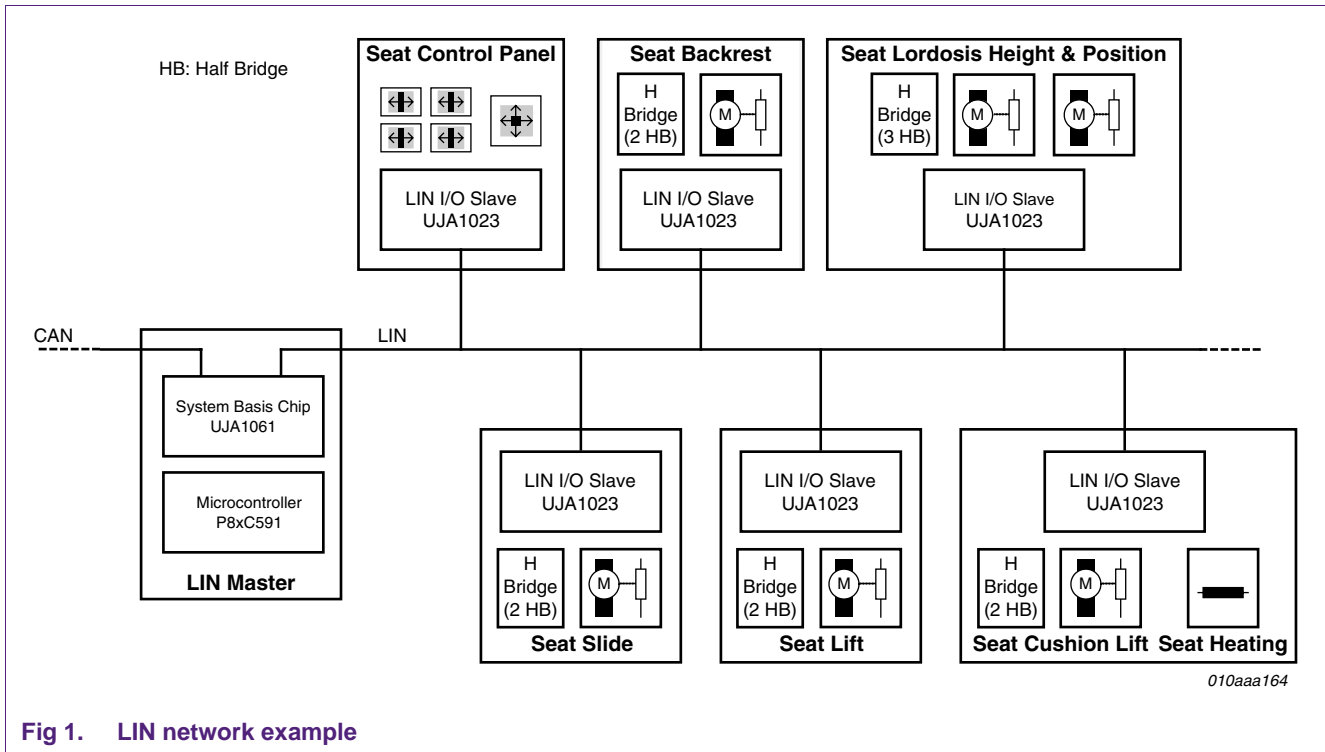

Fig 1.   LIN network example

The LIN I/O slave UJA1023 was developed to provide a fully integrated LIN slave for common automotive input and output applications. It is suitable for applications such as switch panels, driving TOPFETs, reading analog signals or forming an interface to a microcontroller as part of a stand-alone LIN controller. Figure 1 illustrates application examples using the LIN I/O slave UJA1023.

Fig 2. Block diagram
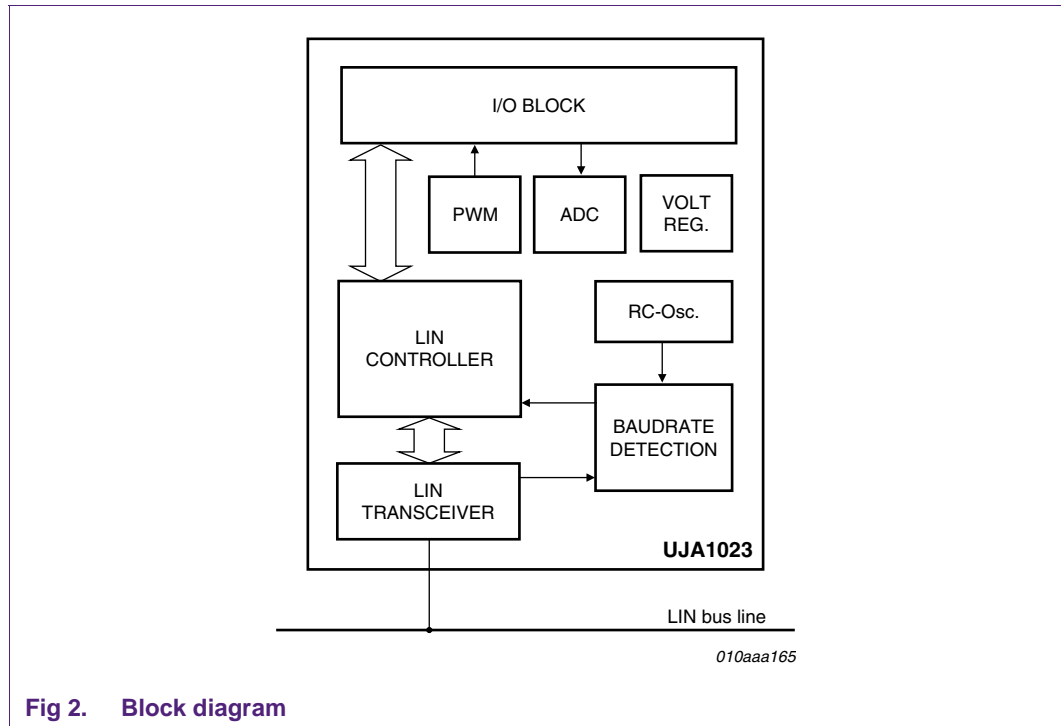
This application note describes the technical implementation of the UJA1023 (see Ref. 1) as a LIN slave within a LIN network. Its focus is to provide application recommendations for the design of LIN Electronic Control Units (ECUs) using the LIN I/O slave UJA1023 from NXP Semiconductors, see Figure 2.

2. Hardware design

2.1 Switch applications

The I/O-pins of the UJA1023 can be used in switch applications in a variety of ways. Switch application can be implemented in two ways:

- Local switch applications, in which the UJA1023 and its switches use the same ground/battery path.
- Remote switch applications, in which the UJA1023 and its switches use separate ground/battery paths.

2.1.1 Local switch applications

A local switch application is an operation where the battery or ground path of the switches uses the same path as the UJA1023. This is typically the case when the UJA1023 and the switches are on the same PCB.

2.1.1.1 Switch to ground

The majority of switch applications are switches or buttons, which are connected to ground. When the switches and the UJA1023 share the same ground path, the switches can be connected directly to the I/O pins of the UJA1023 (see Figure 3 and Figure 4).

Typically, the pull-up current $I_{sc(HS)}$ (see Ref. 1) of the internal HIGH-side transistor is sufficient for the switches (see Figure 3). If a higher pull-up current is needed, an external pull-up resistor R_{pu} can be added (see Figure 4). The reference voltage, V_{ref}, of the internal HIGH-side transistor is the applied voltage on pin VIO. So the external pull-up resistor should also be connected to VIO.
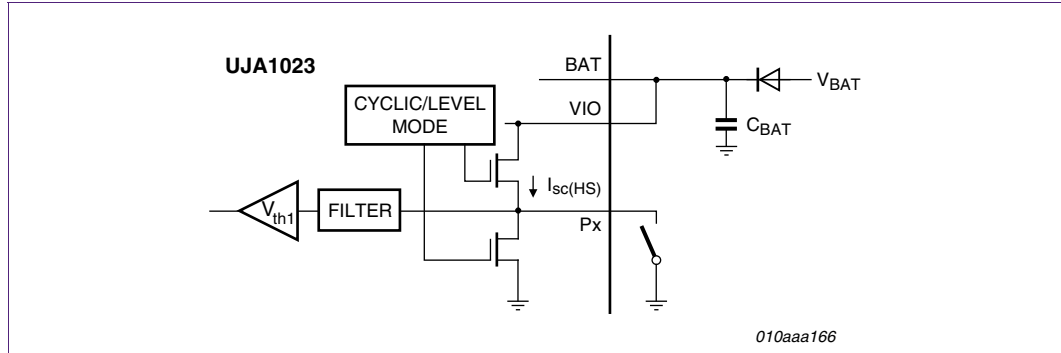

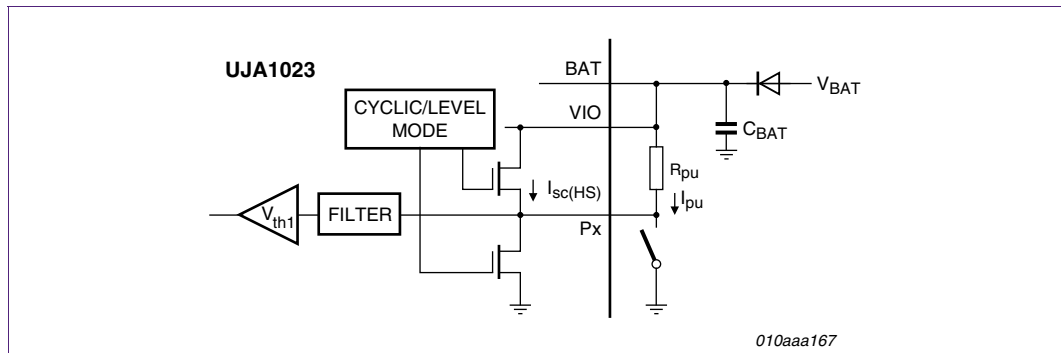**Fig 3.   Local switch to ground - internal HIGH-side switch as pull-up**

Fig 4.   Local switch to ground - external pull-up

The current, I_S, through a closed switch is:

$$I_{S(level)} = I_{sc(HS)}$$ for the applications in Figure 3 and Figure 4,

$$I_{S(cyclic)} = I_{sc(HS)} \times \frac{t_{on(PxOut)}}{T_{cy}}$$ for the application in Figure 3 and

$$I_S = I_{sc(HS)} + I_{pu} = I_{sc(HS)} + \frac{V_{ref}}{R_{pu}}$$ for the application in Figure 4

where:

$I_{sc(HC)}$ is the HIGH-side short circuit current (see Ref. 1)

$t_{on(PxOut)}$ is the Px output turn on time (see Ref. 1)

T_{cy} is the cycle period time (see Ref. 1)

V_{ref} is the reference voltage applied on VIO

R_{pu} is the external switch pull-up resistor.

The UJA1023 provides three input thresholds. For switch applications, it is recommended to use the input threshold V_{th1} (see Ref. 1). For small signal inputs with a voltage reference between 3 V and 5 V it is recommended to use the input threshold V_{th2} (see Ref. 1). For switch diagnosis it is recommended to use the input threshold V_{th3} (see Ref. 1). The input threshold V_{th3} (unlike V_{th1}) is battery-related, which enables it to detect if a switch with a parallel diagnosis resistor R_D is connected to the I/O pin Px of the UJA1023 as shown in Figure 5. Table 1 lists the diagnostic states for V_{th1} and V_{th3} for the circuit shown in Figure 5.

Table 1. Switch diagnosis

V_{th1}	V_{th3}	Diagnosis
HIGH	HIGH	open I/O pin
HIGH	LOW	switch is connected to I/O pin
LOW	LOW	switch is closed
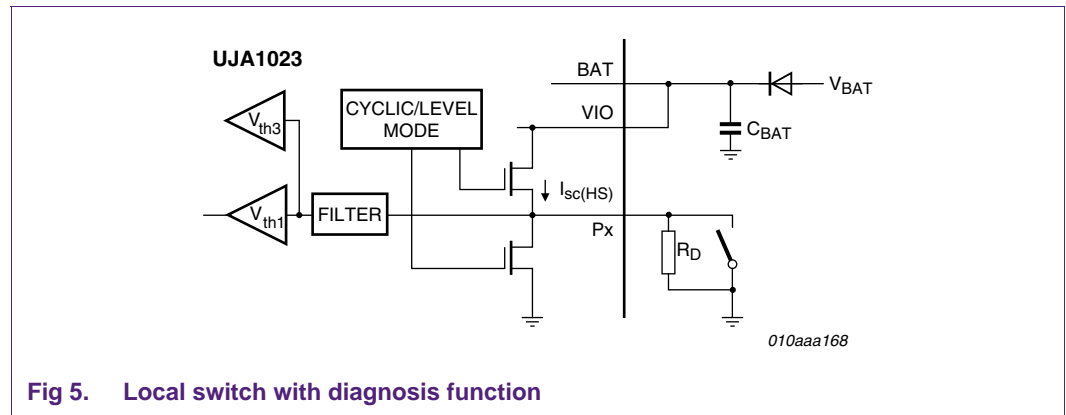
Fig 5.   Local switch with diagnosis function

The diagnosis resistor R_D has a value of 2.8 kΩ ($\pm$ 1 %).

2.1.1.2 Switch to battery

Switches are connected to the battery in some applications. Figure 6 and Figure 7 show typical applications with a local switch to battery where the switch and the UJA1023 share the same battery path. In the configuration illustrated in Figure 6, the cyclic sense output mode is configured so that the internal LOW-side transistor of the UJA1023 is used as a pull-down. The switch current is defined by the pull-down current $I_{sc(LS)}$ (see Ref. 1) of the internal LOW-side transistor.
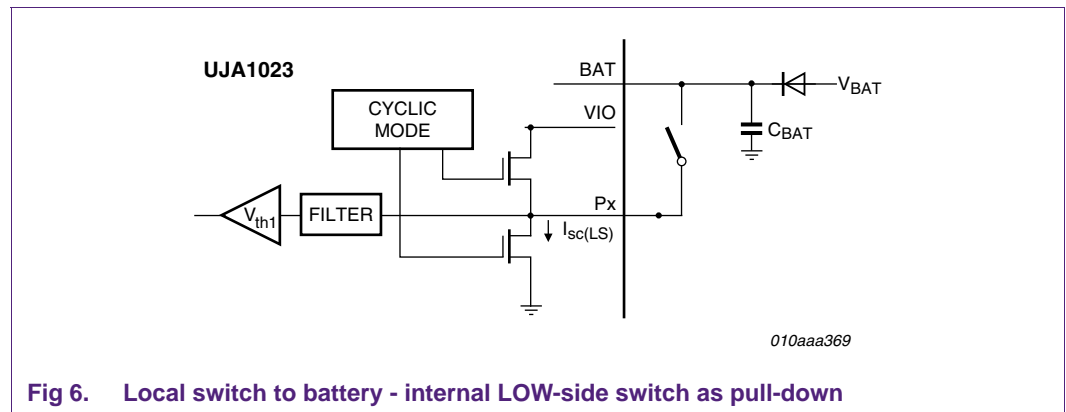
Fig 6.   Local switch to battery - internal LOW-side switch as pull-down
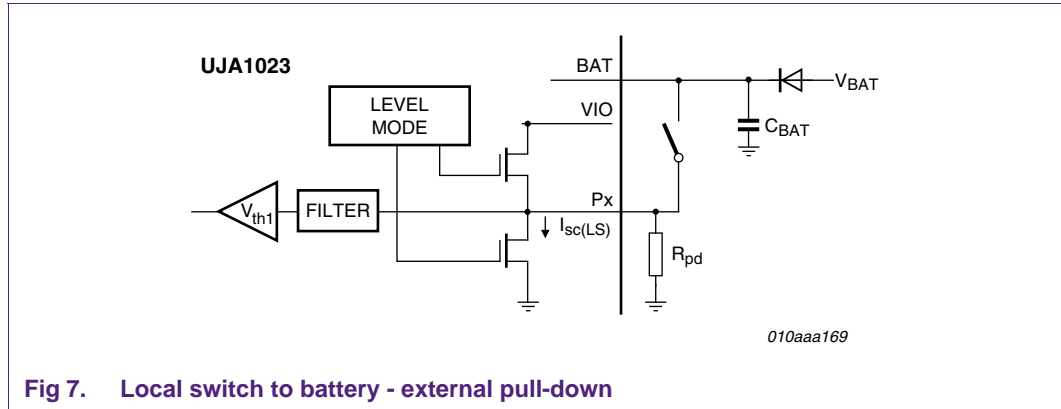
Fig 7.   Local switch to battery - external pull-down

In level mode the internal LOW-side transistor should not be used as the switch pull-down because the power dissipation of the transistor would be too high. In this situation, an external pull-down resistor R_{pd} is recommended (see Figure 7). The value of R_{pd} depends on the switch requirements.

The current I_S through a closed switch is:

$$I_{S(cyclic)} = I_{sc(LS)} \cdot \frac{t_{on(PxOut)}}{T_{cy}} \text{ for the application in Figure 6.}$$

$$I_S = I_{pd} = \frac{V_{BAT}}{R_{pd}} \text{ for the application in Figure 7.}$$

where:

$I_{sc(LS)}$ is the LOW-side short circuit current (see Ref. 1)

$t_{on(PxOut)}$ is the PxOut pin turned on (see Ref. 1)

T_{cy} is the cycle period time (see Ref. 1)

V_{BAT} is the reference voltage applied on BAT

R_{pd} is the external switch pull-down resistor.

2.1.1.3 Switch matrix

The UJA1023 provides a Switch matrix mode to handle situations where more switches than available I/O pins are required. With a switch matrix, up to 16 switches can be applied via the 8 I/O pins. Figure 8 shows an example application of a 4×4 switch matrix.

Matrices of 4×3 and 4×2 can also be connected, Table 2 shows the switch allocation table for Figure 8.

Table 2.   Switch allocation

Switch matrix			Switches (relating to Figure 8)			
4×4	4×3	4×2	SM40	SM41	SM42	SM43
			SM50	SM51	SM52	SM53
			SM60	SM61	SM62	SM63
			SM70	SM71	SM72	SM73
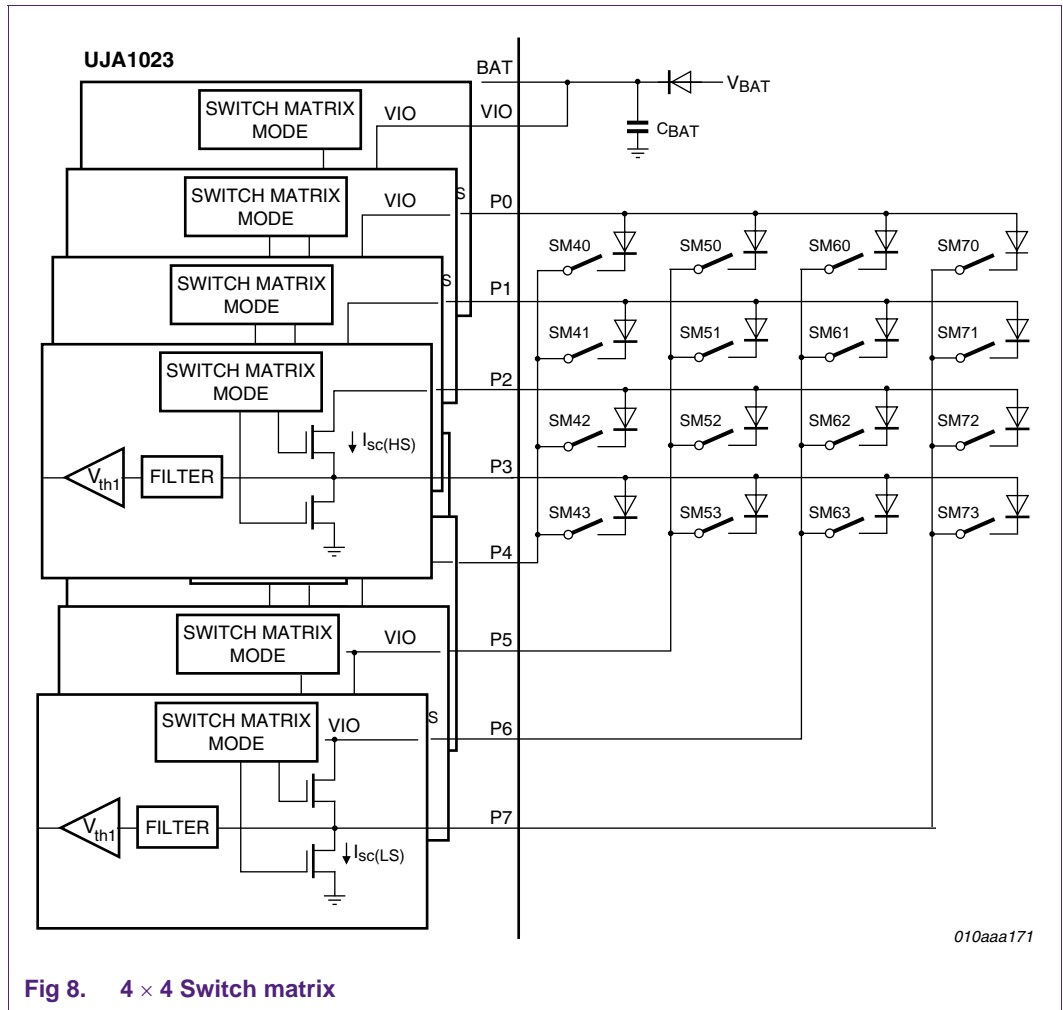
Fig 8.   4 × 4 Switch matrix

The diodes in Figure 8 are only recommended if the switches are closed simultaneously. Figure 9 shows how, without the diodes, the wrong switch could be detected.
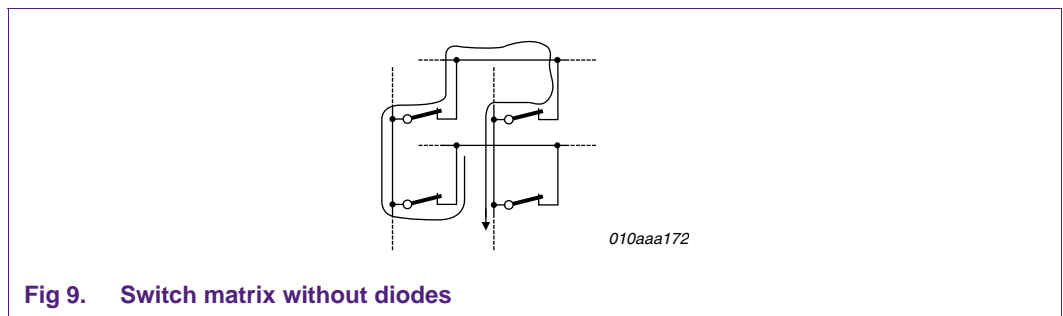
Fig 9.   Switch matrix without diodes

2.1.2 Switch application with different supply path

Switch applications with different supply paths are implementations where the switches are connected to a ground or battery voltage different from the ECU in the UJA1023: for example, if a switch is not connected to the ground on the PCB.

Such switch applications often imply plug connections and long wiring, where ESD injection risks are higher. The series resistor R_{SD} (see Figure 11) or R_{SU} (see Figure 12) will typically protect the I/O pin against ESD. For further details, see Section 5.3.

2.1.2.1 Switch to ground

In a situation where the applied switches have a ground path different from that in the UJA1023, it is recommended to add a series resistor to protect the I/O pins against a failure of loss of ground. If the ECU loses its ground connection while the switch is still connected to ground, the series resistor will limit the reverse current through the I/O pin's internal protection diode.

Due to the voltage divider between the internal pull-up and a series resistor, the internal HIGH-side transistor is used as a pull-up and the signal input cannot be realized via one I/O pin only. The switch pull-up can be realized either via a second I/O pin (see Figure 10) or via a resistor connected to the battery (see Figure 11).

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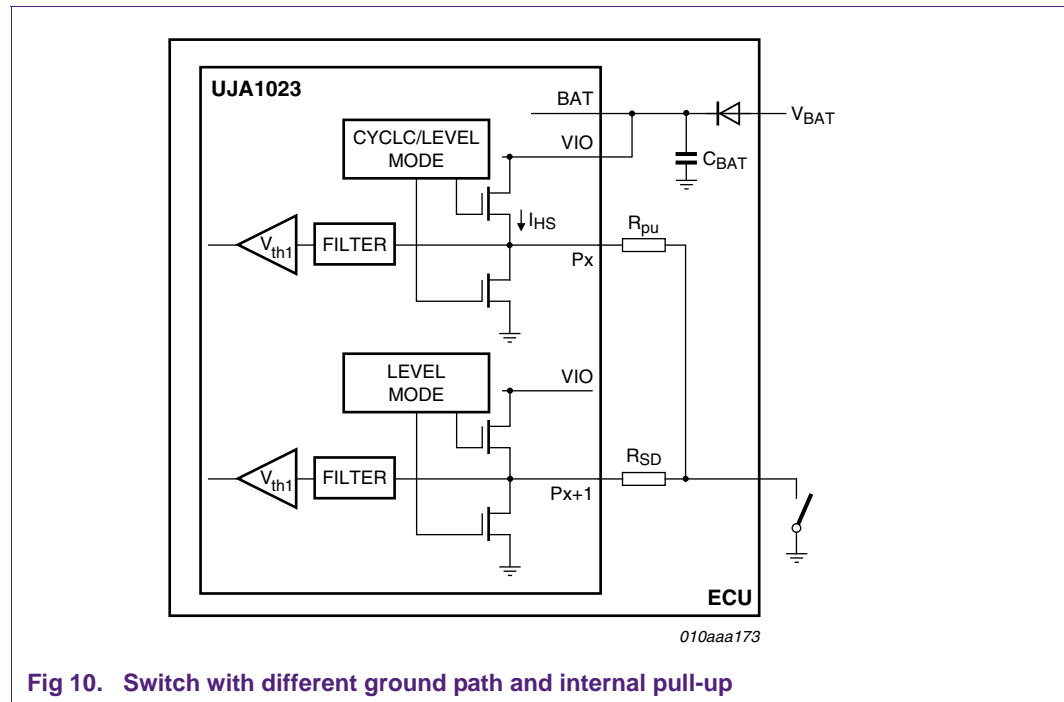
Fig 10. Switch with different ground path and internal pull-up

The maximum supply voltage on pin BAT, $V_{BAT(max)}$, and the applications ground shift $V_{GND\text{-}shift}$ between the UJA1023 and the switch principally define the value of series resistance R_{SD}. R_{SD} can be calculated using the following equations:

$$R_{SD(min)} < R_{SD} < R_{SD(max)} \quad \text{with}$$

$$R_{SD(min)} = \frac{V_{BAT(max)}}{\left|I_{Px(min)}\right|} \quad (I_{Px(min)} = -15 \text{ mA; see Ref. 1}) \text{ and}$$

$$R_{SD(max)} = \frac{V_{IL(th1)(Px)(max)} - \left|V_{GND-shift}\right|}{\left|I_{L(Px)(max)}\right|} \quad \text{with, for example: } V_{GND-shift} = 1.5 \text{ V}$$

where (see Ref. 1):

$V_{IL(th1)(Px)(max)}$ is the maximum Px LOW level input voltage.

$I_{L(Px)(max)}$ is the maximum Px input leakage current.

$I_{Px(min)}$ is the minimum DC current on pins P0 to P7 (limiting value).

Example: for a maximum ground shift of $V_{GND\text{-shift}}$ = 1.5 V and a maximum battery voltage of $V_{BAT(max)}$ = 27 V, the range of possible values for R_{SD} is:

$$R_{SD(min)} = \frac{V_{BAT(max)}}{|I_{Px(min)}|} = 1.8 \text{ k}\Omega$$

$$R_{SD(max)} = \frac{V_{IL(th1)(Px)(max)} - |V_{GND-shift}|}{|I_{L(Px)(max)}|} = 100 \text{ k}\Omega$$

Therefore a typical value for the series resistor R_{SD} would be 10 kΩ.

Similarly the series resistor R_{pu} for the I/O input of the internal HIGH-side transistor in Figure 10 is calculated from the following equations:

$$R_{puU(min)} < R_{pu} < R_{pu(max)} \text{ with}$$

$$R_{pu(min)} = \frac{V_{BAT(max)}}{|I_{Px(min)}|} \ (I_{Px(min)} = -15 \text{ mA; see Ref. 1}) \text{ and}$$

$$R_{pu(max)} = \frac{V_{ref(min)} - R_{SD} \cdot |I_{L(Px)(max)}| - V_{IH(th1)(Px)(min)} - |V_{GND-shift}|}{|I_{L(Px)(max)}|}$$

with, for example: $V_{GND-shift}$ = 1.5 V

where (see Ref. 1):

$V_{IH(th1)(Px)(min)}$ is the maximum Px HIGH level input voltage.

$V_{ref(min)}$ is the minimum VIO reference voltage.

$I_{L(Px)(max)}$ is the maximum Px input leakage current.

$I_{Px(min)}$ is the minimum DC current on pins P0 to P7 (limiting value).

The external pull-up resistor R_{pu} in Figure 11 is determined by the requirement for the current through the switch.
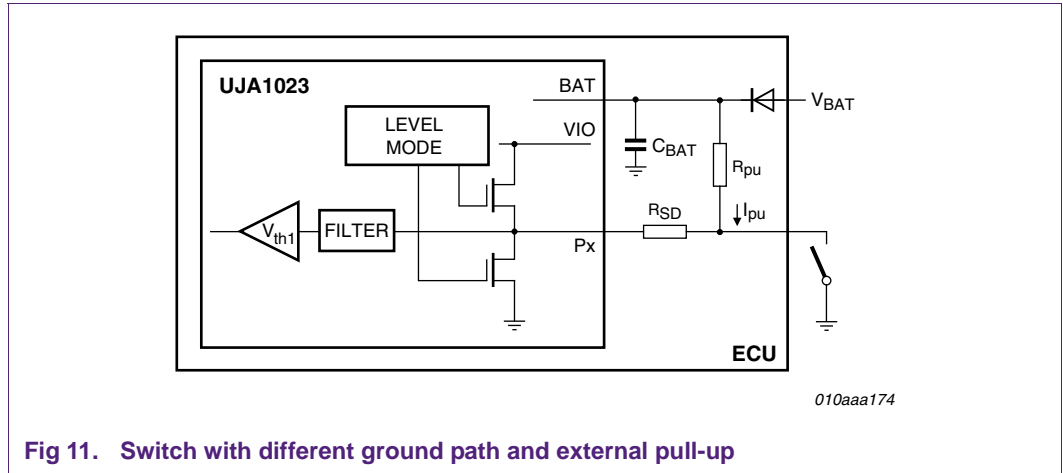
Fig 11. Switch with different ground path and external pull-up

2.1.2.2 Switch to battery

For switch applications with different battery paths between the UJA1023 and the switches, it is recommended to protect the I/O pins against a loss-of-battery failure via a series resistor. For loss of battery, where the ECU has lost its battery connection, the series resistor R_{SU} limits the reverse current through the internal protection diodes of the UJA1023. Figure 12 shows a switch application example for a switch with a different battery path.
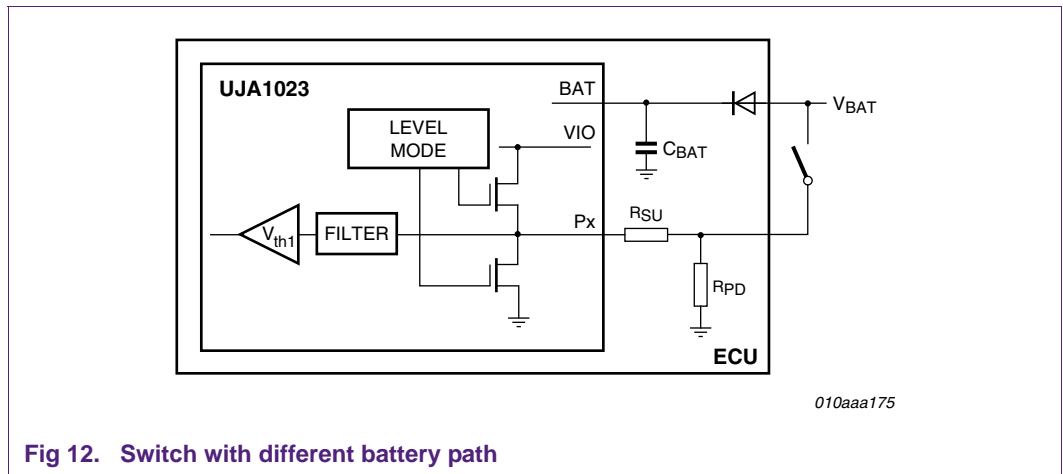
Fig 12. Switch with different battery path

The internal LOW-side transistor cannot be used as a switch pull-down because the internal pull-down transistor and the series resistor R_{SU} behave together like a voltage divider. The input signal on Px would be offset by this voltage divider.

The ground shift, $V_{GND\text{-}shift}$, between the UJA1023 and the switch together with the range of the battery voltage, V_{BAT}, defines the series resistor R_{SU}. The range of R_{SU} is given by the following equations:

$$R_{SU(min)} < R_{SU} < R_{SU(max)} \text{ with}$$

$$R_{SU(min)} = \frac{V_{BAT(max)}}{\left|I_{Px(max)}\right|} \text{ with } I_{Px(max)} = 15 \text{ mA and}$$

$$R_{SU(max)} = \frac{V_{IH(th1)(Px)(min)} - R_{PD} \cdot \left|I_{L(Px)(max)}\right|}{\left|I_{L(Px)(max)}\right|} \quad \text{with, for example, } R_{PD} = 10\,\text{k}\Omega$$

where (see Ref. 1):

$V_{IH(th1)(Px)(min)}$ is the minimum Px HIGH-level input voltage.

$I_{L(Px)(max)}$ is the maximum Px input leakage current.

$I_{Px(max)}$ is the maximum DC current on pins P0 to P7, limiting value.

For example: for an external pull-down resistor R_{PD} = 10 kΩ and a maximum battery voltage of V_{BAT} = 27 V, the range of R_{SU} is:

$$R_{SU(min)} = \frac{V_{BAT(max)}}{\left|I_{Px(max)}\right|} = 1.8\,\text{k}\Omega$$

$$R_{SU(max)} = \frac{V_{IH(th1)(Px)(min)} - R_{PD} \cdot \left|I_{L(Px)(max)}\right|}{\left|I_{L(Px)(max)}\right|} = 360\,\text{k}\Omega$$

A typical value for R_{SU} is 10 kΩ.

In Figure 12 the external pull-down resistor R_{PD} is independent of the UJA1023. Any value required for the switch can be chosen.

2.2 LED applications

Light-emitting diodes (LEDs) can be applied to the I/O pins of the UJA1023. Depending on the connection of the cathode either the HIGH-side transistor or the LOW-side transistor is used to drive the LED application.

2.2.1 HIGH-side output

The UJA1023 HIGH-side transistor is used if the cathode of the LED is wired to ground: One LED or a chain of LEDs can be connected to Px without a series resistor, but from the overall on-chip power dissipation and the thermal conditions it could be necessary to apply a series resistor R_D as shown in Figure 13.
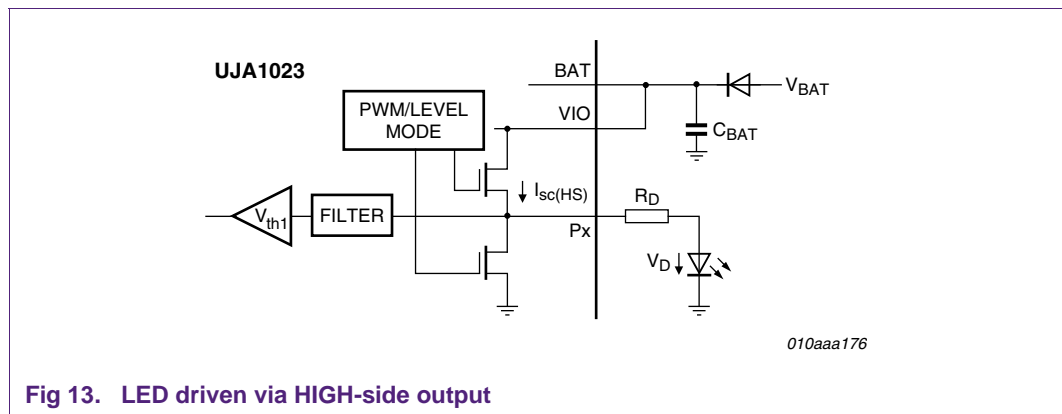

Fig 13. LED driven via HIGH-side output

The minimum value of the series resistor R_D depends mainly on the I/O reference voltage V_{VIO} and the HIGH-side short circuit current $I_{sc(HS)}$ (see Ref. 1). This can be calculated from the following equation:

$$R_{D(min)} = \frac{V_{VIO(max)}I_{sc(HS)(min)} - V_{D_{min}}I_{sc(HS)(min)} - P_{Px(max)}}{I_{sc(HS)(min)}^2}$$

where:

$V_{VIO(max)}$ is the maximum voltage VIO

$V_{D(min)}$ is the minimum voltage drop over the LED application

$I_{sc(HS)(min)}$ is the minimum Px HIGH-side short circuit current (see Ref. 1)

$P_{PX(max)}$ is the maximum Px on-chip power dissipation (see Section 2.5).

2.2.2 LOW-side output

For LED applications where the cathode is wired to a voltage source, such as V_{CC} or V_{BAT}, the LOW-side transistor is used to drive the LEDs. Due to the high short-circuit current $I_{sc(LS)}$ (see Ref. 1) of the LOW-side transistor, a series resistor R_D is recommended to limit the current. Figure 14 shows an application example where a LED is driven via the LOW-side transistor.
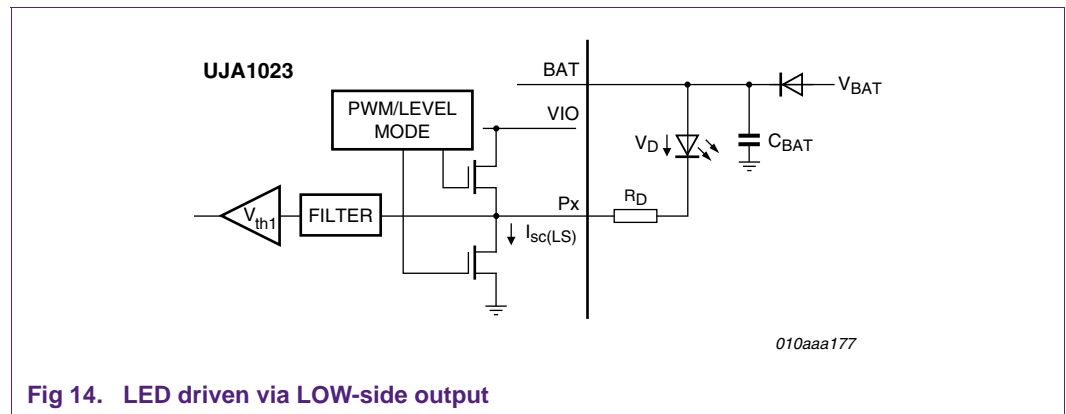
Fig 14. LED driven via LOW-side output

The value of series resistor R_D depends primarily on two factors: the LOW-side short circuit current $I_{sc(LS)}$ and the reference voltage V_{ref} of the LED application. The minimum value of R_D is given by the following equation:

$$R_{D(min)} = \frac{V_{ref(max)}I_{sc(LS)(max)} - V_{D(min)}I_{sc(LS)(mas)} - P_{PX(max)}}{I_{sc(LS)(max)}^2}$$

where:

$V_{ref(max)}$ is the maximum reference voltage (e.g. V_{BAT})

$V_{D(min)}$ is the minimum voltage drop over the LED application

$I_{sc(LS)(max)}$ is the maximum Px LOW-side short circuit current (see Ref. 1)

$P_{PX(max)}$ is the maximum Px on-chip power dissipation (see Section 2.5).

2.3 INH pin

2.3.1 External voltage regulator

The INH output of the UJA1023 can be used to control the inhibit input of one or more external voltage regulators. Figure 15 shows an INH pin application example.
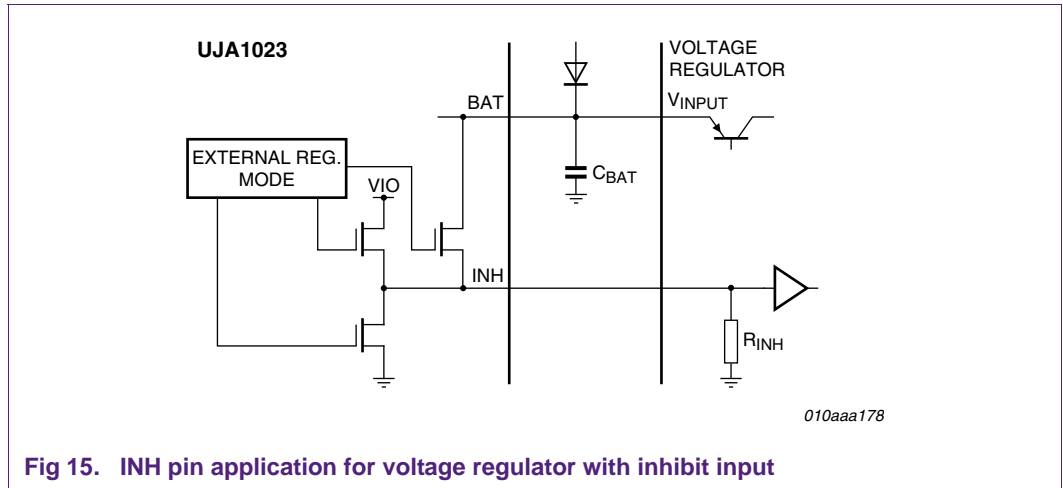
Fig 15. INH pin application for voltage regulator with inhibit input

The output of the INH is a battery-related open drain output. Therefore an external pull-down resistor R_{INH} connected to ground is required. This pull-down is typically integrated within the voltage regulator itself.

2.3.2 Analog-to-Digital Converter (ADC)

2.3.2.1 Functional description of the ADC

The UJA1023 contains a single ADC. This ADC is a bit stream converter. As shown in Figure 16, the bit stream converter is basically a feedback loop, where the input voltage on Px is compared with the reference voltage $0.5V_{VIO}$ on VIO and the 1-bit digital-to-analog converter (DAC) feeds back via INH the rectangle pulse ratio for the external integrator (R_{ADC} and C_{ADC}). The 1-bit code generated in the feedback loop is converted into an 8-bit code by the decimation filter.

Fig 16. Feedback loop of bit stream ADC

The comparator and the 1-bit DAC of the ADC are on-chip, while the adder and the integrator are connected externally. The 1-bit DAC output on INH is fed via the adder and the integrator to the comparator input on Px. The adder and the integrator are realized with an RC combination (R_{ADC} and C_{ADC}).

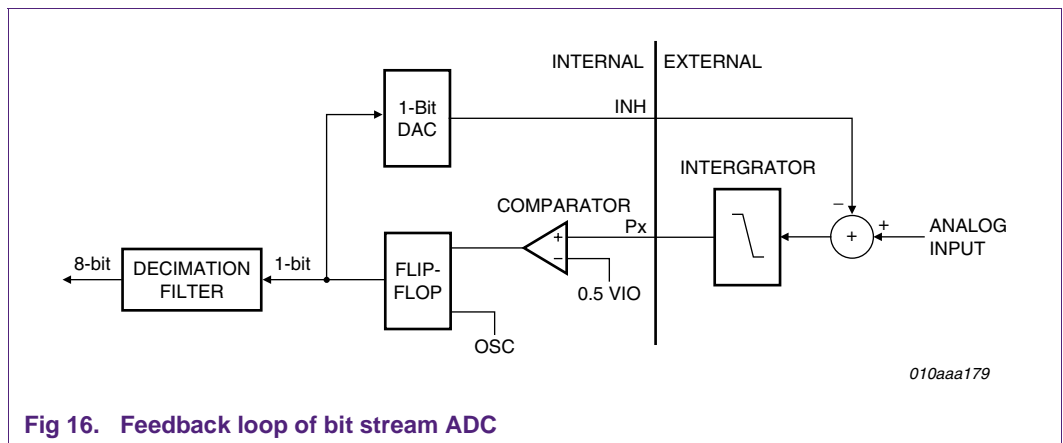The behavior of the feedback loop can be explained with the help of the ADC application example in Figure 17:

For a typical startup situation, a small analog input voltage V_A (near to 0 V) is applied via the potentiometer R_P. Assuming that a voltage above the upper switch-over voltage of the comparator is present on Px, then the output on INH is set to a voltage near to 0 V (see Figure 18). Now both the analog input voltage V_A and the feedback voltage V_{INH} are discharging capacitor C_{ADC}. As long as the voltage on Px remains above the lower switch overvoltage of the comparator, a '1' is clocked into the flip-flop, holding INH LOW. If the lower switch-over voltage is reached, the comparator output switches to LOW. With the next active edge of the sampling clock, the flip-flop will store a '0' and the INH output will be switched to HIGH (a voltage near to V_{VIO}). Now the capacitor C_{ADC} will be loaded and the voltage on Px increases again. A '0' will be stored as long as the voltage stays below the upper switch overvoltage of the comparator. When the upper switch-over voltage is reached, the comparator output is set to HIGH and the INH output is switched to LOW again. Then the cycle starts again.

This example clarifies that the rectangle pulse ratio on the INH output has to compensate fully the low voltage introduced by the analog input voltage V_A in order to be able to increase the voltage on Px. The same applies for a high analog input voltage, but here the voltage on the INH output has to be low enough for the compensation.
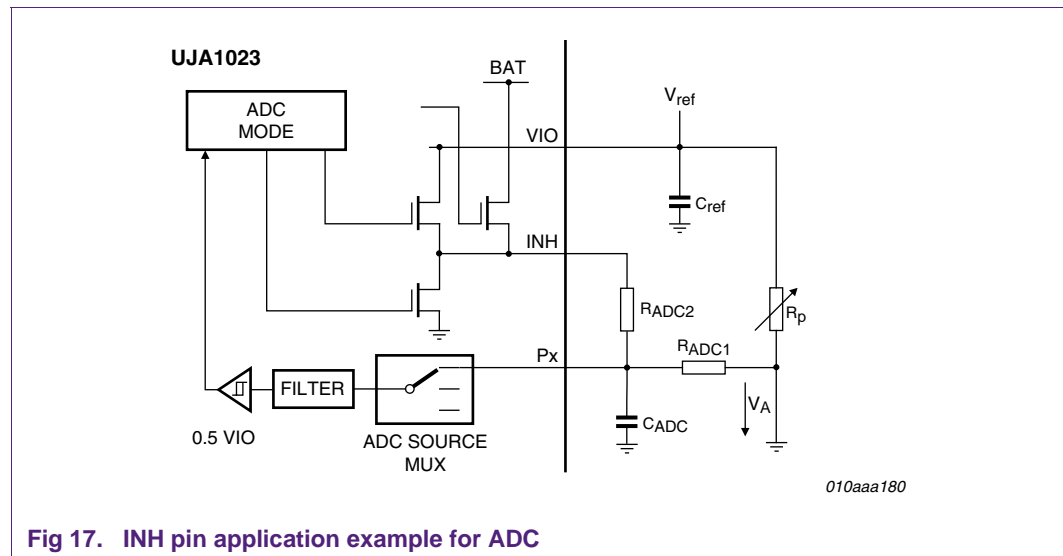

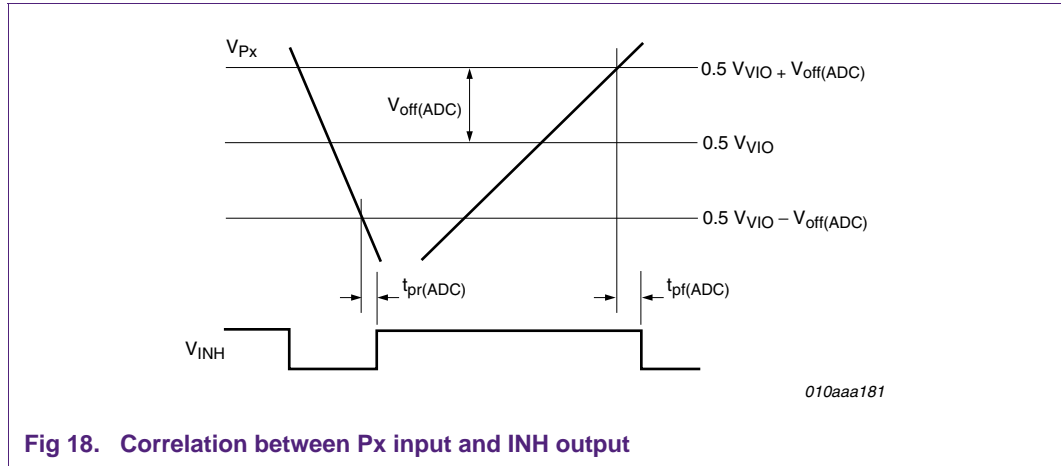**Fig 17. INH pin application example for ADC**

Fig 18. Correlation between Px input and INH output

2.3.2.2 External circuit of the ADC

The range of the analog input voltage, V_A, depends on the ratio of the external resistors R_{ADC1} and R_{ADC2} and the reference voltage $V_{ref} = V_{VIO}$ on VIO. It can be calculated from the following equations:

$$V_{A(min)} < V_A < V_{A(max)} \text{ with}$$

$$V_{A(min)} = \frac{R_{HSon(max)} + R_{ADC2} - R_{ADC1}}{R_{HSon(max)} + R_{ADC2}} \times \frac{V_{VIO}}{2}$$
$$+ \frac{R_{HSon(max)} + R_{ADC1} + R_{ADC2}}{R_{HSon(max)} + R_{ADC2}} \times V_{off(ADC)(max)}$$

and

$$V_{A(max)} = \frac{R_{LSon(max)} + R_{ADC1} + R_{ADC2}}{R_{LSon(max)} + R_{ADC2}} \times \left(\frac{V_{VIO}}{2} - V_{off(ADC)(max)} \right)$$

where

V_{VIO} is the reference voltage on VIO (e.g. V_{BAT}).

$V_{off(ADC)(max)}$ is the maximum comparator offset voltage 50 mV at $V_{VIO} = 12$ V

$R_{HSon(max)}$ is the maximum INH HIGH-level ON-resistance (180 Ω)

$R_{LSon(max)}$ is the maximum INH LOW-level ON-resistance (180 Ω).

With $R_{ADC1} = R_{ADC2}$ and $R_{HSon} = R_{LSon}$ a conversion is achieved, which best transforms the voltage range of V_A into the whole range of achievable digital values:

$$V_A > \frac{R_{on}}{R_{on} + R_{ADC}} \times \frac{V_{VIO}}{2} + \frac{R_{on} + 2R_{ADC}}{R_{on} + R_{ADC}} \times V_{off(ADC)}$$

$$V_A < \frac{R_{on} + 2R_{ADC}}{R_{on} + R_{ADC}} \times \left(\frac{V_{VIO}}{2} - V_{off(ADC)} \right)$$

AN10704_1

Application note **Rev. 01 — 6 April 2009** 16 of 36

For the evaluation of the ADC the values $R_{ADC1} = R_{ADC2} = 100$ kΩ and $C_{ADC} = 10$ nF were chosen. With $R_{ADC} = 100$ kΩ and $R_{on} = 108$ Ω ($R_{ADC} > R_{on}$) the ratio between R_{on} and R_{ADC} becomes smaller than one LSB. Hence the ON-resistance of the INH input can be neglected. As a result the voltage range of V_A can be simplified to:

$$2V_{off(ADC)} < V_A < V_{VIO} - 2V_{off(ADC)}$$

The external circuit should be connected with the shortest possible wiring to the applied I/O pins.

For the above calculation a low-ohmic analog voltage source is assumed. In Figure 17 an application example with a potentiometer R_P is shown; but typically, a potentiometer is not a low-ohmic voltage source. Hence it causes a non-linearity between the potentiometer position 'x' and the analog input voltage V_A:

$$\frac{V_A}{V_{VIO}}(x) \;=\; \frac{2R_{ADC1} + (1-x)R_P}{2R_P R_{ADC1} + 2x(1-x)R_P{}^2} x R_P$$

where:

   V_{VIO} is the reference voltage on VIO (e.g. V_{BAT}).

For example: with $R_{ADC1} = 100$ kΩ and $R_P = 10$ kΩ, the V_A deviation from the position 'x' stays below 0.5 %. Figure 19 shows the impact of the potentiometer value for $R_P = 10$ kΩ and $R_P = 100$ kΩ.
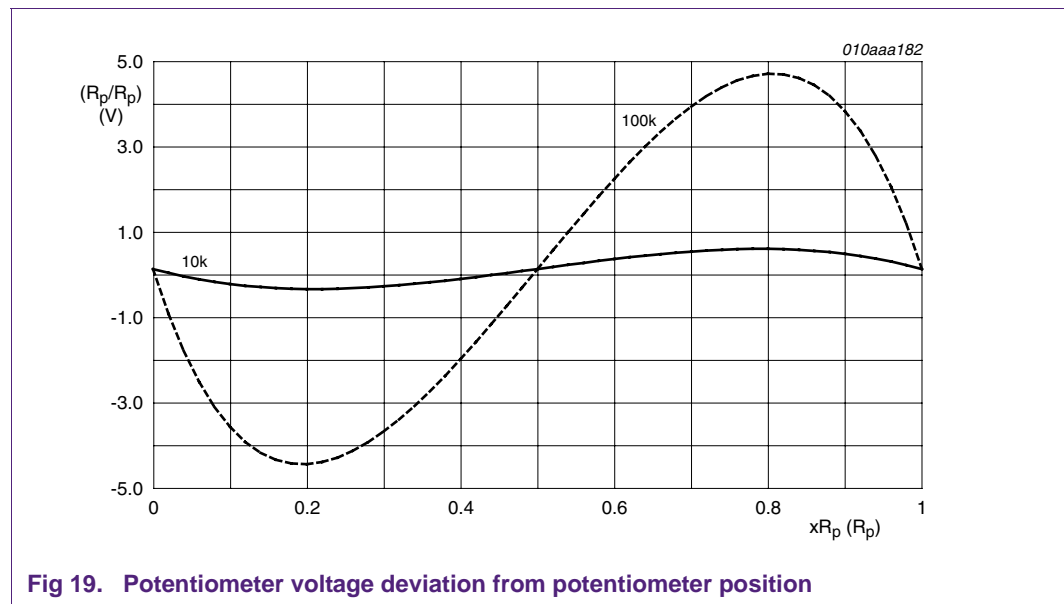

Fig 19. Potentiometer voltage deviation from potentiometer position

2.3.2.3 ADC source multiplexer

For analog-to-digital conversion, only one analog input signal at a time can be applied. More analog input signals can be converted sequentially via the on-chip ADC source multiplexer (see Figure 17). With the multiplexer (MUX), up to 8 analog input sources can be converted.

The application of more than one ADC input source can have a small impact on ADC accuracy, because the current through the ON-resistance, R_{HSon} and R_{LSon}, can vary between one and the factor of applied analog input sources. With $R_{ADC} = R_{ADC1} = R_{ADC2}$ and $R_{on} = R_{HSon} = R_{LSon}$, the ratio between the voltage V_{Ron} over R_{on} and the reference voltage V_{VIO} can be calculated with the following equation:

$$\frac{V_{Ron}}{V_{VIO}} = \frac{nR_{on}}{2R_{ADC} + nR_{on}}$$ where n is the number of ADC input sources (n = 1 to 8)

For example: for R_{ADC} = 100 kΩ, the ratio between V_{Ron} and V_{VIO} might be up to 0.4 % if n = 8. This is in the range of one LSB.

2.3.2.4 ADC sampling

After each complete reception of both the Synchronization Break (SB) and the following Synchronization Field (SF), the analog-to-digital conversion is started. Thus the conversion is triggered independently of the LIN frame identifier. The ADC sampling is shown in Figure 20.
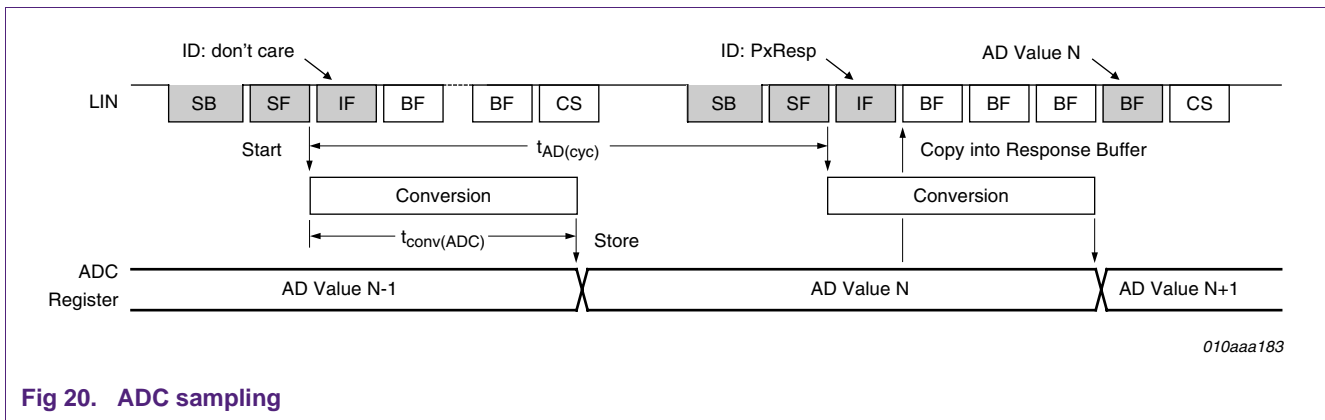
Fig 20. ADC sampling

The converted AD value is stored in an internal ADC register, which is overwritten with each subsequent AD conversion. The AD value can be read via the UJA1023 LIN message frame PxResp. The AD value is provided in the 4th Byte Field (BF) of the PxResp message.

Since the conversion time $t_{conv(ADC)}$ depends on the oscillator frequency f_{osc} (see Ref. 1), it can be calculated from the following equation:

$$t_{conv(ADC)} = \frac{1024}{f_{osc}}$$

where:

   f_{osc} is the internal oscillator frequency (f_{osc} = 450 kHz to 1 MHz).

The ADC cycle time $t_{cy(ADC)}$ must be longer than the conversion time $t_{conv(ADC)}$; otherwise the conversion starts again before the previous conversion has been completed. Thus the minimum cycle time $t_{AD(cyc)(min)}$, is given by the minimum oscillator frequency $f_{osc(min)}$:

$$t_{cy(ADC)(min)} > \frac{1024}{f_{osc(min)}}$$

where:

$f_{osc(min)}$ is the minimum internal oscillator frequency ($f_{osc(min)}$ = 450 kHz).

2.4 Power applications

In many cases the UJA1023 can be used for power applications: e.g. lamps, motors, or heaters can be driven via external power devices like power MOS switches. Since the number of power devices is almost endless only two applications are shown in the following sections.

2.4.1 Power MOS application

A power MOS switch typically has a standard logic level interface for 5 V. An adaptation of the UJA1023 I/O pins to a standard logic level via an external voltage regulator (e.g. Zener diode) is possible, but typically the I/O pin can use battery-related levels by connecting the VIO pin to the LIN slave battery supply voltage. In this case a series resistor is placed between the output of the UJA1023 and the input of the power MOS. A series resistor is not required in the reverse direction from the power MOS output to the UJA1023 input. However, some unloaded power MOS outputs (e.g. status signal) may require either pull-up or pull-down resistors.

An example of an application for a HIGH-side power MOS switch is shown in Figure 21. It can be seen that a power MOS interface is commonly ESD-protected with on-chip suppressor diodes. This has to be taken into account for the dimensioning of the series resistor R_{IN}. The input voltage V_I and current I_I are specified in the data sheets of power MOS switches.

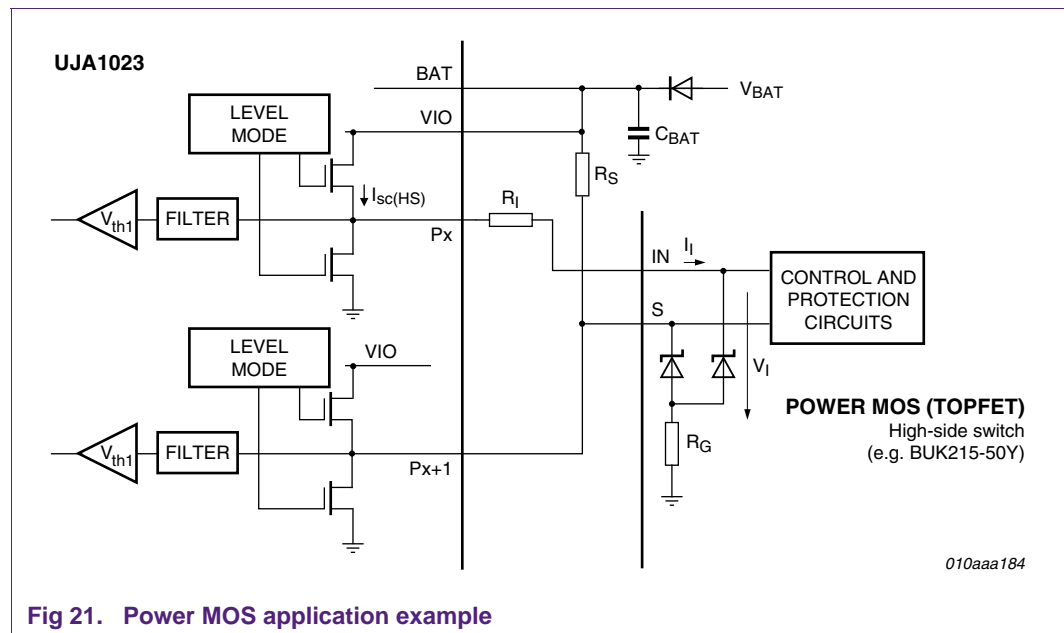

Fig 21.   Power MOS application example

For example: the value of the input series resistor R_I in the power MOS application shown in Figure 21 can be calculated as follows:

$$R_{I(min)} < R_I < R_{I(max)} \text{ with}$$

$$R_{I(min)} = \frac{V_{BAT(max)} - V_{I(clamp)(min)}}{I_{I(max)}} \text{ and}$$

$$R_{I(max)} = \frac{V_{BAT(min)} - V_{I(on)(max)}}{I_{I(on)(max)}}$$

where:

$V_{I(clamp)(min)}$ is the minimum IN clamping voltage.

$V_{I(on)(max)}$ is the maximum IN turn-on threshold voltage.

$I_{I(max)}$ is the maximum IN continuous current.

$I_{I(on)(max)}$ is the maximum IN turn-on current.

2.4.2 MOSFET application

The MOSFET application example in Figure 22 shows an N-channel transistor. An N-channel MOSFET is typically used as a LOW-side power switch. It can be seen that the battery voltage is applied on the HIGH-level I/O output reference VIO. So the MOSFET is switched with the battery-related output of the UJA1023. In most cases, the maximum battery voltage is higher than the maximum transistor gate-source voltage, $V_{GS(max)}$. Therefore, a simple voltage divider (R_{I1} & R_{I2}) may be applied to reduce the voltage levels between the UJA1023 and the MOSFET gate.
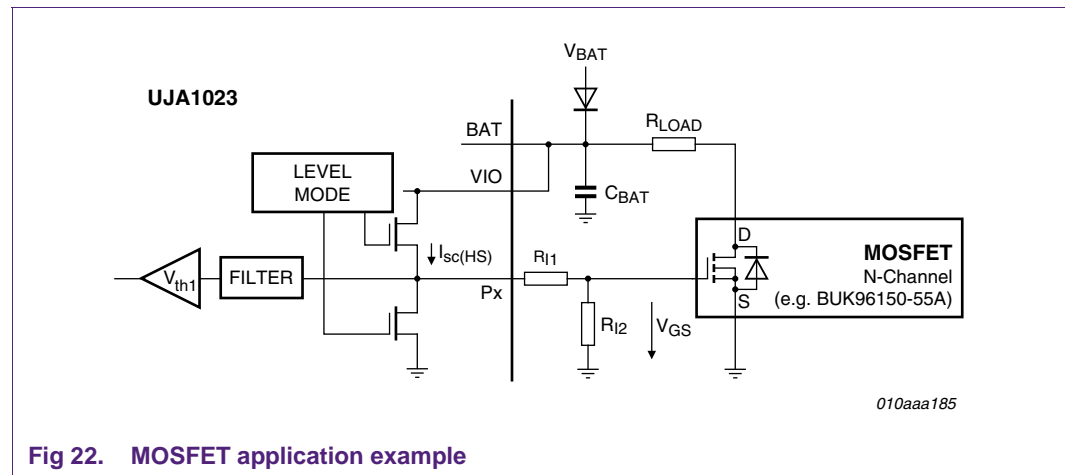
Fig 22. MOSFET application example

2.5 Thermal analysis

The maximum power dissipation P_{max} of the UJA1023 depends on the thermal resistance $R_{th(j-a)}$ (see Ref. 1) of the IC package, the maximum virtual junction temperature $T_{vj(max)}$ (see Ref. 1) and the maximum ambient temperature $T_{amb(max)}$. $R_{th(j-a)}$ is the ability of the IC package to disperse heat to its environment and is typically specified for free-air conditions. The use of large copper planes attached to the GND pin in real-world applications can reduce the thermal resistance and hence increase the value of the maximum power dissipation P_{max}.

The power dissipation of the UJA1023 is the sum of the base dissipation and the I/O pin dissipation, P_{IO}. The base power dissipation is independent of external applications. It depends only on the supply voltage V_{BAT}. The I/O pin dissipation, P_{IO}, is determined by the external circuitry in the application. This should not exceed $P_{IO(max)}$, which is given by the following equation:

$$P_{IO(max)} = P_{max} - V_{BAT(max)} \times I_{BAT(b)(max)} - V_{VIO} \times I_{VIO(max)} \text{ with}$$

$$P_{max} = \frac{T_{vj(max)} - T_{amb(max)}}{R_{th(j-a)}} \text{ and}$$

$$I_{BAT(b)} = 0.45 \times I_{BAT(LIN, dom)(max)} + N\frac{I_{BAT(HS \& LS, EN)(max)}}{8} \text{ and}$$

$$I_{VIO(max)} = N\frac{I_{VIO(HS, EN)(max)}}{8} + M(I_{VIO(ADC, EN)(max)} - I_{VIO(HS, EN)(max)})$$

where:

$V_{BAT(max)}$ is the maximum voltage on pin BAT (see Ref. 1).

$I_{BAT(LIN, dom)(max)}$ is the maximum supply current into pin BAT (Normal mode; LIN sending dominant) (see Ref. 1).

$I_{BAT(HS \& LS, EN)(max)}$ is the maximum supply current into pin BAT (additional current if all HIGH- and LOW-side switches are activated; see Ref. 1).

N is the number of activated switches (N:= 0…8; see Ref. 1).

$I_{VIO(HS, EN)(max)}$ is the maximum supply current into pin VIO (HIGH-side switches are activated; see Ref. 1)

$I_{VIO(ADC, EN)(max)}$ is the maximum supply current into pin VIO (ADC enabled; see Ref. 1)

M is the number of enabled ADC (M:= 0...1; see Ref. 1).

$T_{vj(max)}$ is the maximum virtual junction temperature (K; see Ref. 1).

$T_{amb(max)}$ is the maximum ambient temperature (K).

$R_{th(j-a)}$ is the thermal resistance (K/Ω; see Ref. 1).

The I/O pin power dissipation P_{IO} is the dissipation sum on all I/O pins and the INH pin.

$$P_{IO(max)} > P_{INH(max)} + \sum_{x=0}^{7} P_{Px(max)} = P_{INH(max)} + P_{P0(max)} + P_{P1(max)} + \dots + P_{P7(max)}$$

where:

$P_{INH(max)}$ is the maximum INH on-chip power dissipation

$P_{PX(max)}$ is the maximum Px on-chip power dissipation.

When calculating values for the external I/O components in an application, care should be taken that the total I/O pin power dissipation is less than $P_{IO(max)}$.

3. Configuration interface of the UJA1023

3.1 Overview

The UJA1023 configuration is performed in accordance with the LIN 2.0 Diagnostic and Configuration Specification (see Ref. 2). In the LIN 2.0 Specification (see Ref. 2), the Packet Data Unit (PDU) structure is applied where the 1st, 2nd and the 3rd data bytes determine the usage of the remaining 5 data bytes. The basic structure of a PDU is shown in Table 3. Each PDU should include the LIN slave Node ADdress (NAD), the Protocol Control Information (PCI) and the Service IDentifier (SID) or Response Service IDentifier (RSID).

Table 3.   Packet data unit

Byte	Symbol	Description	
0	NAD	Node Address 0:	reserved for go-to-sleep-command
		Node Address 1 to 126:	diagnostic slave node address
		Node Address 127:	reserved for broadcast (wild cards)
		Node Address 128 to 255:	free usage (to be compatible to LIN1.3)
1	PCI	Protocol Control Information:	4 MSB bits = 0000/ 4 LSB bits = number of data bytes
2	SID/RSID	(Response) Service Identifier:	determines the contents of the data bytes
3	D1	data depends on SID	
4	D2	data depends on SID	
5	D3	data depends on SID	
6	D4	data depends on SID	
7	D5	data depends on SID	

The PDU is embedded in the Master Request (MR) and Slave Response (SR) LIN commands. The LIN frame identifiers are 60 (3Ch) for the MR and 61 (3Dh) for the SR. The services (SID/RSID) specify the use and contents of the 5 data bytes. Two kinds of services are defined: SID for MR messages and RSID for SR messages. All LIN 2.0 service identifiers (SID/RSID) are listed in Table 4.

Table 4.   Service identifier

SID/RSID (HEX)	Description
B0	Request: Assign NAD
F0	Response: positive feedback of Assign NAD
B1	Request: Assign Frame ID (mandatory)
F1	Response: positive feedback of Assign Frame ID
B2	Request: Read by Identifier (mandatory)
F2	Response: positive feedback of Read by Identifier
B3	Request: Conditional Change NAD
F3	Response: positive feedback of Conditional Change NAD

Table 4. **Service identifier**

SID/RSID (HEX)	Description
B4	Request: Data Dump
F4	Response: Data Dump feedback
7F	Response: negative feedback

The UJA1023 NAD and LIN Frame identifier configuration can be executed with the LIN 2.0 configuration services (see Ref. 2) Assign NAD and Assign Frame ID. Additionally, a confirmation can be received via LIN 2.0 RSID from the UJA1023 for each transmitted configuration message. Applying this handshaking concept ensures the correct recognition of the configuration bytes.

The LIN I/O slave has three configuration input pins which represent the initial NAD according to LIN 2.0 (see Ref. 2). This allows for the differentiation of eight identical slave devices via plug coding in one LIN network. The UJA1023 configuration pins can be routed to the module plug, enabling differentiation between electrically equivalent modules. Alternatively, the slaves can be configured through a daisy chain NAD configuration option. This makes it possible to extend the number of slaves in one network beyond eight identical slave devices.

All hardware-related configuration is realized with the help of the LIN 2.0 configuration service Data Dump (see Ref. 2). The versatile configuration possibilities of the UJA1023 are covered with three optional messages. Similar to the NAD and Frame ID configuration, the I/O port configuration can be reviewed via a SR, the Data Dump response service. Furthermore, the UJA1023 provides diagnostic data via this response service.

Table 5. **Overview of configuration services**

Name	Typ	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Assign NAD	MR	Initial NAD	PCI HEX: 06	SID HEX: B0	NXP ID HEX: 0011		UJA1023 ID HEX: 0000		New NAD
	SR	Initial NAD	PCI HEX: 01	pRSID HEX: F0	HEX: FF	HEX: FF	HEX: FF	HEX: FF	HEX: FF
Assign Frame ID	MR	NAD	PCI HEX: 06	SID HEX: B1	NXP ID HEX: 0011		Message ID		Frame ID
	SR	NAD	PCI HEX: 01	pRSID HEX: F1	HEX: FF	HEX: FF	HEX: FF	HEX: FF	HEX: FF
Read by Identifier	MR	NAD	PCI HEX: 06	SID HEX: B2	Identifier HEX: 00	NXP ID HEX: 0011		UJA1023 ID HEX: 0000	
	SR	NAD	PCI HEX: 01	pRSID HEX: F2	NXP ID HEX: 0011		UJA1023 ID HEX: 0000		Variant
	SR	NAD	PCI HEX: 03	nRSID HEX: F7	Req SID HEX: B2	Error HEX: 12	HEX: FF	HEX: FF	HEX: FF
Data Dump	MR	NAD	PCI	SID HEX: B4	I/O Port configuration data				
	SR	NAD	PCI	RSID HEX: F4	I/O port review data / slave diagnosis data				

An overview of the UJA1023 configuration services is shown in Table 4. In addition to these configuration services, the LIN I/O slave provides two LIN commands for the I/O ports. One is used for sending output values to the ports and the other transmits I/O slave input values to the LIN master.

A typical configuration flow for the UJA1023 is shown in Figure 23. The configuration flow is not disturbed if LIN commands other than those shown in Figure 23 are sent to other LIN slave nodes. Thus the LIN master can transmit other LIN messages while it (re-)configures the UJA1023. Even when a second MR follows the MR instead of the SR, the LIN I/O slave configuration message remains valid. Thus the use of the SR is optional.

Although for the I/O configuration the use of the three data dump configuration services is optional, the sequence of these services is not optional. Thus if more than one I/O configuration block has to be transmitted via data dump services, the sequence has to be in ascending order of the I/O configuration block numbers: for example the 3rd I/O configuration data block (see Ref. 1) follows the 2nd I/O configuration block (see Ref. 1).
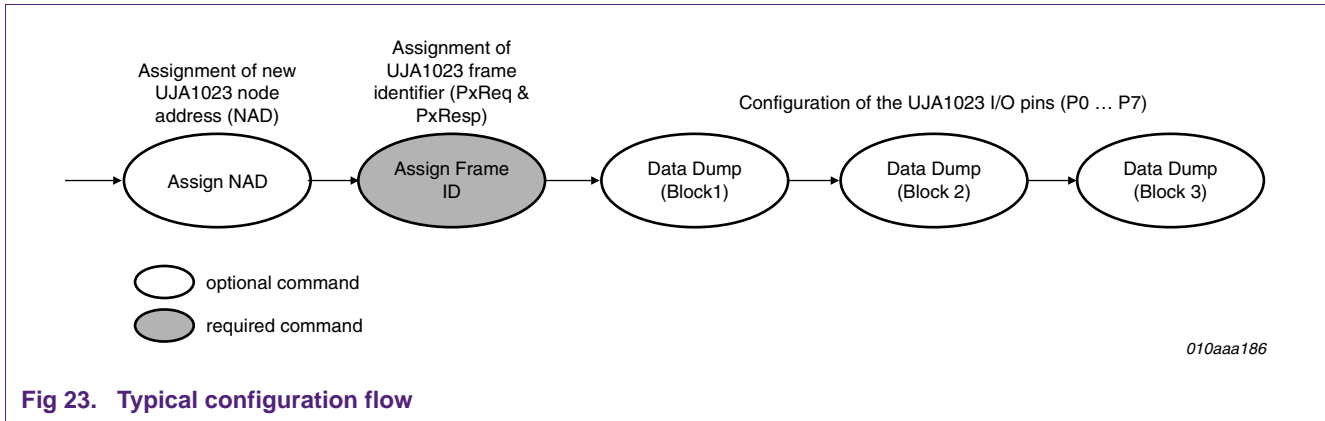

Fig 23.   Typical configuration flow

3.2   Node address assignment

With the service Assign NAD (see Ref. 2) it is possible to (re-)configure a NAD of a dedicated LIN slave if more equal LIN slaves are present. If the Assign NAD is used, LIN slaves can be distinguished between the Supplier ID, the Function ID and between their Initial NAD. Table 6 shows the contents of an Assign NAD request.

Table 6.   Assign NAD

D0	D1	D2	D3	D4	D5	D6	D7
Initial NAD	PCI HEX: 06	SID HEX: B0	Supplier ID LSB	Supplier ID MSB	Function ID LSB	Function ID MSB	New NAD

The new NAD of the UJA1023) is assigned when the LIN supplier code of NXP (0011h) and the UJA1023 function ID (0000h) of the Assign NAD service has been received (see Ref. 1). The function ID is the unique 16-bit NXP product identifier of the LIN I/O slave. This identifier is necessary to differentiate between different LIN slave products from the same product supplier.

The Initial NAD is like a fixed default node address which cannot be changed via a LIN command. It makes sure that the NAD as well as Frame ID can be (re)configured if a LIN slave node has changed or lost its NAD or Frame ID (stored in RAM) in consequence of EMC, ESD or short supply voltage drops.

Furthermore, the Initial NAD is used to differentiate between similar LIN slaves, e.g. when more than one UJA1023 is applied in a network. The UJA1023 provides two ways to make this differentiation: the plug NAD assignment and the daisy chain NAD assignment. The type of NAD assignment can be distinguished on the Initial NAD. In Table 7 all initial NADs of the UJA1023 are shown.

Table 7.   Initial NAD

Initial NAD (HEX)	Description
08 to 0F	Plug NAD Assignment (see Section 3.2.1).
20	Daisy chain NAD assignment initialization. Enables daisy chain pull-ups (see Section 3.2.2).
21	Daisy chain NAD assignment. Assigns the new NAD (see Section 3.2.2).
23	Daisy chain NAD assignment finished. Disable daisy chain pull-ups (see Section 3.2.2).
70	Physical layer test mode. The input on P6 is put through to the LIN bus (like a TXD) and the output on P7 represents the LIN bus states (like a RXD).
71	Auto bit rate detection test mode. Received data can be "mirrored" back.

3.2.1 Plug NAD assignment

The plug NAD assignment (see Ref. 1) is the default slave-node address assignment of the UJA1023, i.e. after power-on the plug NAD assignment is applied automatically. Thus it is not necessary to perform the assign NAD service (see Ref. 2). Nevertheless a new NAD can be assigned via the service assign NAD (see Ref. 2) if another NAD than the default is requested.

The default NAD of the UJA1023 depends on the input levels on the configuration pins. Table 8 shows the correlation of the default NAD to the configuration pin input. Furthermore, the Initial NAD for the configuration pin combinations is shown. When the UJA1023 gets a new NAD, the initial NAD is used within the assign NAD service to address the LIN slave. The new NAD is assigned only if the Initial NAD matches.

Table 8.   Correlation between address pins, initial NAD and default NAD

Address pins			Initial NAD (HEX)	Default NAD (HEX)
C3	C2	C1		
0	0	0	08	60
0	0	1	09	61
0	1	0	0A	62
0	1	1	0B	63
1	0	0	0C	64
1	0	1	0D	65
1	1	0	0E	66
1	1	1	0F	67

All configuration pins have an on-chip pull-up: i.e. the default input is HIGH. Thus a LOW on a configuration pin can be achieved with a connection to ground.
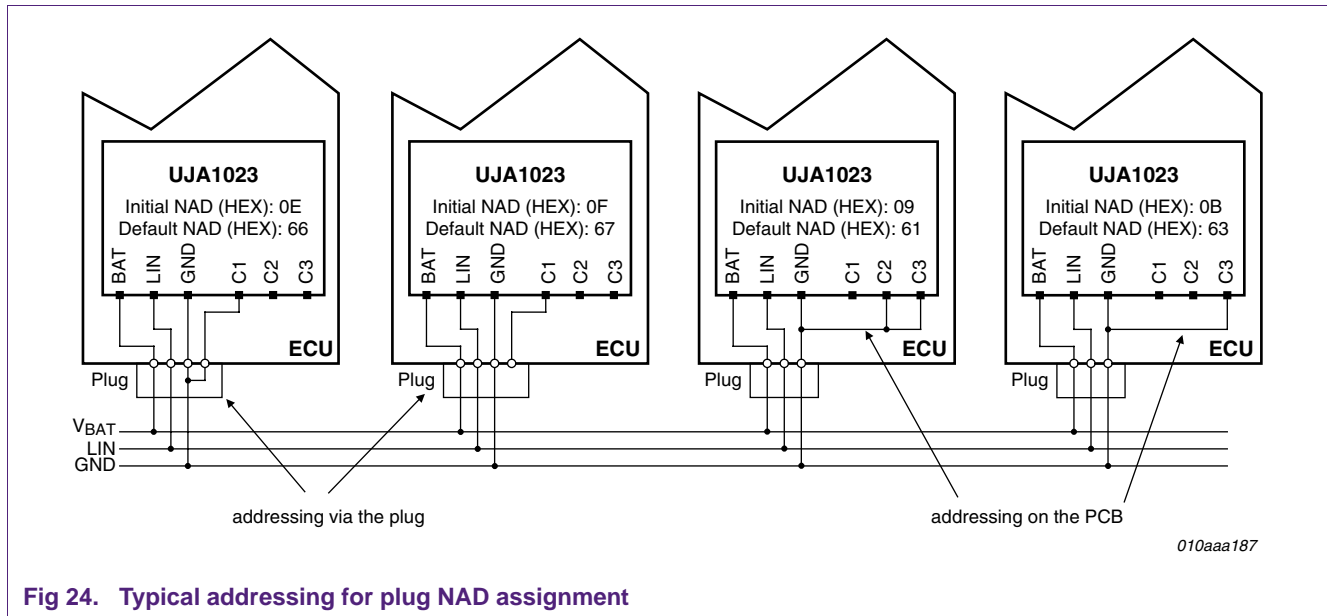
Fig 24. Typical addressing for plug NAD assignment

There are two options for addressing the UJA1023 via the plug NAD assignment (see Ref. 1 and Figure 24):

- Addressing via the plug:
  - One or all configuration pins are connected to the plug of the ECU. The differentiation of the LIN I/O slaves is made via the plug. Each ECU can be completely identical.
- Addressing on the PCB:
  - The differentiation of the LIN I/O slaves is applied on the PCB of the ECU. The addressing can be realized with hard-wired connections or with assembly options.

3.2.2 Daisy chain NAD assignment

After power-on, the plug NAD assignment is carried out by default. However, once the UJA1023 receives the service Assign NAD (see Ref. 2), it analyzes the initial NAD (see Ref. 1). If the initial NAD is Daisy Chain ON, it enables the pull-up on the internal configuration pins of each UJA1023 respectively. The new NAD is assigned and the output on C3 is driven LOW, when the initial NAD, and the assigned NAD has been received via daisy chain and the input level on C1 is LOW. With the initial NAD, Daisy Chain OFF, the NAD assignment is completed and the pull-up on the configuration pins is disabled.
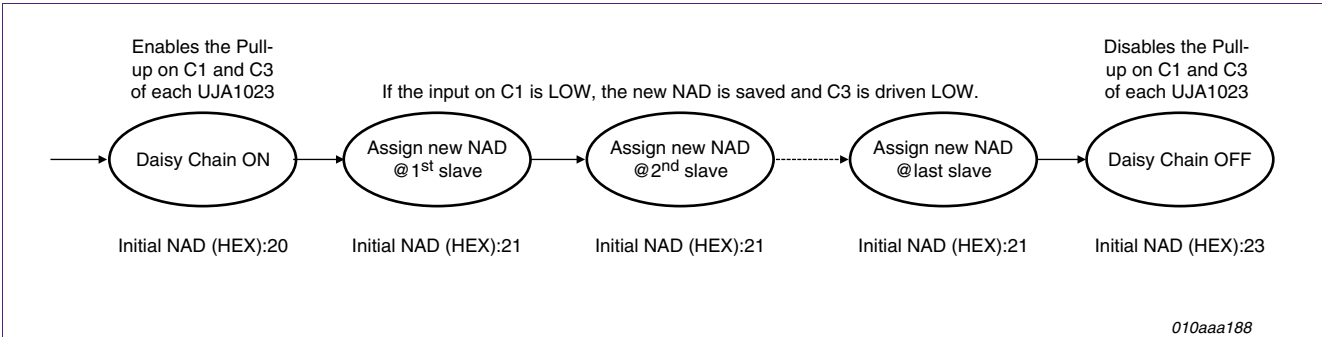
Fig 25. Daisy chain NAD assignment flow

In Figure 25, the typical daisy chain NAD assignment flow is illustrated. First the daisy chain assignment is initialized, then all LIN I/O slaves are successively configured, and finally the daisy chain assignment is finished.

The typical wiring of the UJA1023 daisy chain is shown in Figure 26. The configuration pin C1 of the 1st slave is hardwired to ground and pin C3 is connected to the C1 pin of the 2nd slave. The configuration pin C3 of the 2nd slave is connected to the C1 pin of the 3rd slave and so on.
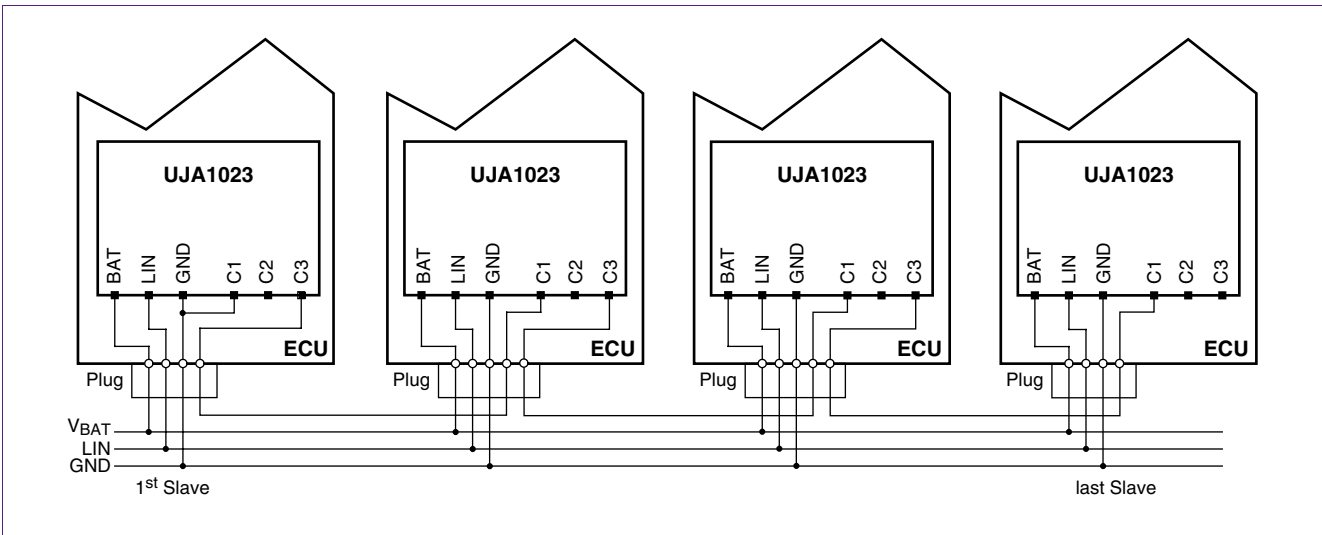

Fig 26. Typical daisy chain

A typical NAD assignment message trace for the UJA1023 daisy chain in Figure 26 is given in Table 9. It shows that other LIN commands can be sent in between and an SR is not required.

Table 9. Example of a typical daisy chain NAD assignment message trace

LIN frame message trace	Description
SB SF 3C 20 06 B0 11 00 00 00 00 19	//Daisy Chain ON(Pull-up ON)
...	//Optional other LIN commands
SB SF 3C 21 06 B0 11 00 00 00 30 E6	//Assignment NAD via Daisy Chain @ 1st slave with 30 (HEX)
...	// Optional other LIN commands

Table 9.   Example of a typical daisy chain NAD assignment message trace *…continued*

LIN frame message trace	Description
SB SF 3C 21 06 B0 11 00 00 00 31 E5	//Assignment NAD via Daisy Chain @ 2nd slave with 31 (HEX)
...	// Optional other LIN commands
SB SF 3C 21 06 B0 11 00 00 00 46 D0	//Assignment NAD via Daisy Chain @ last slave with 46 (HEX)
...	// Optional other LIN commands
SB SF 3C 23 06 B0 11 00 00 00 00 16	//Daisy Chain OFF (Pull-up OFF)
...	

3.3   LIN frame identifier assignment

The Assign Frame ID service (see Ref. 2) is used to (re-)assign the protected frame identifiers (see Ref. 2) to the application-specific LIN slave frames. A protected LIN frame identifier is the Frame identifier together with its parity bits. The configuration service Assign Frame ID is shown in Table 10.

Table 10.   Assign frame ID

D0	D1	D2	D3	D4	D5	D6	D7
NAD	PCI HEX: 06	SID HEX: B1	Supplier ID LSB	Supplier ID MSB	Message ID LSB	Message ID MSB	Protected ID

The UJA1023 has two application-specific LIN slave frames (see Ref. 1); the PxReq and the PxResp. The protected frame identifiers are assigned to PxReq and PxResp via a message identifier. The differentiation between the application specific LIN slave frames is made via the unique supplier ID (NXP ID) and a unique supplier-dependent message identifier.

The UJA1023 provides three message identifiers for the protected frame identifier assignment of PxReq and PxResp. The message identifiers are shown in Table 11. The message ID 0000h can be used to simultaneously assign both PxReq and PxResp. Whereas PxReq is assigned with the protected ID in the Assign Frame ID service, PxResp is automatically assigned with the incremented-by-one protected ID. Nevertheless with the message identifiers 0001h and 0002h the respective protected identifiers for PxReq and PxResp can be assigned independently of each other.

Table 11.   Message identifier

Message ID		LIN I/O slave frames
MSB (HEX)	LSB (HEX)	
00	00	PxReq and PxResp (= Protected ID +1)
00	01	PxResp
00	02	PxReq

4.   The LIN transceiver within the UJA1023

The UJA1023 contains a LIN transceiver according to the LIN 2.0 specification (see Ref. 2). The general implementation principle is according to the TJA1020 with several system optimizations dealing with LIN 2.0 options.

4.1 States of the LIN transceiver

Figure 27 shows the state diagram of the LIN transceiver. It consists of three states; the Active mode, the Off-line mode and the Failsilent mode. These states are directly coupled to the main states of the UJA1023. When the LIN I/O slave is in Configuration mode, Normal mode or Standby mode, the LIN transceiver will be in Active mode. In all other cases, the LIN transmitter will be in either Off-line mode or Failsilent mode. The state diagram distinguishes between transitions that are master-controlled and/or automatic.

UJA1023 Active Modes:
- Configuration
- Normal
- Standby

UJA1023 Low Power Modes:
- Sleep
- LH Sleep
- Limp Home

Active
R_{LIN}: $R_{pu(slave)}$
Tx: ON

Failsilent
R_{LIN}: OFF
Tx: OFF

Off-Line
R_{LIN}: I_{pu}
Tx: OFF

$LIN < V_{THR}$ for $t > t_{to(dom)}$

local wake-up

UJA1023 enters Low Power Mode

UJA1023 enters Active Mode

undervoltage

power-on

$LIN < V_{THR}$ for $t > t_{to(rec)}$

$LIN > V_{THR}$ for $t > t_{to(dom)}$

——— Master controlled or automatic transition
- - - - - automatic transition

R_{LIN}: LIN slave termination: - $R_{pu(slave)}$(typ. 30kOhm)
- I_{pu}(typ. 60μA)
Tx: Transmitter
V_{THR}: LIN receiver threshold: $V_{th(dom)}$(1) < V_{THR} < $V_{th(rec)}$(1)

010aaa190

Fig 27. State diagram of the LIN transceiver

4.1.1 Active mode of LIN transceiver

The Active mode is used for transmitting and receiving data via LIN. In this mode the LIN slave termination resistor $R_{pu(slave)}$ (see Ref. 1) is active.

4.1.2 Off-line mode of LIN transceiver

In Off-line mode the LIN transmitter is disabled and the LIN receiver monitors the LIN wire for wake-up events and LIN to ground short circuit failures. Instead of $R_{pu(slave)}$ (see Ref. 1) during Off-line mode pulls the current source I_{pu} (see Ref. 1) on the LIN bus to BAT.

4.1.3 Failsilent mode of LIN transceiver

The Failsilent mode observes the LIN wire for failure recovery. It is entered when the LIN wire is shorted to ground for more than the bus dominant time-out $t_{to(dom)}$ (see Ref. 1), and it is quiet when the LIN bus is recessive for more than bus recessive time-out $t_{to(rec)}$ (see Ref. 1). Beside the LIN transmitter, LIN bus termination is also switched off: i.e. neither the LIN slave termination resistor $R_{pu(slave)}$ (see Ref. 1) nor the pull-up current source I_{pu} (see Ref. 1) are active.

4.2 LIN failure diagnosis

The UJA1023 distinguishes between the following two failures on its LIN interface:

- LIN is clamped dominant, e.g. due to a short circuit between the LIN wire and GND.
- LIN is clamped recessive, e.g. due to a short circuit between the LIN wire and the battery.

4.2.1 LIN bus is clamped dominant

If LIN is shorted to GND the LIN transceiver automatically changes to the Failsilent mode. In Failsilent mode the LIN bus is floated in order to limit power consumption while the system is in its LOW-power mode. This failure is detected if the LIN bus wire is shorted to ground for more than $t_{to(dom)}$ (see Ref. 1). LIN bus communication is disabled.

If the bus wire becomes recessive for longer than $t_{to(rec)}$ (see Ref. 1) the current source I_{pu} (see Ref. 1) is enabled and pulls the LIN bus to the recessive state. Additionally each time the Active mode of LIN is entered the strong LIN slave termination resistor $R_{pu(slave)}$ (see Ref. 1) becomes active again.

4.2.2 LIN bus is clamped recessive

The LIN Bus is clamped recessive if the LIN bus-wire is shorted to the battery supply voltage. This failure is detected indirectly when the LIN line remains recessive for longer than the bus idle time-out time $t_{to(idle)}$ (see Ref. 1). In this case the UJA1023 enters the LOW-power Off-line mode.

4.2.3 Wake-up via LIN

The UJA1023 can be woken up via LIN while the LIN transceiver is in the Off-line mode. The LIN wake-up (see Ref. 2) is specified as a dominant state for 250 μs to 5 ms. A LIN wake-up is detected when the LIN bus becomes dominant for more than $t_{wake(bus)}$ (see Ref. 1) followed by a recessive transition on the LIN bus as depicted in Figure 28.
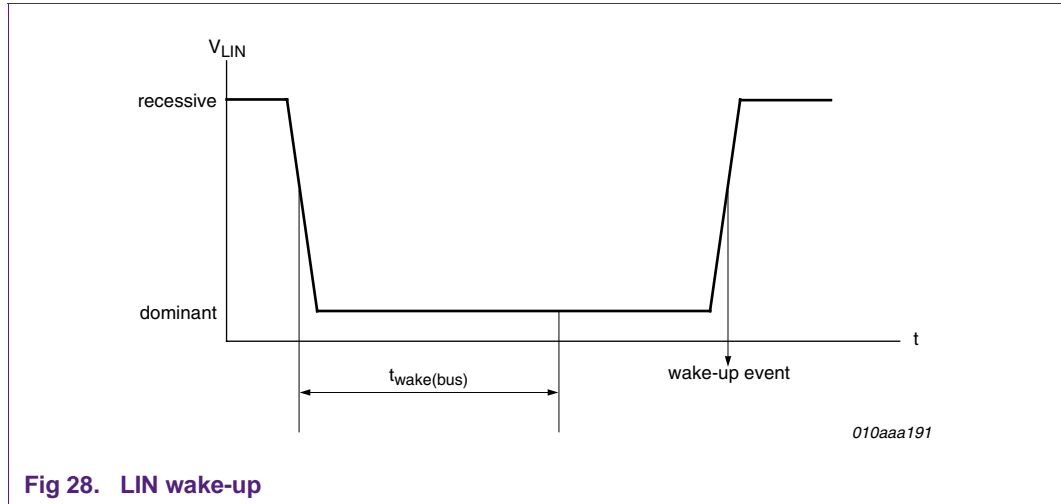
Fig 28. LIN wake-up

5. ESD aspects

5.1 ESD on LIN bus

5.1.1 General design hints for ESD

The on-chip ESD protection of pin LIN of the UJA1023 is designed to withstand $V_{esd(LIN)} = \pm 8$ kV (see Ref. 1) according to the Human Body Model (HBM) JESD22 A114 B (100 pF / 1.5 kΩ) and $V_{esd} = \pm 4$ kV according to IEC 61000-4-2 (150 pF / 300 Ω) (see Ref. 9). External ESD protection on the LIN bus connection is recommended if the UJA1023 is subjected to higher ESD pulses. Figure 29 shows a set-up for such external ESD protection.

The clamping voltage V_{CL} of the ESD protection diodes should be chosen above the maximum battery voltage in order to prevent damage if the LIN bus line is shorted to the battery line. Furthermore, the positive clamping voltage $V_{CL(pos)}$ should be below the maximum LIN bus voltage $V_{LIN(max)} = 40$ V (see Ref. 1) and the negative clamping voltage $V_{CL(neg)}$ should be above the minimal LIN bus voltage $V_{LIN(min)} = -27$ V (see Ref. 1).

According to the LIN Specification, rev. 2.0 (see Ref. 2), the LIN slave node capacitance shall be less than $C_{SLAVE(max)} = 250$ pF to ground. Together with the inherent capacitance of an ESD protection device (e.g. suppressor diode $P_{ESD1LIN}$ (see Ref. 10)) this requirement (< 250 pF) must be fulfilled.

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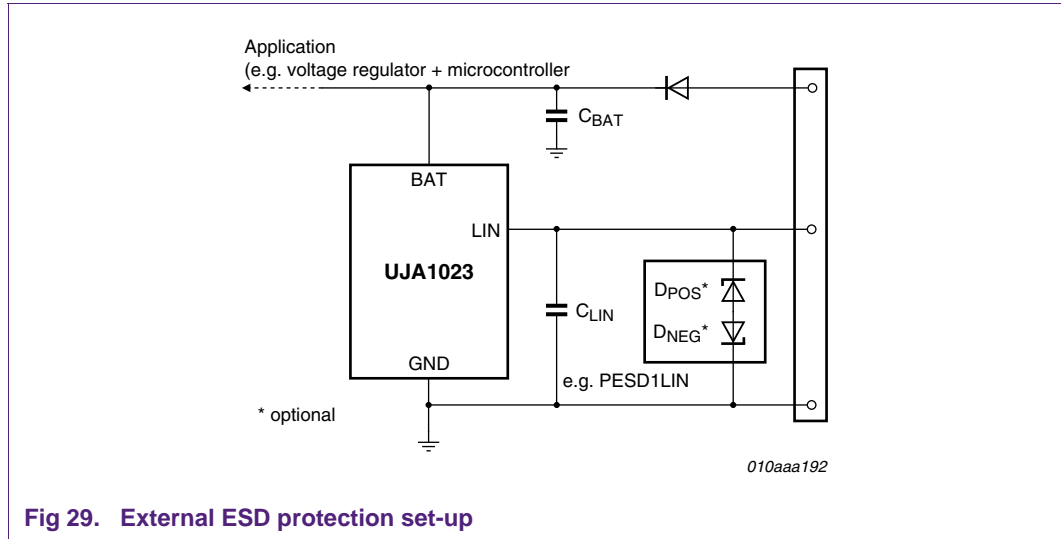
Fig 29. External ESD protection set-up

The suppressor diodes D_{POS} and D_{NEG} and the LIN node capacitor C_{LIN} should be placed as close as possible to the position where the highest ESD injection risk occurs. Typically, connectors represent the highest possibility for ESD injection.

5.1.2 ESD test results

The test house IBEE (see Ref. 7) has tested the ESD robustness of the UJA1023 according to the LIN EMC Test Specification (see Ref. 6). The ESD test results are shown in Table 12.

Table 12.   ESD test results

Applied components				V_{ESD} (see Ref. 9)	Reference
C_{BAT}	C_{LIN}	$D_{POS/MNEG}$	L_{FERRIT}[1]		
100 nF	-	-	-	± 5.0 kV	Ref. 7
100 nF	220 pF	-	-	± 4.0 kV	Ref. 7
100 nF	220 pF	$P_{ESD1LIN}$	-	± 11.0 kV	Ref. 7
100 nF	220 pF	$P_{ESD1LIN}$	MMBZ2012Y202B	> 15.0 kV	Ref. 7

[1] The ferrite LFERRITE was connected in series and placed between the PESD1LIN and the LIN pin of the UJA1023.

5.2 ESD on configuration pins C1 to C3

The configuration pins might be connected to an ECU plug. This is normal for a daisy chain configuration. Thus the ESD risk can be as high as that on the LIN bus.

The on-chip ESD protection on C1 to C3 is similar to the protection of the LIN bus. They are designed to withstand $V_{esd(Cx)} = \pm 8$ kV (see Ref. 1) according to the human body model JESD22 A114 B (100 pF / 1.5 kΩ). Hence, on C1 to C3 the same external ESD protection is recommended as shown in Figure 29 if the configuration pins of the UJA1023 are subjected to higher ESD pulses.

AN10704_1

Application note **Rev. 01 — 6 April 2009** **32 of 36**

5.3 ESD on I/O pins P0 to P7

The on-chip ESD protection of the I/O pins P0 to P7 are designed to withstand $V_{esd(other)} = \pm 2$ kV (see Ref. 1) according to the human body model JESD22 A114 B (100 pF / 1.5 kΩ). If the I/O pins are subjected to higher ESD pulses an external protection is recommended.

For common I/O applications a series resistor is sufficient. ESD tests (see Ref. 7) with a series resistor of 5.6 kΩ on one I/O pin have shown robustness against ESD of more[1] than ± 6 kV according to IEC 61000-4-2 (150 pF / 300 Ω) (see Ref. 9).

Alternatively, if a series resistor cannot be applied, an external ESD protection diode and/or ferrite can be used.

6. Abbreviations

Table 13. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
BFByte	Field of the LIN frame
CS	Checksum field of the LIN frame
CAN	Control Area Network
DAC	Digital-to-Analog Converter
ECU	Electronic Control Unit
EMC	Electro-Magnetic Compatibility
ESD	Electrostatic discharge
IF	Identifier Field of the LIN frame
LED	Light Emitting Diode
LIN	Local Interconnect Network
MR	Master Request LIN command
MUX	Multiplexer
NAD	Node Address of a LIN slave
nRSID	negative Response Service Identifier
PCB	Printed-Circuit Board
PCI	Protocol Control Information
PDU	Packet Data Unit
pRSID	positive Response Service Identifier
RSID	Response Service Identifier
SB	Synchronization Break of the LIN frame
SCI	Serial Communications Interface
SF	Synchronization Field of the LIN frame
SID	Service Identifier
SR	Slave Response LIN command
UART	Universal Asynchronous Receiver/Transmitter

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1. Only evaluation up to the given value was possible.

7. References

[1]   Product Data Sheet UJA1023, LIN I/O Slave, Philips Semiconductors, Jul. 2006.

[2]   LIN Specification Package Revision 2.0, LIN Consortium, Sep. 2003.

[3]   International Standard ISO 9141, Road Vehicles - Diagnostic Systems - Requirement for Interchange of Digital Information, International Standardization Organization, 1989.

[4]   Technical Report TR0363, The LIN 2.0 Physical Layer, Philips Semiconductors, Sep. 2004.

[5]   SAE International J2602-1, LIN Network for Vehicle Applications, Sep. 2005.

[6]   LIN Conformance Test Specification, LIN EMC Test Specification, Version 1.0, Aug. 2004.

[7]   UJA1023 - EMC Test Report (Nr. 01-01-06) IBEE Zwickau, Jan. 2006.

[8]   UJA1023 - EMC Test Report (Nr. 02-01-06) IBEE Zwickau, Jan. 2006.

[9]   International Standard IEC 61000-4-2, Electromagnetic Compatibility - Testing and Measurement Techniques - Electrostatic Discharge Immunity Test, International Electrotechnical Commission, 2001.

[10] Data Sheet PESD1LIN, LIN Bus ESD Protection Diode, Philips Semiconductors, Oct. 2004.

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9.　Contents