AN10211

TJA1040 high speed CAN transceiver

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Document information

Info	Content
Keywords	Controller Area Network (CAN), ISO11898, Transceiver, Physical Layer, TJA1040, TJA1041, TJA1050, PCA82C250/C251
Abstract	The TJA1040 is an advanced high speed CAN transceiver for use in automotive and general industrial applications. It supports the differential bus signal representation described in the international standard for in-vehicle high speed CAN applications (ISO11898). CAN (Controller Area Network) is the standard protocol for serial in-vehicle bus communication, particularly for Engine Management and Body Multiplexing. The TJA1040 provides a Standby mode, as known from its functional predecessors PCA82C250 and PCA82C251, but with significantly reduced power consumption. Besides the excellent low-power behavior the TJA1040 offers several valuable system improvements. Highlights are the absolute passive bus behavior if the device is unpowered as well as the excellent EMC performance.

Revision history

Rev	Date	Description
02	20061110	Updated version • The format of this application note has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Update of Section 5.2.1 “Common mode choke”. • Update of Section 5.2.3 “ESD protection”. • Update of Section 6 “Pin FMEA”.
01	20030221	Initial version

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1. Introduction

The high speed CAN transceiver TJA1040 Ref. 1 from NXP Semiconductors provides the physical link between the protocol controller and the physical transmission medium according to ISO11898 (Ref. 2 , Ref. 3 and Ref. 4) and SAE J2284 Ref. 5. This ensures interoperability with other ISO11898 compliant transceiver products.

Since the TJA1040 is based on the same technology as the high speed CAN transceiver TJA1050 Ref. 6 it is processed in the advanced Silicon-on-Insulator (SOI) technology. Compared to its functional predecessors PCA82C250 (C250) Ref. 7 and PCA82C251 (C251) Ref. 8 the TJA1040 shows a reduction of about 20 dB in electromagnetic emission (EME). Additionally the electromagnetic immunity (EMI) has improved significantly.

Besides electromagnetic compatibility (EMC), another key feature of the TJA1040 is its Standby mode. This mode provides a very low current consumption (less than 15 μA) and remote wake-up capability via the CAN bus lines using a differential wake-up receiver. This makes the TJA1040 the preferred transceiver for applications, which keep the microcontroller and the applications V_{CC} always active. Moreover the TJA1040 offers ideal passive behavior when unpowered. It is completely invisible to the bus if the V_{CC} supply of the transceiver is switched off. This feature is of main interest for ignition key controlled nodes (clamp-15), which are unpowered completely when the ignition key is turned off while other ECUs continue communication (partial networking).

The TJA1040 is available without packaging (bare die) as well as in an SO8 package as shown in Figure 1. It is pin compatible with other high speed CAN transceivers from NXP Semiconductors like the C250, C251, TJA1050 and the TJA1041 Ref. 9 with the upper part of its SO14 pinning.

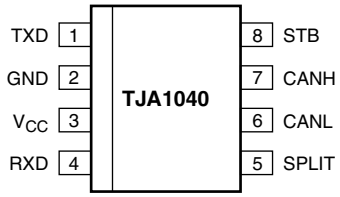


Fig 1. Pinning diagram of the TJA1040

2. General high speed CAN application

Figure 2 illustrates a general high speed CAN application. Several ECUs (Electronic Control Units) are connected via stubs to a linear bus topology. Each bus end is terminated with 120 Ω (R_T), resulting in the nominal 60 Ω bus load according to ISO11898. The figure shows the split termination concept, which is helpful when improving the EMC of high speed CAN bus systems Ref. 10. The former single 120 Ω termination resistor is split into two resistors of half value ($R_T/2$) with the center tap connected to ground via the capacitor C_{spl}.

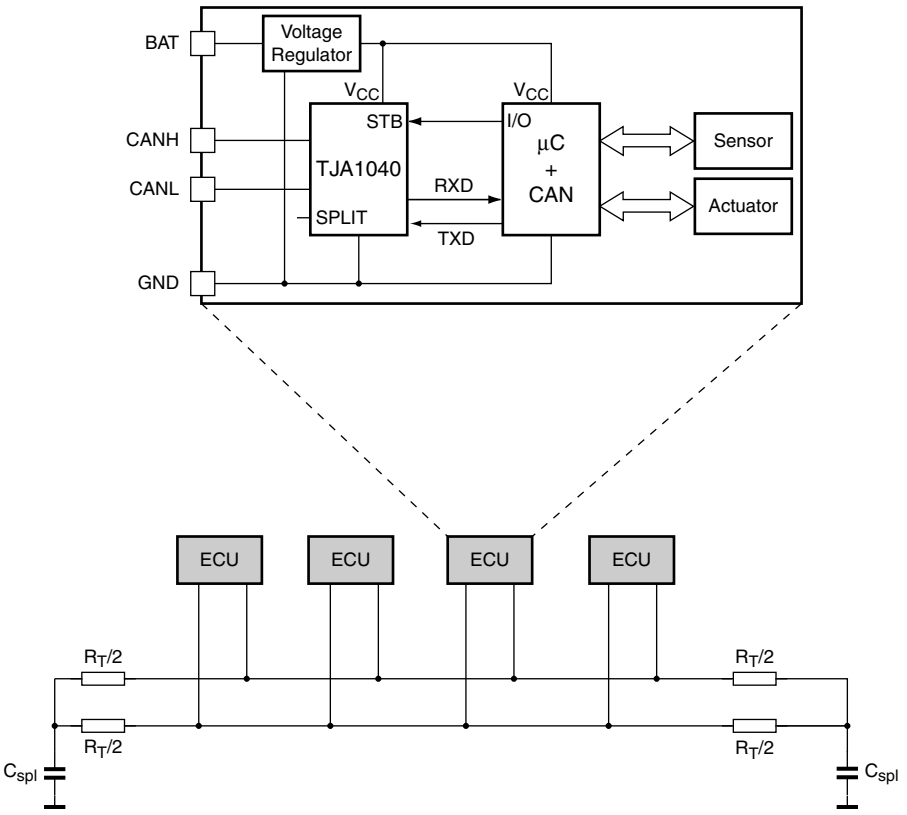


Fig 2. High speed CAN application

The block diagram in Figure 2 describes the internal structure of an ECU. Typically, an ECU consists of a stand-alone transceiver (here TJA1040) and a host microcontroller with integrated CAN-controller, which are supplied by a voltage regulator. While the high speed CAN transceiver needs a +5 V supply voltage to support the ISO11898 bus levels, new microcontroller products are increasingly using lower supply voltages like 3.3 V. In this case a dedicated 3.3 V voltage regulator is necessary for the microcontroller supply. The protocol controller is connected to the transceiver via a serial data output line (TXD) and a serial data input line (RXD). The transceiver is attached to the bus lines via its two bus terminals CANH and CANL, which provide differential receive and transmit capability. In the case of the TJA1040 the pin STB is connected to an I/O pin of the host microcontroller for operation mode control. The split termination approach can be further improved using the pin SPLIT for DC stabilization of the common mode voltage Section 4.4.

The protocol controller outputs a serial transmit data stream to the TXD input of the transceiver. An internal pull-up function within the TJA1040 sets the TXD input to logic HIGH, which means that the bus output driver stays recessive in the case of a TXD open circuit condition. In the recessive state (see Figure 3) the CANH and CANL pins are biased to a voltage level of $V_{CC}/2$. If a logic LOW level is applied to TXD, the output stage is activated, generating a dominant state on the bus line (see Figure 3). The output driver CANH provides a source output from V_{CC} and the output driver CANL a sink output towards GND. This is illustrated in Figure 4 showing the block diagram of the TJA1040.

If no bus node transmits a dominant bit, the bus stays in recessive state. If one or multiple bus nodes transmit a dominant bit, then the bus lines enter the dominant state overriding the recessive state (wired-AND characteristic).

The receiver converts the differential bus signal into a logic level signal, which is output at RXD. The serial receive data stream is provided to the bus protocol controller for decoding. The internal receiver comparator is always active. It monitors the bus while the bus node is transmitting a message. This is required to support the non-destructive bit-by-bit arbitration scheme of CAN.

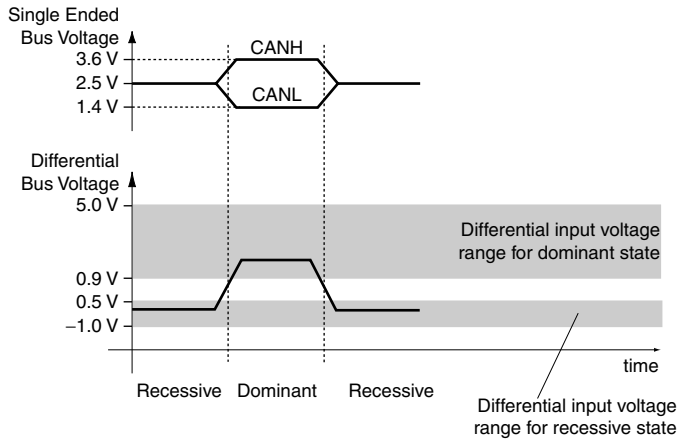


Fig 3. Nominal bus levels according to ISO11898

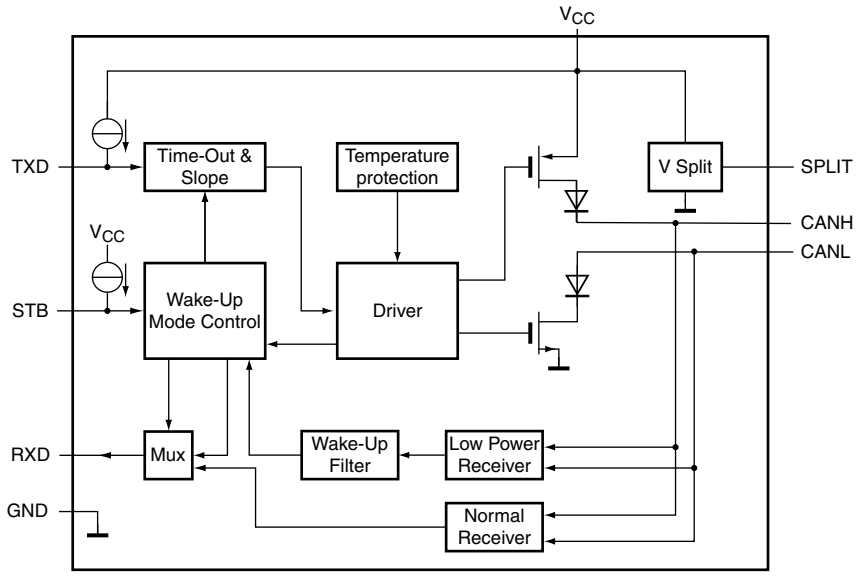


Fig 4. Block diagram of the TJA1040

3. Application specific requirements on high speed CAN

In-vehicle high speed CAN networks come with different requirements, depending on the implemented application. First of all, high speed CAN is the ideal choice for all applications which require a high data throughput (up to 1 Mbit/s). Though from the ECU power management point of view, four different application areas (Type A - D) for high speed CAN can be distinguished, as illustrated in Figure 5.

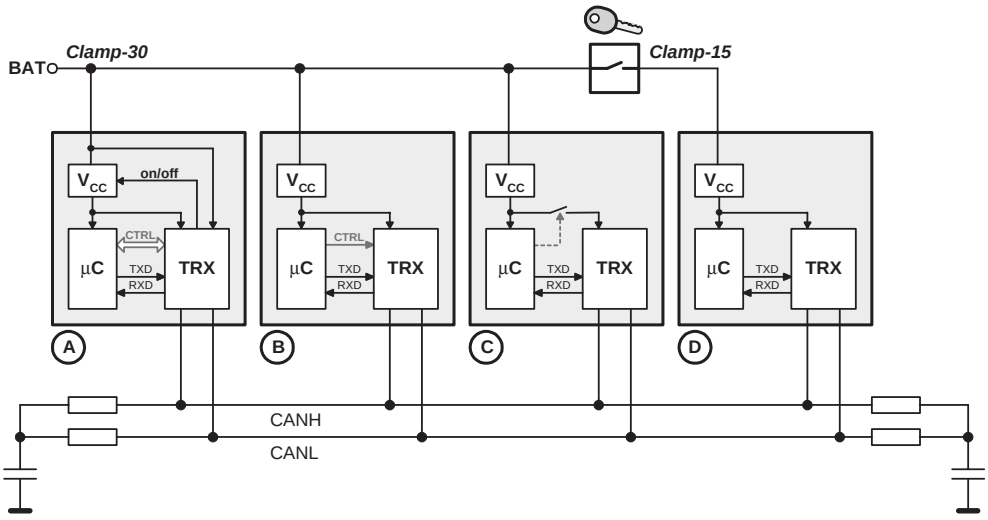


Fig 5. Different application areas for high speed CAN

Type A — Applications which have to be available all the time, even when the car is parked and the ignition-key is off, are permanently supplied from a battery supply line, called Clamp-30. However, those nodes need the possibility to reduce the current consumption for saving the battery load by controlling the local ECU supply (V_{CC}). These type A applications make it possible to switch off the entire supply system of the ECU including the microcontroller supply while keeping the wake-up capability via CAN.

Type B — Those nodes of applications, which need an always-active microcontroller, are permanently supplied from the battery supply line Clamp-30 using a continuously active V_{CC} supply. To reduce the ECU power consumption, the transceiver needs to be set into a mode with reduced supply current while V_{CC} stays active.

Type C — Dedicated applications that need an always-active microcontroller and therefore are permanently supplied from the Clamp-30 line. In contrast to type B applications, further current can be saved, because the transceiver can become completely unpowered by microcontroller control. These applications require absolute passive bus behavior of the transceiver, while its voltage supply is inactive. This is needed in order not to affect the remaining bus system, which might continue communication.

Type D — Applications, which do not need to be available with ignition-key off, are in that case simply switched off and become totally unpowered. They are supplied from a switched battery supply line, called Clamp-15. This supply line is only active with ignition-key on. Depending on system requirements, e.g. partial communication of the still supplied nodes during ignition-key off, these unpowered nodes need to behave passively towards the remaining bus, similar to type C applications.

The NXP Semiconductors transceiver products TJA1040, TJA1041 and TJA1050 (see also Section 10.1) offer different features to completely cover the described power management requirements.

3.1 Type A applications

The TJA1041 can be put into a Sleep mode (all V_{CC} supplies off), which allows reducing the total current consumption of the entire ECU to typically 20 μA, while keeping the capability to receive wake-up events from the bus and to restart the application. The TJA1041 can take control over the ECU internal power supply and wake-up requests. It is the first choice transceiver for applications of type A, which need to be remotely available all the time.

3.2 Type B applications

Type B applications require a dedicated transceiver operation mode with reduced current consumption, while V_{CC} stays active all the time. The TJA1040 with its Standby mode offers the best choice for these applications. During Standby mode the device reduces the V_{CC} supply current to a minimum in order to save current. In spite of the very low current consumption, the TJA1040 still monitors the CAN bus lines for bus traffic and allows waking up the host microcontroller.

3.3 Type C and D applications

Within these applications, the supply voltage of the transceiver is directly controlled by the host microcontroller or the ignition key. The transceiver does not necessarily need to provide a dedicated mode with reduced power consumption. Most important is a passive behavior of the transceiver, when unpowered. Parasitic currents within the ECU towards the microcontroller as well as towards the bus lines have to be avoided. Depending on the systems CAN bus requirements, the TJA1040 as well as the TJA1050 support this kind of application.

If there is further bus communication of other CAN ECUs present, while the type C application transceiver is switched off (partial networking), the TJA1040 is the first choice. This is because of the perfect floating behavior on the bus lines while V_{CC} is off. The remaining bus system will not be affected by any unpowered TJA1040.

If there is no ongoing communication (no partial networking), the TJA1050 offers a comparable alternative. In contrast to the TJA1040, the unpowered TJA1050 affects a running bus communication due to a small reverse bus current. This slightly increases the electromagnetic emission during partial networking time. But if there is no ongoing communication, the TJA1050 achieves the same performance as the TJA1040.

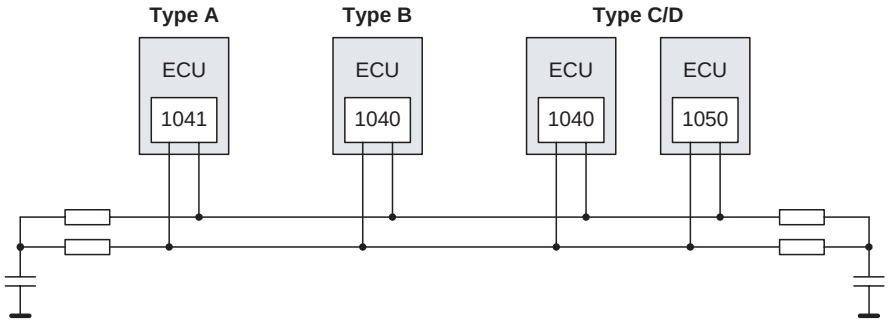


Fig 6. Application areas for the TJA1040, TJA1041 and TJA1050

4. Main features of the TJA1040

4.1 Operation modes

The TJA1040 provides two different operation modes: Normal mode and Standby mode. Similar to the C250 and C251 transceivers, a dedicated pin selects the actual operation mode.

4.1.1 Normal mode

During normal CAN communication, the Normal mode is selected by applying a LOW level to the pin STB. In this mode the transceiver can transmit and receive data via the bus lines CANH and CANL. The digital bit stream input at TXD is converted into the corresponding analog bus signals. Simultaneously, the Normal Receiver (see Figure 4) converts the analog data on the bus lines into a digital bit stream, which is output to RXD via the internal multiplexer. In Normal mode the bus lines are biased to $V_{CC}/2$ and the transmitter is enabled.

4.1.2 Standby mode

The Standby mode with significantly reduced current consumption is activated with a HIGH level applied to pin STB. In Standby mode the transmitter and receiver of the TJA1040 are switched off and therefore are not capable of transmitting and receiving regular CAN messages. However, a Low Power Receiver (see Figure 4) monitors the bus lines for CAN messages. Only dominant CAN states, which are stable longer than the bus wake-up time t_{BUS} Ref. 1, and therefore indicate bus traffic, are reflected to the pin RXD by a logic LOW level (wake-up detected). This offers a maximum electromagnetic immunity against unwanted wake-up events. To enter the Normal mode after the wake-up detection a LOW level has to be applied to the pin STB. Entering Normal mode activates the Normal Receiver of the TJA1040 again.

Table 1. Operation modes of the TJA1040

Operation mode	STB	Bus Bias	RXD information	
			RXD = LOW	RXD = HIGH
Normal	LOW	$V_{CC}/2$	Bus dominant	Bus recessive
Standby	HIGH	Ground	Wake-up detected	No wake-up detected

4.2 Excellent EMC behavior

Electromagnetic compatibility has been one main design target of the TJA1040. During Normal mode a precondition for a low electromagnetic emission in the critical AM-band is a very good symmetry of the signals CANH and CANL, when switching between the dominant and recessive levels and vice versa. In the TJA1040 design, this symmetry is optimised by using a fixed slope function instead of a variable one, known from the C250/C251. Based on the fixed and optimised slope time, the emission could be decreased by more than 20 dB compared to the C250/C251, especially if the split termination approach is used. If a specific system implementation needs further reduction of the emission and enhancement of immunity in the FM-band, it is possible to add a common mode choke externally to the bus pins CANH and CANL.

4.3 Passive behavior

In up to date in-vehicle networks partial networking is widely implemented. In Section 3 partial networking is introduced with different applications. In these typical example applications, some transceivers can become unpowered (e.g. Clamp-15 nodes) while other transceivers are continuously supplied (e.g. Clamp-30 nodes). In such networks the TJA1040 is favoured for those applications, which are partly unpowered, because of its excellent passive behavior to the bus when the V_{CC} supply is switched off. In addition, the TJA1040 is protected against reverse currents via the pins TXD, RXD and STB. There will be no backward current via those pins if the accompanying microcontroller is still supplied.

4.4 Common mode stabilization, SPLIT pin

The high impedance characteristic of the bus during recessive state leaves the bus vulnerable to even small leakage currents, which may occur with unpowered transceivers or ECUs within the bus system. As a result the common mode voltage can show a significant voltage drop from the nominal $V_{CC}/2$ value. After transmitting the first dominant bit of a CAN frame (Start-of-Frame Bit) the common mode voltage would restore to its nominal value. This would lead to a large common mode step and an increased emission. The TJA1040 provides a common mode stabilization by offering a voltage source of nominal $V_{CC}/2$ at the pin SPLIT (Figure 7). The common mode stabilization improves the EMC performance of the TJA1040 significantly. Its use is recommended if there are unpowered nodes while other nodes keep communicating.

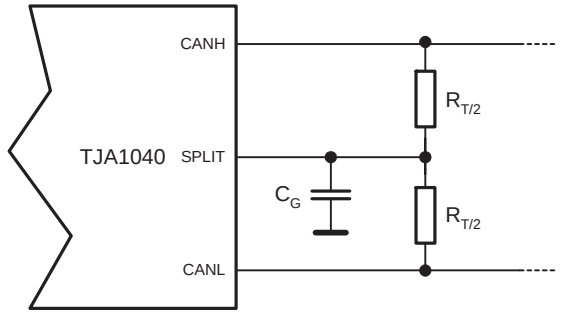


Fig 7. Common mode stabilization with SPLIT pin

4.5 Interfacing to microcontroller with non 5V supply

As the TJA1040 supports the physical layer of the ISO11898 standard, it requires a +5 V supply voltage as reference voltage. On the other hand, new microcontroller generations often require supply voltages lower than 5 V, mostly +3.3 V and less.

In order to support a microcontroller with low supply voltages, the TJA1040 provides a reduced input threshold voltage at its input pins TXD and STB. An input voltage of 2 V at these pins is safely interpreted as a HIGH level and allows a direct drive out of a 3 V microcontroller. It should be noticed that the output level of the TJA1040's pins towards the microcontroller is still based on the 5 V transceiver supply. TXD and STB provide an internal weak pull-up current source towards V_{CC} (fail-safe open circuit behavior) while RXD offers a push-pull driver stage, which drives the pin to V_{CC} in a recessive bus state.

Common 3 V microcontrollers tolerate voltages above their own supply voltage if the current is limited. Due to the weak and current limited pull-up source within TXD and STB, a direct connection between the 3 V microcontroller and the 5 V supplied TJA1040 is typically possible without further protection measures (please check the data sheet of the chosen microcontroller). Since RXD offers a strong driver towards V_{CC}, the RXD input of the microcontroller needs to be 5 V-tolerant. Alternatively a level shifter or a simple series resistor between RXD of the TJA1040 and the microcontroller could be used.

Take into account that any hardware between the transceiver's TXD/RXD interface and the microcontroller might lengthen the loop delay of the system, which has an impact on the overall bit timing parameters. Especially at very high bit rates ≥ 500 kBit/s, this parameter has to be checked carefully.

4.6 TXD dominant time-out function

The TJA1040 provides a TXD dominant time-out function, which prevents the bus lines from being clamped to a permanent dominant level and from blocking all network communication.

The function of the TXD dominant time-out is illustrated in Figure 8. After a maximum allowable TXD dominant time (t_{DOM}) the transmitter of the transceiver is disabled and releases the bus lines recessive again. The next dominant output drive is possible only after setting TXD to HIGH again. According to the CAN protocol a maximum of eleven successive dominant bits is allowed on TXD only (worst case of five successive dominant bits followed immediately by an error frame). Along with the minimum specified TXD dominant time-out (t_{DOM_min}), this limits the minimum suitable bit rate to 40 kbit/s.

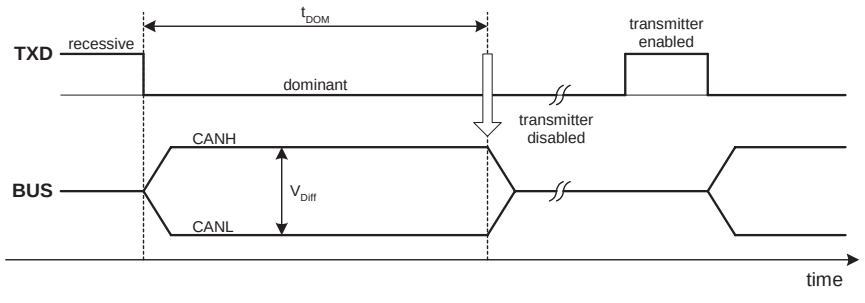
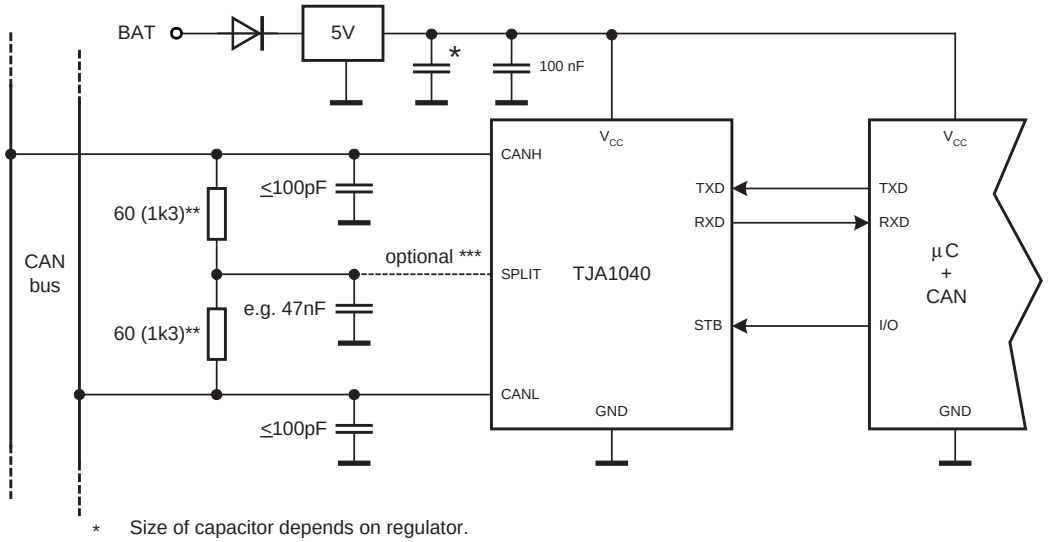


Fig 8. TXD dominant time-out feature

5. Hardware application

Besides the excellent behavior of the TJA1040 itself, a careful system implementation dealing with termination, topology and external circuitry is very important to make optimum use of the transceiver's advantages. This chapter presents a typical application example for the TJA1040 and application hints dealing with the split termination concept and required external circuitry.

Figure 9 shows how to integrate the TJA1040 within a typical application. In the example, a 5 V supplied host microcontroller is assumed. A dedicated 5 V regulator supplies the TJA1040 transceiver and the microcontroller. Two capacitors are placed at the output of the voltage regulator for V_{CC} supply buffering purposes. The CAN-controller of the microcontroller is connected to the transceiver via TXD and RXD. Pin STB is connected to an I/O pin of the host microcontroller for operation mode control. The CAN bus lines are attached via the two bus terminals CANH and CANL. In-between matching capacitors are placed and a typical split termination is shown to improve EMC performance.



* Size of capacitor depends on regulator.
** For stub nodes an optional "weak" termination improves the EMC behaviour of the system in terms of emission.
*** Optional common mode stabilization by a voltage source of VCC/2 at the pin SPLIT.

Fig 9. Typical application for the TJA1040 with a 5V microcontroller

5.1 Split termination concept

Practice has shown that effective reduction of electromagnetic emission can be achieved by a modified bus termination concept called split termination. In addition this concept contributes to higher immunity of the bus system. The split termination concept is illustrated in Figure 10. Basically each of the two termination resistors of the bus line end nodes is split into two resistors of equal value, i.e. two 60 Ω resistors instead of one 120 Ω resistor. It is common practice to include the termination within the ECU. Stub nodes, which are connected to the bus via stubs, can optionally be equipped with a similar split termination configuration. The resistor value for the stub nodes has to be chosen such that the busload of all the termination resistors stays within the range of 45 Ω to 65 Ω. As an example for up to 10 nodes (8 stub nodes and 2 bus line end nodes) a typical resistor value is 1.3 kΩ.

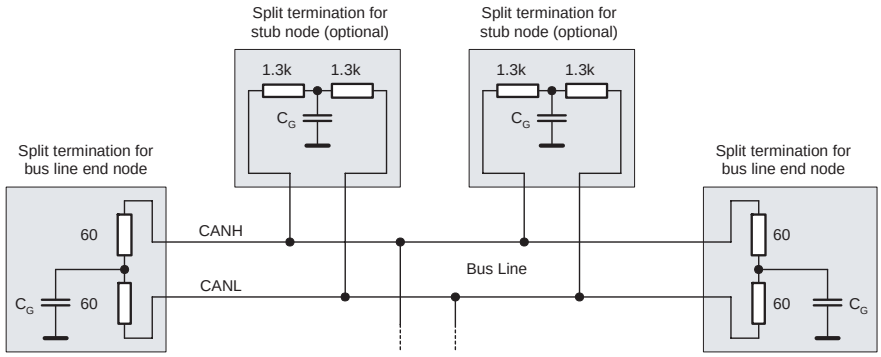


Fig 10. Typical split termination concept

5.2 Optional circuitry at CANH and CANL

The EMC performance of the TJA1040 has been optimized for use of the split termination without a choke. Hence, it is highly recommended to implement the split termination. The excellent output stage symmetry allows going without chokes as shown by different emission measurements. If, however, the system performance is still not sufficient, there is the option to use additional measures like common mode chokes, capacitors and ESD clamping diodes.

5.2.1 Common mode choke

A common mode choke provides high impedance for common mode signals and low impedance for differential signals. Due to this, common mode signals produced by RF noise and/or by non-perfect transceiver driver symmetry get effectively reduced while passing the choke. In fact, a common mode choke helps to reduce emission and to improve immunity against common mode disturbances.

Former transceiver devices usually needed a common mode choke to fulfil the stringent emission and immunity requirements of the automotive industry when using unshielded twisted-pair cable. The TJA1040 has the potential to build in-vehicle bus systems without chokes. Whether a choke is needed or not finally depends on the specific system implementation like the wiring harness and the symmetry of the two bus lines (matching tolerances of resistors and capacitors).

Besides the RF noise reduction the stray inductance (non-coupled portion of inductance) may establish a resonant circuit together with pin capacitance. This can result in unwanted oscillations between the bus pins and the choke, both for differential and common mode signals, and in extra emission around the resonant frequency. To avoid such oscillations, it is highly recommended to use only chokes with a stray inductance lower than 500 nH. Bifilar wound chokes typically show an even lower stray inductance. Figure 11 shows an application, using a common mode choke. As shown the choke shall be placed nearest to the transceiver bus pins.

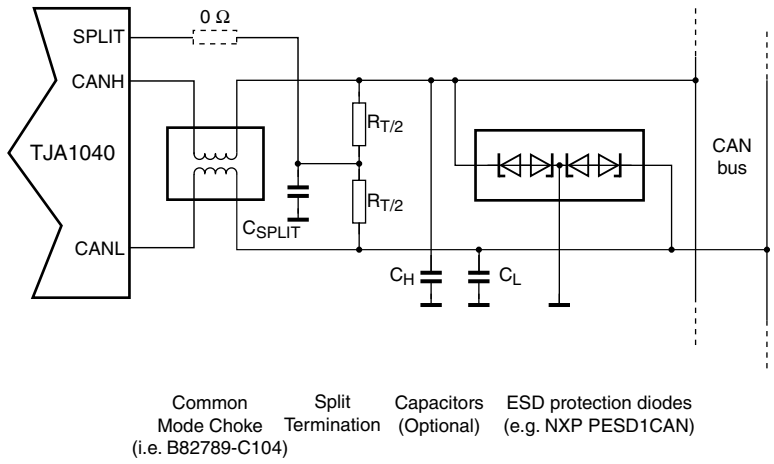


Fig 11. Optional circuitry at CANH and CANL

5.2.2 Capacitors

Matching capacitors (in pairs) at CANH and CANL to GND (C_H and C_L) are frequently used to enhance immunity against electromagnetic interferences. Along with the impedance of corresponding noise sources (RF), capacitors at CANH and CANL to GND form an RC low-pass filter. Regarding immunity, the capacitor value should be as large as possible to achieve a low corner frequency. The overall capacitive load and impedance of the output stage establish an RC low-pass filter for the data signals. The associated corner frequency must be well above the data transmission frequency. This results in a limit for the capacitor value depending on the number of nodes and the data transmission frequency. Notice that capacitors increase the signal loop delay due to reducing rise and fall times. Due to that, bit timing requirements, especially at 500 kbit/s, call for a value of lower than 100 pF (see also SAE J2284 and ISO11898). At a bit rate of 125 kbit/s the capacitor value should not exceed 470 pF. Typically, the capacitors are placed between the common mode choke (if applied at all) and the ESD clamping diodes as shown in Figure 11.

5.2.3 ESD protection

The TJA1040 is designed to withstand ESD pulses of up to 6 kV according to the human body model at the bus pins CANH, CANL and pin SPLIT and thus typically does not need further external protection methods. Nevertheless, if much higher protection is required, external clamping devices can be applied to the CANH and CANL lines.

NXP offers a dedicated protection device for the CAN bus, providing high robustness against ESD and automotive transients. The PESD1CAN ESD protection diode Ref. 13, featuring a very fast diode structure with very low capacitance (typ. 11 pF), is compliant to IEC61000-4-2 (level 4), thus allowing air and contact discharge of more than 15 kV and 8 kV, respectively. Tests at an independent test house have confirmed typically more than 20 kV ESD robustness for ECUs equipped with the PESD1CAN diode and a common mode choke. To be most effective the PESD1CAN diode shall be placed close to the ECU connector as shown in Figure 11.

5.3 Buffering at V_{CC}

The voltage supply via the pin V_{CC} provides the current needed for the transmitter and receiver of the TJA1040. The voltage regulator for the supply must be able to deliver a current of 71 mA on average. Using a linear voltage regulator, it is recommended to stabilize the output voltage with a bypass capacitor of about 22 μF. As illustrated in Figure 9 this capacitor should be connected at the output of the voltage regulator.

An additional capacitor in the range 47 nF to 100 nF should be connected between V_{CC} and GND close to the transceiver. Its function is to buffer the V_{CC} supply voltage. For reliability reasons it might be useful to apply two capacitors in series connection between V_{CC} and GND. Thus, a single shorted capacitor cannot short-circuit the V_{CC} supply.

5.4 Optional circuitry at TXD and RXD

Depending on the used microcontroller and PCB layout, the digital signals at TXD and RXD during bit transitions might degrade the system EMC performance. Here a series resistor of about 1 kΩ within the TXD and/or RXD line could be an option to reduce the electromagnetic emission of the system. Along with the pin capacitance this would help to smooth the edges to some degree. For high bus speeds (≥ 500 kbit/s) the additional delay within TXD and RXD has to be taken into account.

6. Pin FMEA

This chapter provides an FMEA (Failure mode and Effects Analysis) for typical failure situations, when dedicated pins of the TJA1040 are short-circuited to supply voltages like V_{BAT}, V_{CC}, GND or to neighbored pins or are simply left open. The individual failures are classified, due to their corresponding effects on the transceiver and bus communication in Table 2.

Table 2. Classification of failure effects

Class	Effects
A	Damage to transceiver Bus may be affected
B	No damage to transceiver No bus communication possible
C	No damage to transceiver Bus communication possible Corrupted node not able to communicate
D	No damage to transceiver Bus communication possible Reduced functionality of transceiver

Table 3, Table 4 and Table 5 show the FMEA matrix with the failure classifications and additional remarks on failure effects:

Table 3. FMEA matrix for pin short-circuits between neighbored pins

Pin	Short to V_{BAT} (12V … 40V)		Short to V_{CC} (5V)	
	Class	Remark	Class	Remark
(1) TXD	A	Limiting value exceeded	C	TXD clamped recessive; node eventually goes Bus-Off
(2) GND	C	Node is left unpowered	C	Transceiver is left unpowered
(3) VCC	A	Limiting value exceeded	---	---
(4) RXD	A	Limiting value exceeded	C	RXD is clamped recessive and CAN controller expects an idle bus; node produces Error Frames on bus until Bus-Off is entered; communication continuously disturbed due to random communication trials of shorted node
(5) SPLIT	D	Bus charged to V_{BAT} - level; bit timing problem possible	D	Bus charged to V_{CC} - level; bit timing problem possible
(6) CANL	B	No bus communication	B	No bus communication
(7) CANH	D	Degradation of EMC; bit timing problem possible	D	Degradation of EMC; bit timing problem possible
(8) STB	A	Limiting value exceeded	C	Transceiver permanent in Standby mode (transmitter disabled)

Table 4. FMEA matrix for pin short-circuits to GND and open pins

Pin	Short to ground		Open	
	Class	Remark	Class	Remark
(1) TXD	C	TXD dominant clamping; transmitter disabled; node eventually goes Bus-Off	C	TXD clamped recessive; node eventually goes Bus-Off
(2) GND	---	---	C	Transceiver is left unpowered and behaves passive to the bus lines
(3) VCC	C	Transceiver is left unpowered and behaves passive to the bus lines	C	Transceiver is left unpowered; no V_{CC} reverse supply from mC to transceiver
(4) RXD	C	RXD clamped dominant	C	Node may produce Error Frames on bus until Bus-Off is entered
(5) SPLIT	D	Bus discharged to GND - level; bit timing problem possible	D	No DC common mode stabilization
(6) CANL	D	Degradation of EMC; bit timing problem possible	C	Receiving from bus possible only, if there is no termination resistor within this interrupted bus segment present; transmitting across the interruption is not possible
(7) CANH	B	No bus communication	C	Receiving from bus possible only, if there is no termination resistor within this interrupted bus segment present; transmitting across the interruption is not possible
(8) STB	D	Transceiver permanent in Normal mode	C	Transceiver permanent in Standby mode (transmitter disabled)

Table 5. FMEA matrix for pin short-circuits between neighbored pins

Pin short	Short to neighboured pin	
	Class	Remark
TXD-GND	C	Transmitter disabled after TXD Dominant Timeout
GND-V_{CC}	C	TRX unpowered, bus not affected
V_{CC}-RXD	C	RXD is clamped recessive, bus communication disturbed
SPLIT-CANL	D	Degradation of EMC
CANL-CANH	B	No bus communication, bus clamped recessive
CANH-STB	D	Transceiver is not able to enter Standby mode if the bus is driven dominant

7. Bus network aspects

This chapter deals with items like the maximum number of nodes, the maximum bus line length and topology aspects. In particular the topology appears to have a significant influence on the system performance.

7.1 Maximum number of nodes

The number of nodes which can be connected to a bus depends on the minimum load resistance a transceiver can drive. The TJA1040 transceiver provides an output drive capability down to a minimum load of $R_{L,min}$ = 45 Ω for V_{CC} > 4.75 V. The overall busload is defined by the termination resistance R_T, the bus line resistance R_W and the transceiver's differential input resistance R_{diff}. The DC circuit model of a bus system is shown in Figure 12. For worst case consideration the bus line resistance R_W is considered to be zero. This leads to the following relations for calculating the maximum number of nodes:

$$\frac{R_{T.min} \times R_{diff.min}}{n_{max} \times R_{T.min} + 2R_{diff.min}} > R_{L.min} \quad (1)$$

Rearranged to n_{max} :

$$n_{max} < R_{diff.min} \times \left(\frac{1}{R_{L.min}} - \frac{2}{R_{T.min}}\right) \quad (2)$$

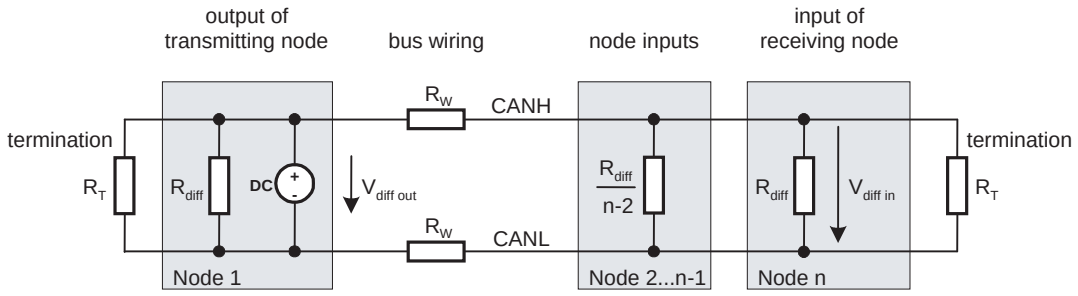


Fig 12. DC circuit model for a bus system according to ISO11898

Table 6 gives the maximum number of nodes for two different termination resistances. Notice that connecting a large number of nodes requires relatively large termination resistances.

Table 6. Maximum number of nodes (see datasheets for $R_{diff,\ min}$ and $R_{L,min}$)

Transceiver	$R_{diff,min}$(kΩ)	$R_{L,min}$(Ω)	Nodes (maximum) ($R_{T,min}$=118 Ω)	Nodes (maximum) ($R_{T,min}$=130 Ω)
TJA1040 TJA1041 TJA1050	25	45 @ V_{CC}=4.75 V	131	170
C250 C251	20	45 @ V_{CC}=4.9 V	105	136

7.2 Maximum bus line length

The maximum achievable bus line length in a CAN network is determined essentially by the following physical effects:

1. Loop delays of the connected bus nodes (CAN controller, transceiver etc.) and the delay of the bus line.

2. Relative oscillator tolerance between nodes.

3. Signal amplitude drop due to the series resistance of the bus cable and the input resistance of bus nodes (for a detailed description refer to Ref. 11).

Effects 1 and 2 result in a value for the maximum bus line length with respect to the CAN bit timing Ref. 11. Effect 3, on the other hand, results in a value with respect to the output signal drop along the bus line. The minimum of the two values has to be taken as the actual maximum allowable bus line length. As the signal drop is only significant for very long lengths, effect 3 can often be neglected for high data rates.

Table 7. Maximum bus line length for some standards and the TJA1040 (BT tol. = Bit Time Tolerance)

Specification	Data rate		
	125 kbit/s (BT tol. = +/- 1.25%)	250 kbit/s (BT tol. = +/- 0.75%)	500 kbit/s (BT tol. = +/- 0.5%)
SAE J2284	50 m	50 m	30 m
TJA1040	80 m	80 m	40 m

Table 7 gives the maximum bus line length for the bit rates 125 kbit/s, 250 kbit/s and 500 kbit/s, along with values specified in the SAE J2284 Ref. 5 standard associated to CAN. The calculation is based on effects 1 and 2 assuming a minimum propagation delay between any two nodes of 200 ns and a maximum bus signal delay of 8 ns/m. Notice that the stated values apply only for a well-terminated linear topology. Bad signal quality because of inadequate termination can lower the maximum allowable bus line length.

7.3 Topology aspects

The topology describes the wiring harness structure. Typical structures are linear, star- or multistar-like. In automotive, shielded or unshielded twisted pair cable usually functions as a transmission line. Transmission lines are generally characterized by the length-related resistance R_{Length}, the specific line delay t_{delay} and the characteristic line impedance Z. Table 8 shows the physical media parameters specified in the ISO11898 and SAE J2284 standard. Notice that SAE J2284 specifies the twist rate r_{twist} in addition.

Table 8. Physical media parameters of a pair of wires (shielded or unshielded)

Parameter	Notation	Unit	ISO 11898			SAE J2284		
			Min.	Nom.	Max.	Min.	Nom.	Max.
Impedance	Z	Ω	95	120	140	108	120	132
Length-related resistance	R_{Length}	mΩ/m	-	70	-	-	70	-
Specific line delay	t_{delay}	ns/m	-	5	-	-	5.5	-
Twist rate	r_{twist}	twist/m	-	-	-	33	-	50

7.3.1 Ringing due to signal reflections

Transmission lines must be terminated with the characteristic line impedance, otherwise signal reflections will occur on the bus causing significant ringing. The topology has to be chosen such that reflections will be minimized. Often the topology is a trade-off between reflections and wiring constraints.

CAN is well prepared to deal with reflection ringing due to some useful protocol features:

- Only recessive to dominant transitions are used for resynchronization.
- Resynchronization is allowed only once between the sample points of two bits and only, if the previous bit was sampled and processed with recessive value.
- The sample point is programmable to be close to the end of the bit time.

7.3.2 Linear topology

The high speed CAN standard ISO11898 defines a single line structure as network topology. The bus line is terminated at both ends with a single termination resistor. The nodes are connected via unterminated drop cables or stubs to the bus. To keep the ringing duration short compared to the bit time, the stub length should be as short as possible. For example the ISO11898 standard limits the stub length to 0.3 m at 1 Mbit/s. The corresponding SAE standard, J2284-500, recommends keeping the stub length below 1 m. To minimize standing waves, ECUs should not be placed equally spaced on the network and cable tail lengths should not all be the same Ref. 5. Table 9 along with Figure 13 illustrate the topology requirements of the SAE J2284-500 standard. At lower bit rates the maximum distance between any two ECUs as well as the ECU cable stub lengths may become longer.

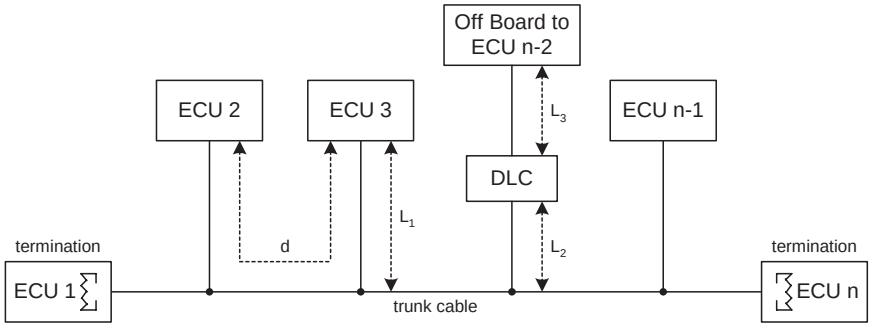


Fig 13. Topology requirements of SAE J2284

In practice some deviation from that stringent topology proposals might be necessary, because longer stub lengths are needed. Essentially the maximum allowable stub length depends on the bit timing parameters, the trunk cable length and the accumulated drop cable length. For a rule of thumb calculation of the maximum allowable stub length refer to Ref. 12.

The star topology is neither covered by ISO11898 nor by SAE J2284. However, it is sometimes used in automotive applications to overcome wiring constraints within the car. Generally, the signal integrity suffers from a star topology compared to a linear topology. It is recommended to prove the feasibility of a specific topology in each case by simulations or measurements on a system setup.

Table 9. ECU topology requirements of SAE J2284-500

Parameter	Symbol	Unit	Min.	Nom.	Max.
ECU cable stub length	L1	m	0	-	1
In-vehicle DLC cable stub length	L2	m	0	-	1
Off board DLC cable stub length	L3	m	0	-	5
Distance between any two ECUs	d	m	0.1	-	30

8. Interoperability

Interoperability of the high speed CAN transceivers C250, C251, TJA1040, TJA1041 and TJA1050 (see also Section 10.1) is guaranteed due to their compatibility with the ISO11898 standard. They can work together in the same bus network.

There are some issues related to different bus biasing behavior during low-power operation, which are considered in this chapter. Table 10 shows the bus biasing in the different operation modes as well as in unpowered condition. Whenever there is a difference in the bus biasing, a steady DC compensation current will flow within the system. The common mode input resistance mainly defines the amount of this compensation current. This is shown in Figure 14 for a bus in recessive state including TJA1040 and TJA1041 nodes.

Table 10. Bus biasing of NXP transceivers depending on operation mode

Transceiver	Operation mode	Bus bias
TJA1040	Normal	$V_{CC}/2$
	Standby	weak GND
	Unpowered	floating
TJA1041	Normal, Pwon/Listen-Only	$V_{CC}/2$
	Standby, Sleep, Go-to-Sleep, Unpowered	weak GND
TJA1050	Normal, Silent	$V_{CC}/2$
	Unpowered	weak GND
C250/C251	Normal, Standby	$V_{CC}/2$
	Unpowered	GND

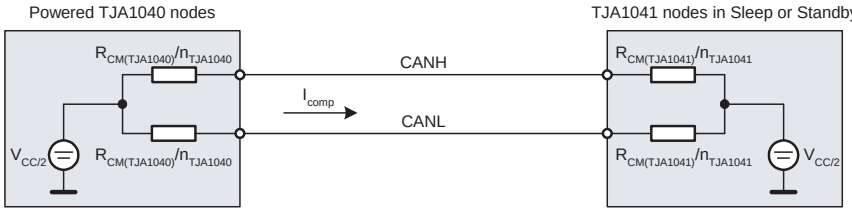


Fig 14. Equivalent bus circuit for a mixed system of TJA1040 nodes in Normal mode and TJA1041 nodes in Standby/Sleep mode

Due to the large common mode input resistance, CAN communication is not affected when parts of the network are still within low-power mode, while other nodes have already started communication. However, degradation of the emission performance is expected.

The following formula allows calculation of the whole biasing compensation current in a mixed system of TJA1040 and TJA1041 nodes.

$$I_{comp,max} = \frac{V_{CC}/2}{R_{CM(TJA1040)}/2n_{TJA1040} + R_{CM(TJA1041)}/2n_{TJA1041}} \quad (3)$$

Where:

$n_{TJA1040}$: number of nodes of powered TJA1040

$n_{TJA1041}$: number of nodes of TJA1041 in Standby/Sleep mode

$R_{CM(TJA1040)}$ =15k: min. common mode input resistance of TJA1040 at pin CANH/L

$R_{CM(TJA1041)}$ =15k: min. common mode input resistance of TJA1041 at pin CANH/L

Table 11. Conditions leading to DC compensation current

Transceiver		TJA1040		
		Normal	Standby	Unpowered
TJA1041	Normal	---	X	---
	Pwon/Listen-Only	---	X	---
	Standby	X	---	---
	Sleep	X	---	---
	Goto-Sleep	X	---	---
	Unpowered	X	---	---
TJA1050	Normal	---	X	---
	Silent	---	X	---
	Unpowered	X	---	---
C250/C251	Normal	---	X	---
	Standby	---	X	---
	Unpowered	X	---	---

X = DC compensation current --- = No DC compensation current

Table 11 identifies the conditions leading to different bus biasing and DC compensation current when different high speed CAN transceivers work together in the same bus network. The perfect passive behavior of the TJA1040 when unpowered is clear recognisable in Table 11 since an unpowered TJA1040 node never leads to a DC compensation current.

8.1 TJA1040 mixed with TJA1041 nodes

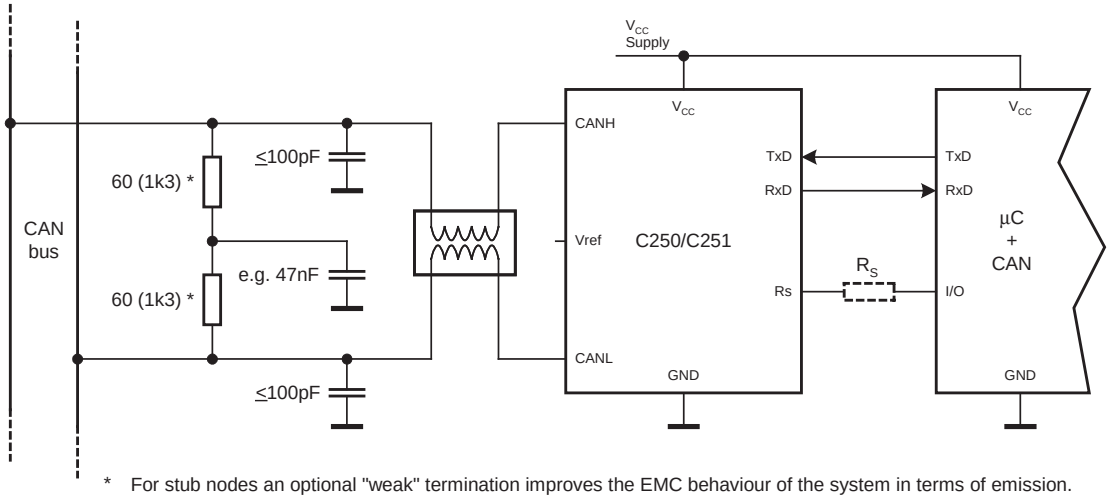
In a mixed system of TJA1040 and TJA1041 nodes, it is not expected to have situations of different bus biasing. In the low-power modes both the TJA1040 and TJA1041 show a weak termination to GND. When the bus is in power-down with all nodes either in Standby or Sleep mode, there is no DC compensation current. During normal CAN operation, when all nodes are in Normal (high speed) or Pwon/Listen-Only mode for diagnosis features, the bus is collectively biased to $V_{CC}/2$. There is no DC compensation current.

8.2 TJA1040 mixed with TJA1050 or C250/C251 nodes

Table 11 reveals also that some compensation current is flowing if TJA1040 nodes are in Normal mode, while other TJA1050 or C250/C251 nodes are left unpowered. Moreover, compensation current occurs when TJA1040 nodes are in Standby mode, while other TJA1050 or C250/C251 nodes are kept powered in any operation mode. However, the compensation current is negligible compared to the current saving due to the very low standby supply current of the TJA1040. So, upgrading existing C250/C251 ECUs with the TJA1040 always improves the overall current budget of the system, even if there are some C250/C251 nodes left in the vehicle.

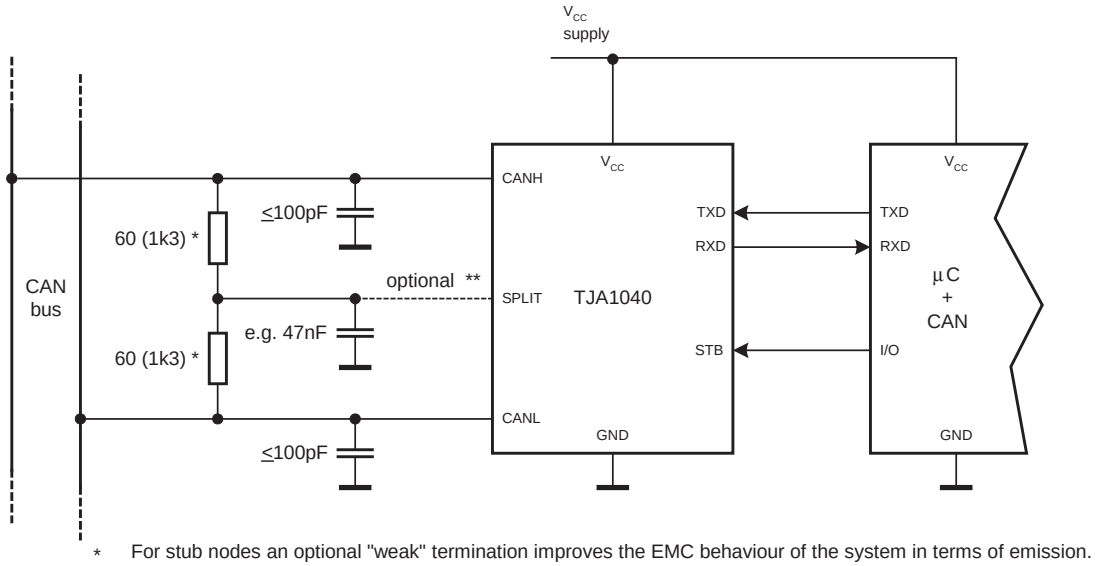
9. Upgrading hints

This chapter describes all items to be taken into account, when an existing application using the C250/C251 transceivers should be upgraded towards the TJA1040. In Figure 15 and Figure 16 typical application circuits for the C250/C251 and TJA1040, respectively, are shown.



* For stub nodes an optional "weak" termination improves the EMC behaviour of the system in terms of emission.

Fig 15. Typical application circuit for the C250/C251



* For stub nodes an optional "weak" termination improves the EMC behaviour of the system in terms of emission.
** Optional common mode stabilization by a voltage source of VCC/2 at the pin SPLIT.

Fig 16. Typical application circuit for the TJA1040

9.1 Hardware check list C250/C251 → TJA1040

Comparing the application circuits in Figure 15 and Figure 16, the following items have to be checked when replacing the C250/C251 by the TJA1040:

- If the pin SPLIT should be used for DC stabilization of the common mode voltage, the pin SPLIT (corresponds to pin Vref of C250/C251) is connected optionally to the center tap of the split termination. The pin SPLIT can simply be left open, if not used.
- If the mode control pin 8 of the C250/C251 was applied with a slope control resistor R_S for slope control, this resistor has to be removed. The corresponding pin of the TJA1040 (pin STB) should be directly connected to an output port of the microcontroller. There is the same polarity vs. function of this signal and, no need for a software modification.
- The TJA1040 does not necessarily need a common mode choke. The split termination is highly recommended as it ensures lowest emission, especially in the AM-band.

10. Appendix

10.1 Comparison of C250/C251, TJA1040, TJA1041 and TJA1050

Table 12 lists the main differences between the C250/C251, TJA1040, TJA1041 and TJA1050 from an application point of view.

Table 12. Main differences between C250/C251, TJA1040, TJA1041 and TJA1050

Feature	C250	C251	TJA1040	TJA1041	TJA1050
V_{CC} voltage range	4.5 - 5.5 V	4.5 - 5.5 V	4.75 - 5.25 V	4.75 - 5.25 V	4.75 - 5.25 V
Max. DC voltage at bus pins	–8V…+18 V	–36 V…+36 V	–27V…+40 V	–27V…+40 V	–27V…+40 V
Loop Delay	(R_S=0) 190 ns (R_S=24k) 320 ns	(R_S=0) 190 ns	255 ns	255 ns	250 ns
Standby mode current consumption (remote wake-up)	< 170 μA	< 275 μA	< 15 μA	< 10 μA at V_{CC} < 30 μA at BAT	Not supported
Sleep mode current consumption (remote wake-up)	Not supported	Not supported	Not supported	< 30 μA at BAT	Not supported
Slope Control	Variable	Variable	Fixed, EMC optimized	Fixed, EMC optimized	Fixed, EMC optimized
Passive behavior (Leakage current of bus pins; V_{CC}=0 V)	< 1000 μA ($V_{CANH/L}$=7 V)	< 2000 μA ($V_{CANH/L}$=7 V)	0 μA ($V_{CANH/L}$=5 V)	< 250 μA ($V_{CANH/L}$=5 V)	< 250 μA ($V_{CANH/L}$=5 V)
Common mode stabilization (SPLIT Pin)	No	No	Yes	Yes	No
Bus failure diagnosis	No	No	No	Yes	No
System Fail-Safe Features	No	No	TXD time-out; no reverse currents	TXD time-out; RXD clamping; VCC clamping; no reverse currents	TXD time-out; no reverse currents
3V Microcontroller support	No	No	Yes, 5 V tolerant RXD input at μC needed	Yes	Yes, 5 V tolerant RXD input at μC needed
Power-on detection (first battery connection)	No	No	No	Yes	No

Figure 17 shows the pinning of the C250/C251, TJA1040, TJA1041 and TJA1050. Apart from renaming two pins the pinning of the SO8 package transceivers is identical. Accordingly the upper part of the SO14 pinning of the TJA1041 is compatible to the SO8 pinning of the other transceiver products.

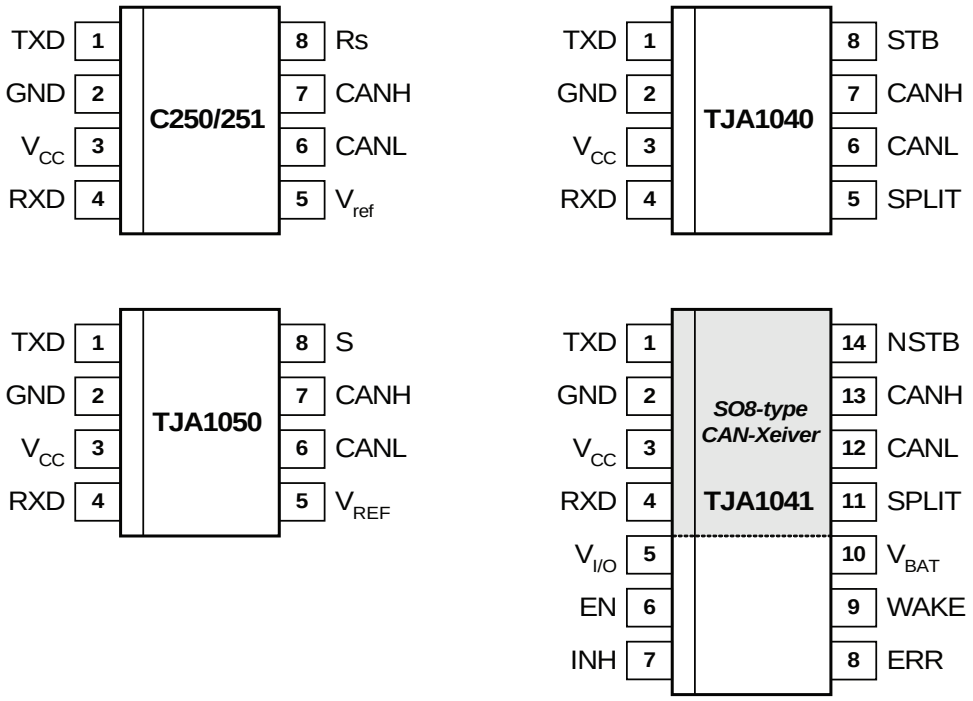


Fig 17. Pinning of the C250/C251, TJA1040, TJA1050 and TJA1041

11. Abbreviations

Table 13. Abbreviations

Acronym	Description
CAN	Controller Area Network
Clamp-15	ECU architecture, Battery supply line after the ignition key, module is temporarily supplied by the battery only (ignition key on)
Clamp-30	ECU architecture, direct battery supply line before the ignition key, module is permanently supplied by the battery
ECU	Electronic Control Unit
EMC	Electromagnetic Compatibility
EME	Electromagnetic Emission
EMI	Electromagnetic Immunity
FMEA	Failure Mode and Effects Analysis
SOI	Silicon On Insulator

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[3] **Road Vehicles - Controller Area Network (CAN) - Part 2: High-speed medium access unit —** ISO11898-2, DIS 2002

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[13] **Data Sheet PESD1CAN, CAN bus ESD protection diode —** Philips Semiconductors, 2005 Oct 17

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