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TDA8024 Smart Card Interface

Rev. 1.0 — 6 August 2013　　　　　　　　　　　　　　**Application note**

Revision history

Rev	Date	Description
1.0	20130806	First official release

Contact information

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1. Introduction

TDA8024 is a smart card interface device making the electrical interface between a micro controller and a smart card. This device supports mainly asynchronous cards (micro controller based IC cards).

This device a direct derivative of the TDA8004 and is pin to pin compatible (precautions have to be taken for PORadj pin).New features have been added in order to be compliant with EMV specification.

The electrical characteristics of TDA8024 are in accordance with NDS requirements (IRD Electrical Interface Specifications doc n° LC-T056) but also comply with ISO7816-3 and E.M.V. (Europay, Mastercard, Visa) normalisation.

TDA8024 can be used in various applications such as pay-TV, point of sales terminals (P.O.S.), public phone, vending machines, and a lot of conditional access applications (i.e. internet ,...).

This device does not support smart cards with a programming voltage (VPP) greater than 5V, because new generation of IC cards does not need such a feature (EEPROM based smart cards).

1.1 Main features

- One protected I/O line and two protected auxiliary lines (AUX1 and AUX2) that can be used as standards I/O lines (same internal structure) or that can be used to drive the C4 or C8 contacts in synchronous applications for example.
- VCC regulation 3V/5V +/-5% with Icc max = 80mA, with current limitation (120mA) in case of short circuit.
- Clock generation (up to 20MHz on the smart card side) with different possible configurations
- Automatic activation and deactivation sequences through an independent internal clock.
- Overload, thermal and card take off protections.
- ESD protections on smart card side (>6kV).
- Asynchronous cards supported.
- Supply voltage from 2.7V to 6.5V with supervision adjustable.
- Supply voltage from 4V to 6.5V for the step up converter (VDDP).
- Built in 10ms de-bouncing on card presence contacts.

This device is proposed in SO28 package and also in TSSOP28 package. The pinning of the TSSOP28 is identical to the SO28 one.

The block diagram of this circuit is presented on the next figure and all the internal blocks will be described in the coming paragraphs.
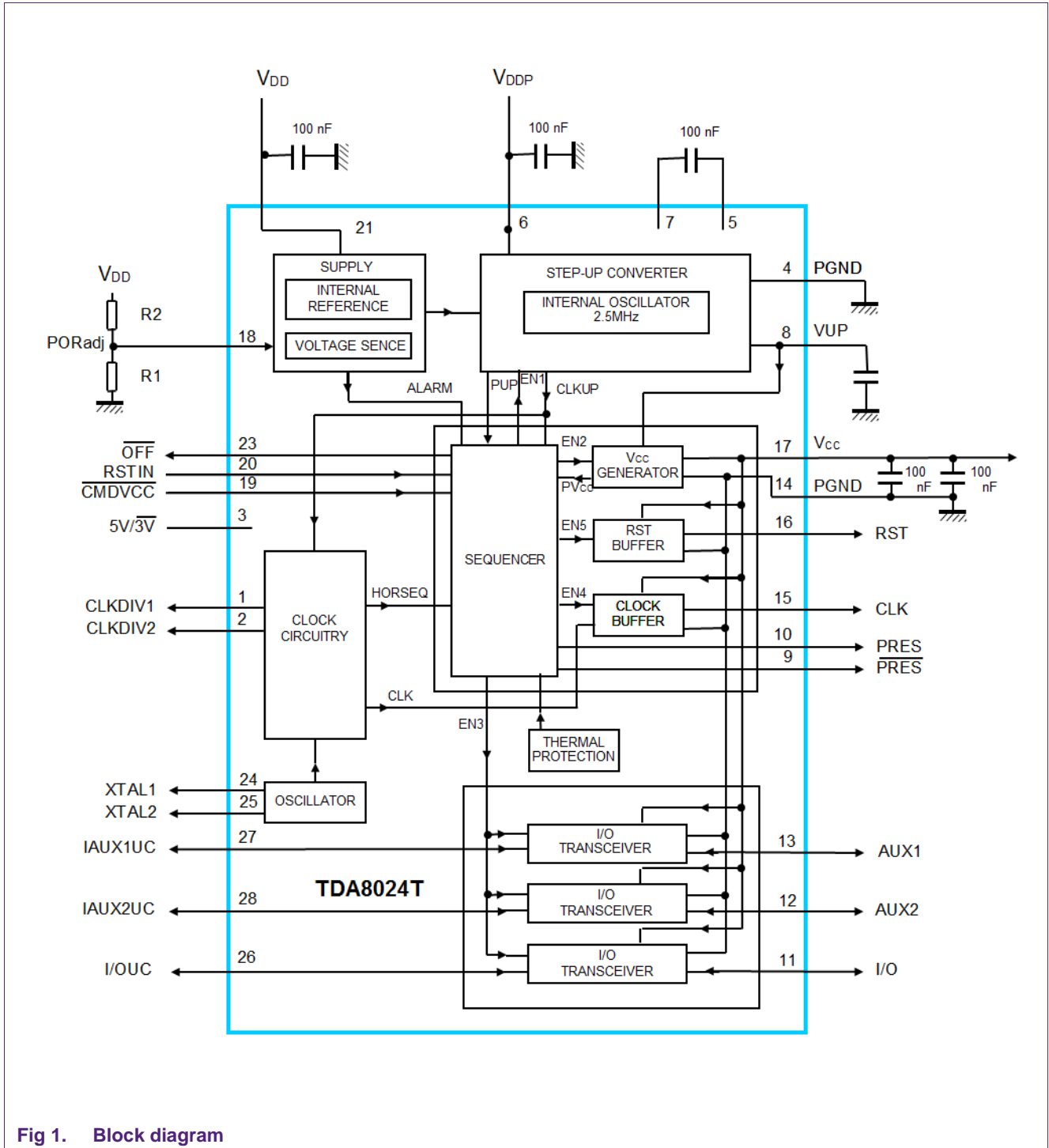

Fig 1.   Block diagram

2. Block overview

2.1 Power supply and voltage supervisor

The power supply pins are VDD and GND for the core, and VDDP and GNDP for the smart card power supply.

VDD shall be in the range of 2.7V to 6.5V. At power on, the logic is held in reset state until VDD reaches the voltage supervisor threshold V_{TH2} (2.45V typ. value).

A voltage supervisor is integrated in order to secure the smart card if the power supply drops below the threshold voltage.

It is possible to add external resistor in order to change supervisor threshold.

Important note: In some rare cases, linked to the board design and chip environment, the logic circuitry can be in an undefined state if Vdd is missing which can lead to an overconsumption. In order to avoid this, Vdd must be raised before Vddp.

2.2 Step up converter

2.2.1 Principle of the step up converter

The step up converter is intended to deliver either a regulated +5V or +3V on the VCC pin when the card is activated whatever the supply voltage on Vddp is within the range 4V to 6.5V.

This step up converter needs a specific supply voltage VDDP that shall be within the range from 4V to 6.5V. This pin needs a close discoupling capacitor.

This step up is from doubler type and is working with an internal oscillator running at 2.5MHz and needs two external capacitors in order to operate properly. A 100nF capacitor is necessary between pins S1 and S2 and another 100nF capacitor is needed between pin VUP and GND.

These capacitors shall be placed as close as possible to the pins of the integrated circuit, in order to have a better efficiency and to avoid pollution on others signals.

2.2.2 Current consumption

The current Iddp depends on the implementation. However, it is possible to approximately estimate its typical value.

The step converter can be in a mode called *voltage follower* with the following cases:
- VCC= 5 V and VDDP> 5.8 V
- VCC= 3 V and VDDP> 4.1 V

In this case, Iddp is the same as Icc (card current), plus around 10mA.

For the following cases, the step converter is in a mode called *voltage doubler*:
- VCC= 5 V and VDDP< 5.7 V
- VCC= 3 V and VDDP< 4.0 V

In voltage doubler mode, Iddp is twice Icc plus few mA (yield losses).

In the following table value example for the CAKE8024 daughterboard

Table 1.   Example of Iddp values in function of Icc in voltage doubler mode

Icc	Iddp typical	Note
0 mA	10 mA	
35 mA	80 mA	
80 mA	200 mA	
150 mA	340mA	Lasts around 100µs (250µs max.) before deactivation

2.3 Clock circuitry

The clock signal CLK can be applied to the smart card through two different ways:
1- Generation of the card clock by the means of crystal oscillator (2 to 26MHz) or resonator tied to XTAL1 and XTAL2 pin.
2- Use of an external signal applied on XTAL1 pin (XTAL2 being left open).

CLKDIV1 and CLKDIV2 pins are programming different clock frequencies on CLK output as shown on the following table:

Table 2.   Clock frequency programming

CLKDIV1	CLKDIV2	CLK
0	0	XTAL/8
0	1	XTAL/4
1	1	XTAL/2
1	0	XTAL

A special circuitry has been built so that any frequency change on CLK during a session is made without any spurious pulses as mentioned in the ISO7816-3 normalisation.

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The following figure shows the synchronous frequency change during a session.

Fig 2. **Synchronous frequency change during a session**
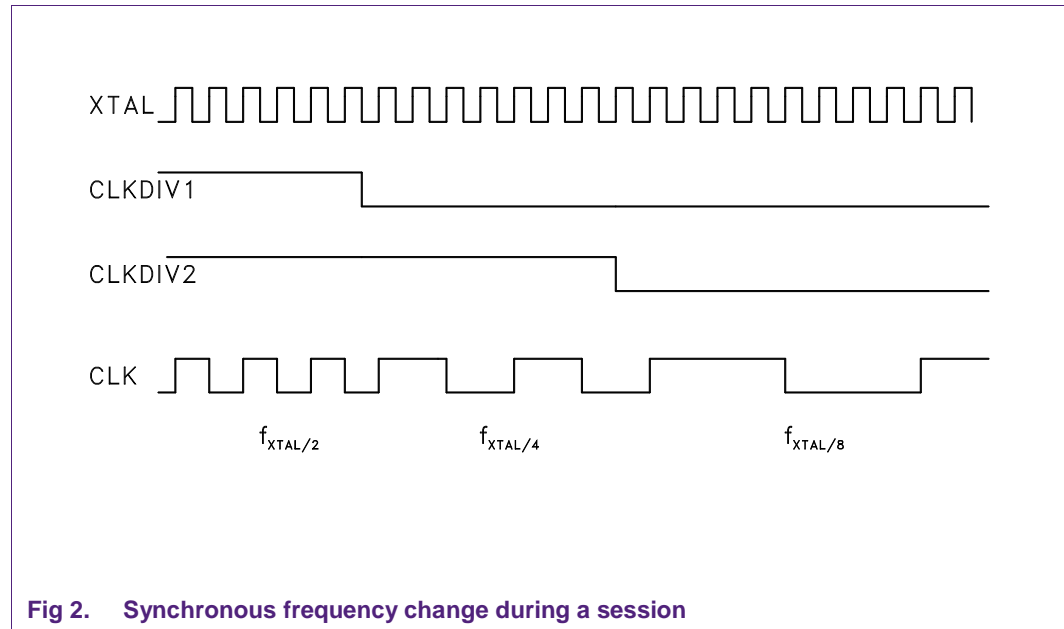
The duty cycle is in the range 45%, 55% of the period during stable operation.
Rise and fall times of the CLK signal are 16ns maximum which allows to be fully compliant with the E.M.V. specification with a 5 MHz signal on CLK (tr, tf <8% of the period).

2.4 VCC generation

This output pin is used to supply VCC to the IC card.
For an average current of less than 80mA, the active level of VCC is in the range of 4.75V/ 5.25V.
In case of current pulses, (dynamic loads) VCC remains between 4.5V and 5.5V for a maximum load of 40nAs.
When VCC is shorted to ground Icc is limited to 120mA and if during normal operation Icc exceeds 90mA (overload detection), an automatic deactivation is performed.

The slew rate of VCC at power on is 0.18V/µs.

Two decoupling capacitors of 100nF are necessary on VCC pin; one shall be placed close to the VCC pin of the integrated circuit and the other shall be placed as close as possible of the VCC contact of the smart card socket. With such a decoupling system, the NDS requirements for VCC behaviour with fast transients are fulfilled.

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2.5 Logic circuitry

The logic block is built with a sequencer that enables or disables the different signals whatever the circuit mode is. It manages all the activation and deactivation phases.

2.5.1 Activation sequence

An activation sequence is initiated by setting the pin CMDVCCN to low level.
The internal sequencer drives the following sequence:
1- Step up converter starts.
2- VCC rises from 0 to +5V (or from 0 to +3V).
3- I_O, AUX1, AUX2 are enabled
4- CLK is sent (by setting RSTIN to low level).
5- RST is enabled.

If RSTIN is switched from high to low level between the t3 and t5 window, it will automatically make CLK start at the same time; this allows a proper count of the clock cycles for the answer to reset procedure.

2.5.2 Deactivation sequence

When a communication is completed, the host microcontroller sets the CMDVCCN line to high level and the circuit starts an automatic deactivation sequence.
1-RST goes to low level.
2- CLK is stopped.
3- I_O, AUX1, AUX2 are pulled low.
4- VCC falls to low level.
5- VUP falls to zero.

This deactivation sequence is completed in 100μs maximum.

2.5.3 Protection

The following fault conditions are monitored by the circuit:
- short circuit or current overload on VCC
- card removal during a transaction
- overheating problem
- supply voltage (VDD) dropping
- V_{DDP} too low, or current from VUP too high

When one of the five conditions occurs the circuit pulls the OFFN line to low level and a deactivation sequence is automatically processed.
If either the fourth or the fifth condition occurs, a deactivation sequence is automatically processed; the host controller has to wait at least 10 ms before starting a new activation.

When the deactivation sequence is completed, the OFFN line is reset to its high level by setting CMDVCCN to high level except if the card has been taken off.

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2.5.4 Presence detection

The PRES or PRESN contacts are giving the card presence information (to the TDA8024) when they are connected to the switch of the card reader socket. These pins are in the inactive state when they are open and there is a logic OR between these two signals. So the unused pin can be left open. The presence card information is then given to the host controller by the means of the OFFN pin and a built in 10 ms de-bouncing is automatically perform.

2.5.4.1 Card insertion

On TDA8024 a card insertion is determined by the fact that OFFN is rising from low to high level; depending on the type of presence card contact of the card reader no software de-bouncing is necessary on the OFFN signal.
On the example below, we can see the delay between the rising edge of PRES pin and the rising edge of OFFN.

Fig 3. Delay between the rising edge of PRES pin and the rising edge of OFFN
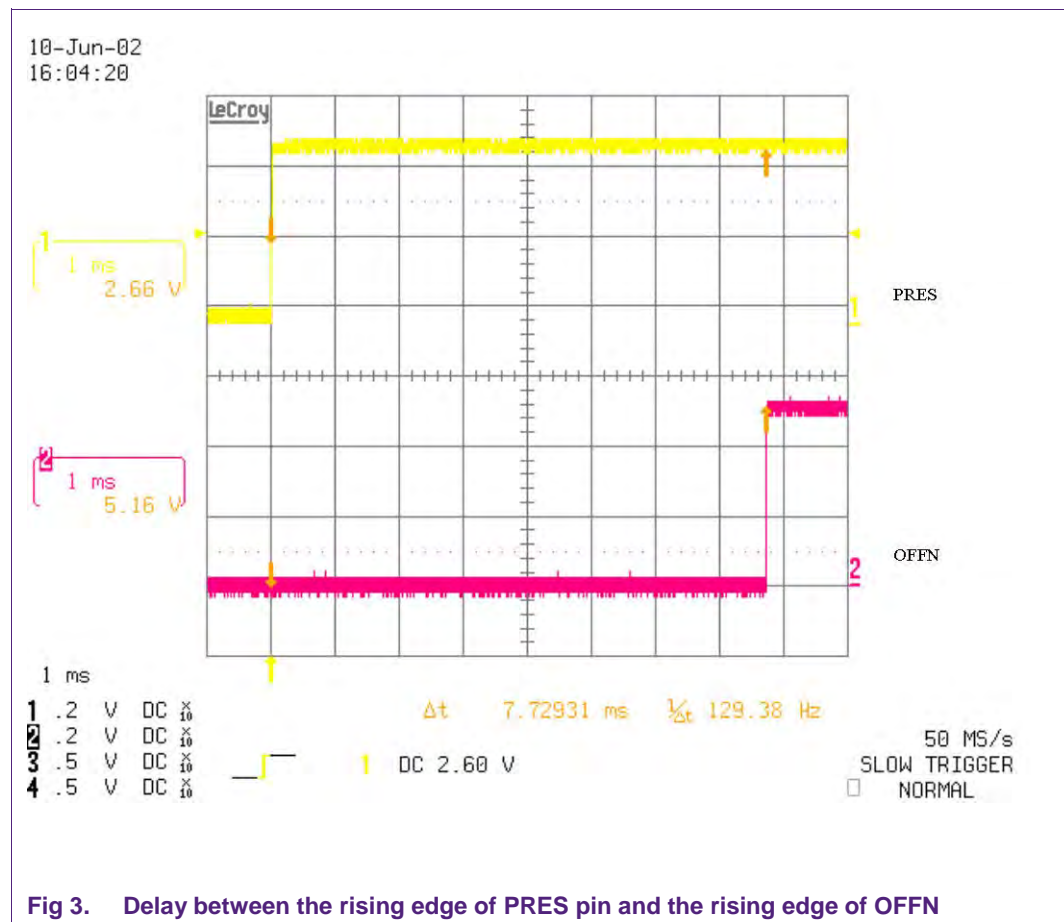
2.5.4.2 Card removal

In case of card removal the OFFN pin will switch from high level to low level and TDA8024 deactivates securely the card. If CMDVCCN is set back to high level 260µs after OFFN has gone low and if OFFN stays low, we can deduce that the card has been removed.

Fig 4.   Card deactivation while card is removed
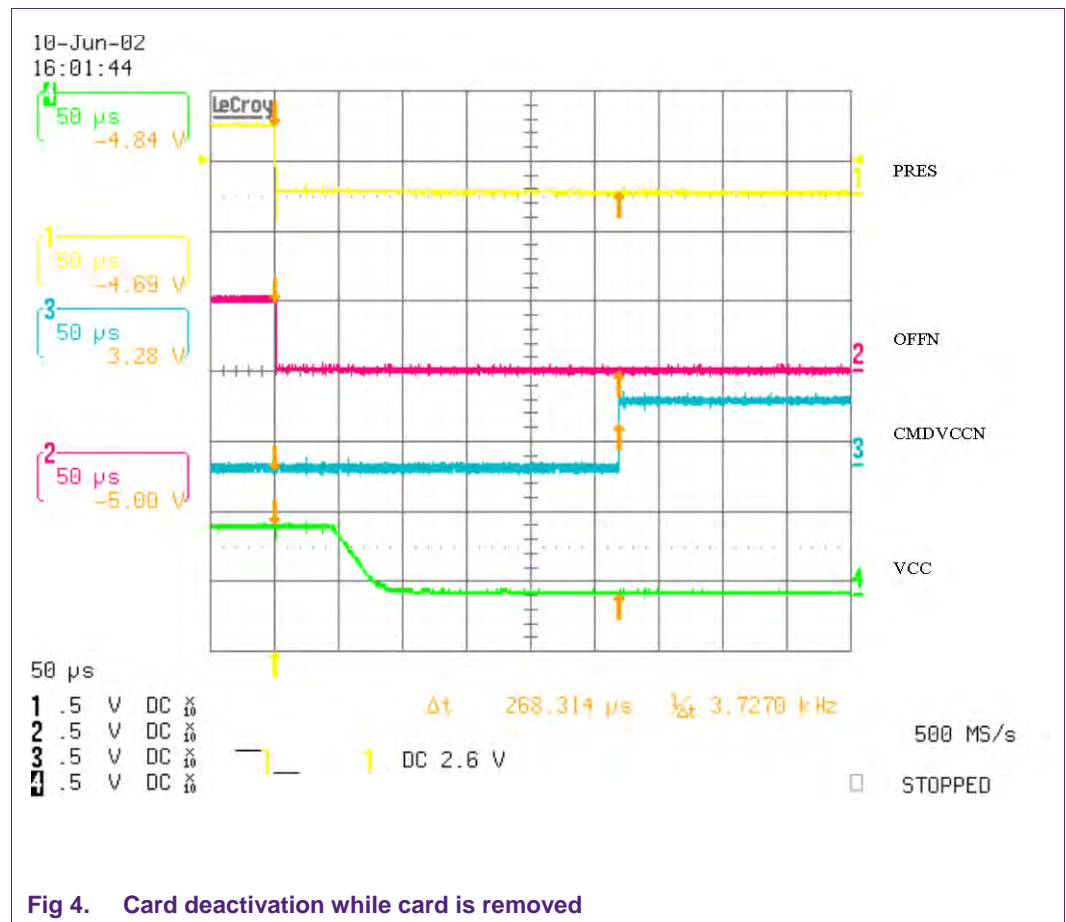
Hardware problem (over current on VCC, short circuit, over temperature)

During a card session, if a hardware problem occurs, the OFFN pin will be set automatically to low level and the card securely deactivated. If CMDVCCN is set back to high level 260µs after OFFN has gone low and if OFFN goes back high, we can deduce that a hardware problem has occurred.
On the example below, trace 1 shows OFFN and trace 2 shows CMDVCCN.

Fig 5. Example of hardware problem during card session
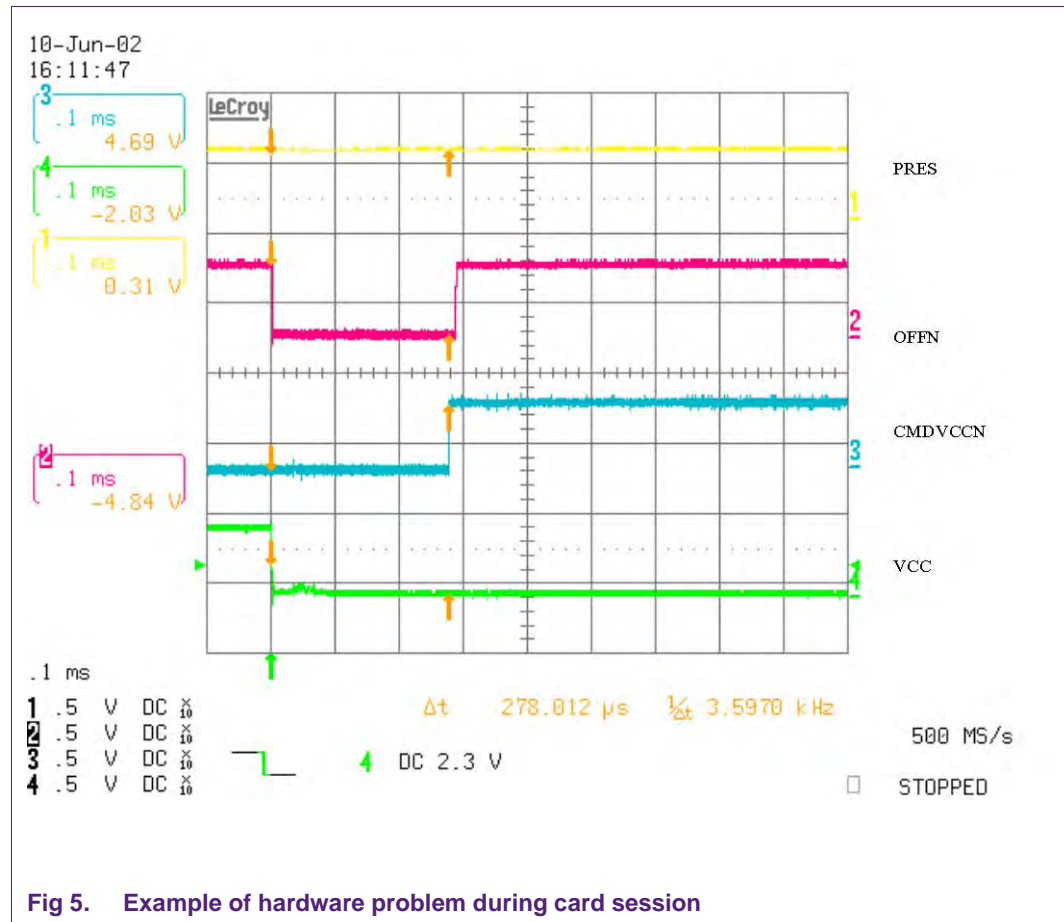
Remark:
The minimum timing for setting CMDVCCN back high after OFFN has gone low is dependent on hardware design and must be at least 260 µs long.

2.6 I/O, AUX1 and AUX2 lines

On TDA8024 one I/O line is available but also two auxiliary lines that can either be used as standards I/Os or that can be used to drive the C4 and C8 contacts in synchronous cards applications.

These lines are referenced to VDD on the micro controller side (so that 3V operation is possible), and on the card side the lines are referenced to VCC.

2.7 PORadj line

When connected to ground, the voltage supervisor threshold if set to Vth2 + Vhys2 and a reset pulse of 10 ms is generated by the supervisor.

If an external resistor bridge is connected to this pin (R1 to GND, R2 to VDD) then the following formula will give the new threshold:

$$Vth2ext \ rise = (1+R2/R1)(\ Vbg+ Vhysext/2),$$
$$Vth2ext \ fall =(1+R2/R1)(Vbg - Vhysext/2),$$
$$where \ Vbg=1.25V \ typ, \ and \ Vhysext=60mV \ typ)$$

The reset pulse generated by the supervisor is set to 20 ms.

Warning:

When the PORadj pin is not used, it is strongly recommended to tie the PORadj pin to GND so that this pin should not be sensitive to noise, otherwise an unexpected reset of the device can occur.
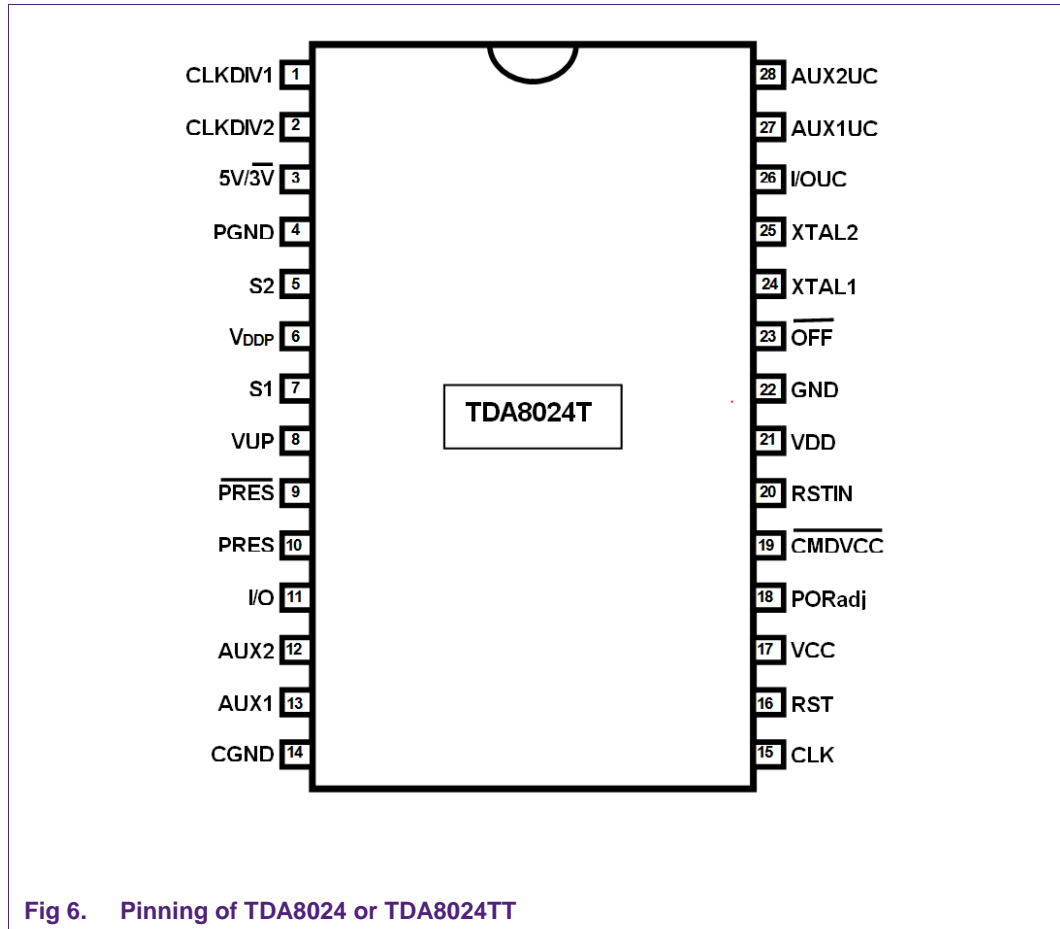
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3. Pinning and pin function of TDA8024T or TDA8024TT

TDA8024 is available in SO28 or TSSOP28 package.

The following table gives the pin function:

Table 3. Pins functions

PIN TDA8024	Symbol	Description
1	CLKDIV1	Control input for CLK frequency selection
2	CLKDIV2	Control input for CLK frequency selection
3	5V/3V_N	Card VCC control, 5V when high, 3V when low
4	GNDP	Ground for the step up converter part
5	S2	Capacitance for step up converter (connected to S1 via 100nF)
6	VDDP	Supply voltage for step up converter
7	S1	Capacitance for step up converter (connected to S2 via 100nF)
8	VUP	Output from step up converter (connected to ground via 100nF)
9	PRES_N	Card presence contact (Active Low)
10	PRES	Card presence contact (Active High)
11	I_O	Data line from/to the smart card
12	AUX2	Auxiliary data line from/to the smart card
13	AUX1	Auxiliary data line from/to the smart card
14	GNDC	Ground for card signals
15	CLK	Clock output to the smart card
16	RST	Reset output to the smart card
17	VCC	Smart card supply voltage (discoupling 100nF mandatory)
18	PORadj	Supervisor threshold; connected to GND if not used
19	CMDVCC_N	Control for smart card activation (Active Low)
20	RSTIN	Control input for RST management
21	VDD	Supply voltage
22	GND	Ground
23	OFF_N	Open drain NMOS interrupt to microcontroller (Active Low)
24	XTAL1	Crystal connexion or input for external clock
25	XTAL2	Crystal connexion
26	I_OμC	Data line from/to the microcontroller
27	AUX1μC	Auxiliary data line from/to the microcontroller
28	AUX2μC	Auxiliary data line from/to the microcontroller

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CLKDIV1	1		28	AUX2UC
CLKDIV2	2		27	AUX1UC
5V/$\overline{3V}$	3		26	I/OUC
PGND	4		25	XTAL2
S2	5		24	XTAL1
V_{DDP}	6	**TDA8024T**	23	$\overline{OFF}$
S1	7		22	GND
VUP	8		21	VDD
$\overline{PRES}$	9		20	RSTIN
PRES	10		19	$\overline{CMDVCC}$
I/O	11		18	PORadj
AUX2	12		17	VCC
AUX1	13		16	RST
CGND	14		15	CLK

Fig 6.   **Pinning of TDA8024 or TDA8024TT**

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4. Smart card interface application

4.1 Introduction

The main applications for TDA8024 are pay TV (multistandards Conditional Access Systems) but also multipurpose card readers such as in banking applications, public phone, vending machines, PC terminals or keyboards.
Different application examples are given in the coming paragraphs.

4.2 External components

The basic external components for TDA8024 are:

- a crystal oscillator plus 2 capacitors for clock generation.
- a 100nF capacitor on VUP
- a 100nF capacitor between S1 and S2
- 2x100nF capacitors on VCC: one close to pin 17, the other close to the VCC contact of the card reader socket.
- 2 discoupling capacitors 100nF plus 10µF (polarised) between VDD and GND
- 2 discoupling capacitors 100nF plus 10µF (polarised) between VDDP and GND

For layout considerations the discoupling capacitors on VDDP must be as close as possible of VDDP pin and the other capacitors (on VUP, S1, S2) must be as close as possible of the IC pins.

The 100nF capacitors on VUP, S1, S2 and VCC must be low ESR capacitors.

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4.3 Activation of TDA8024

4.3.1 Asynchronous application

An activation is possible if a smart card is present (OFFN high).

Then CMDVCCN has to be set to low level; a transition on RSTIN in the t3, t5 window will make CLK start at the same time. It is advised to switch RSTIN pin from high level to low level, 140µs after CMDVCCN has been set to low level, in order to allow a precise count of the 40000 clock cycles by the host controller.

Figure below shows this activation phase:

t1: 140µs   (within the t3 and t5 window of the specification)
t2: 40000 clock cycles (ISO7816-3)

Fig 7.   Activation phase
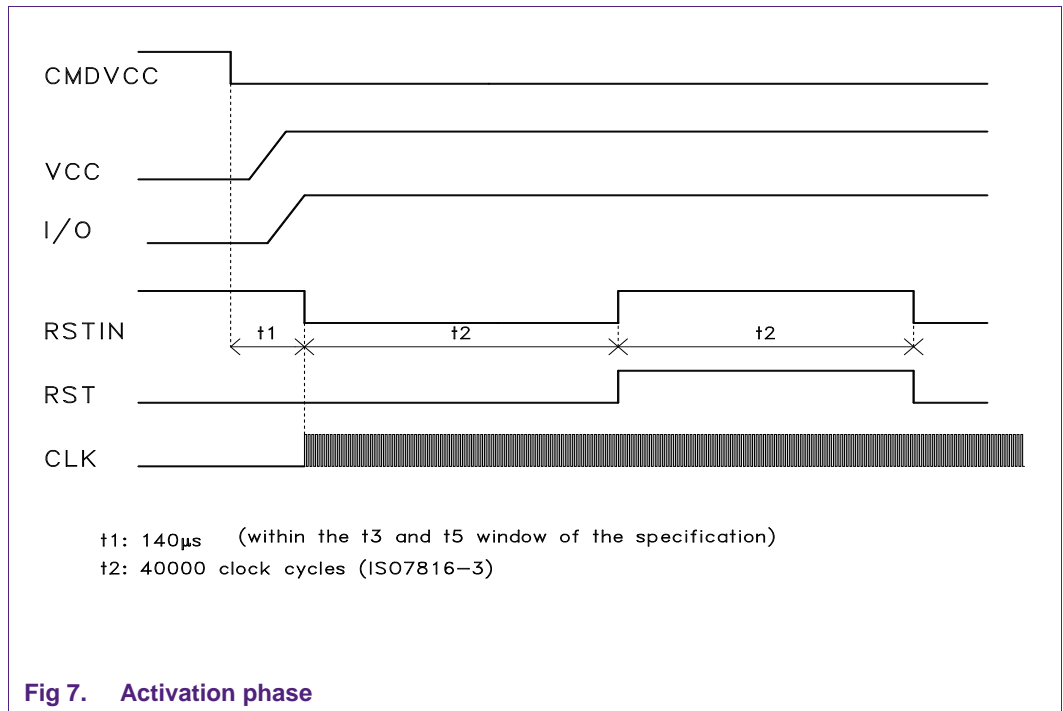
Another possibility is to start the activation by holding the XTAL1 line low (at least during 220µs); so the count of the CLK cycles can start as soon as the clock is present on XTAL1 and also on CLK line as presented on the following figure.

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t1: 140µs   (within the t3 and t5 window of the specification)
t2: 40000 clock cycles (ISO7816-3)

Fig 8.   Start the activation by holding the XTAL1 line
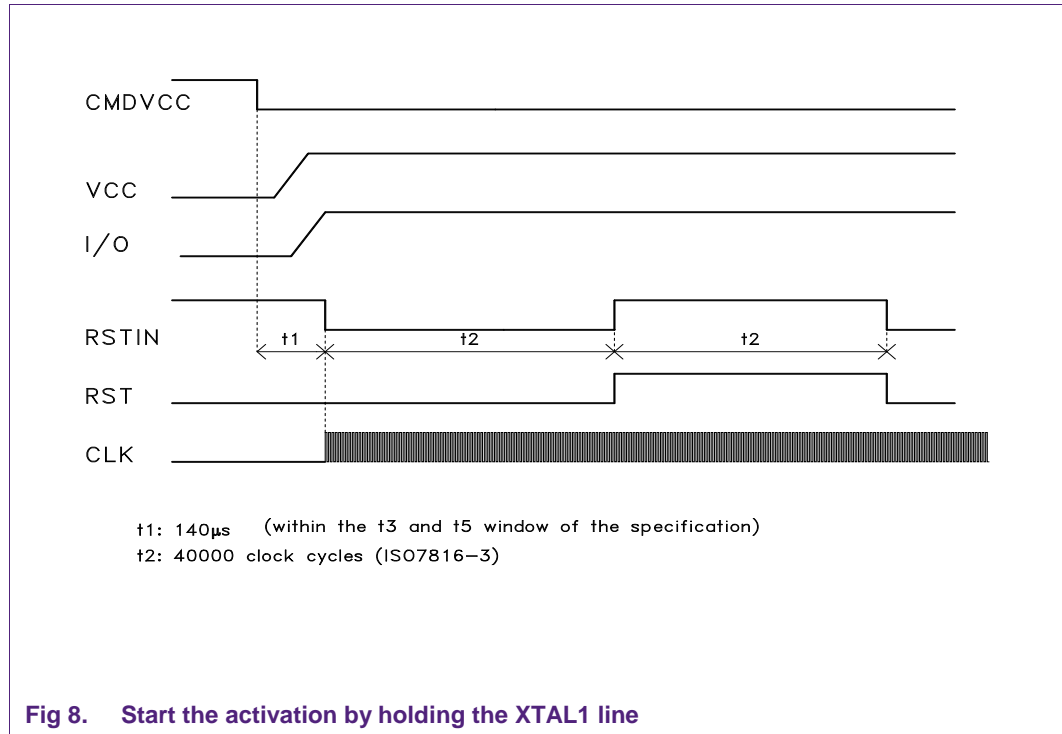
4.3.2 Application for asynchronous cards with the ICAM V2 from NDS

A pay TV application of TDA8024 for asynchronous smart cards is presented on Fig 9.

All the commands lines are directly driven by NDS device. AUX1 and AUX2 lines are used to drive the C4 and C8 contacts. On the smart card socket, the C6 contact (VPP) is connected to the C1 contact (VCC) in order to be able to drive smart cards that require a +5V on VPP during a writing phase.

A reference layout has been made for this application (on a dual sided pcb) and is given in Annex 1.

The layout recommendations are the following:
Use low ESR capacitors for the step up converter (capacitors C3, C4).
Place the 220nF capacitor (C1) as close as possible of the contact C1I of the card reader.

It is recommended to implement a GND line between CLK line and RST line in order to avoid cross talk form CLK on RST line.

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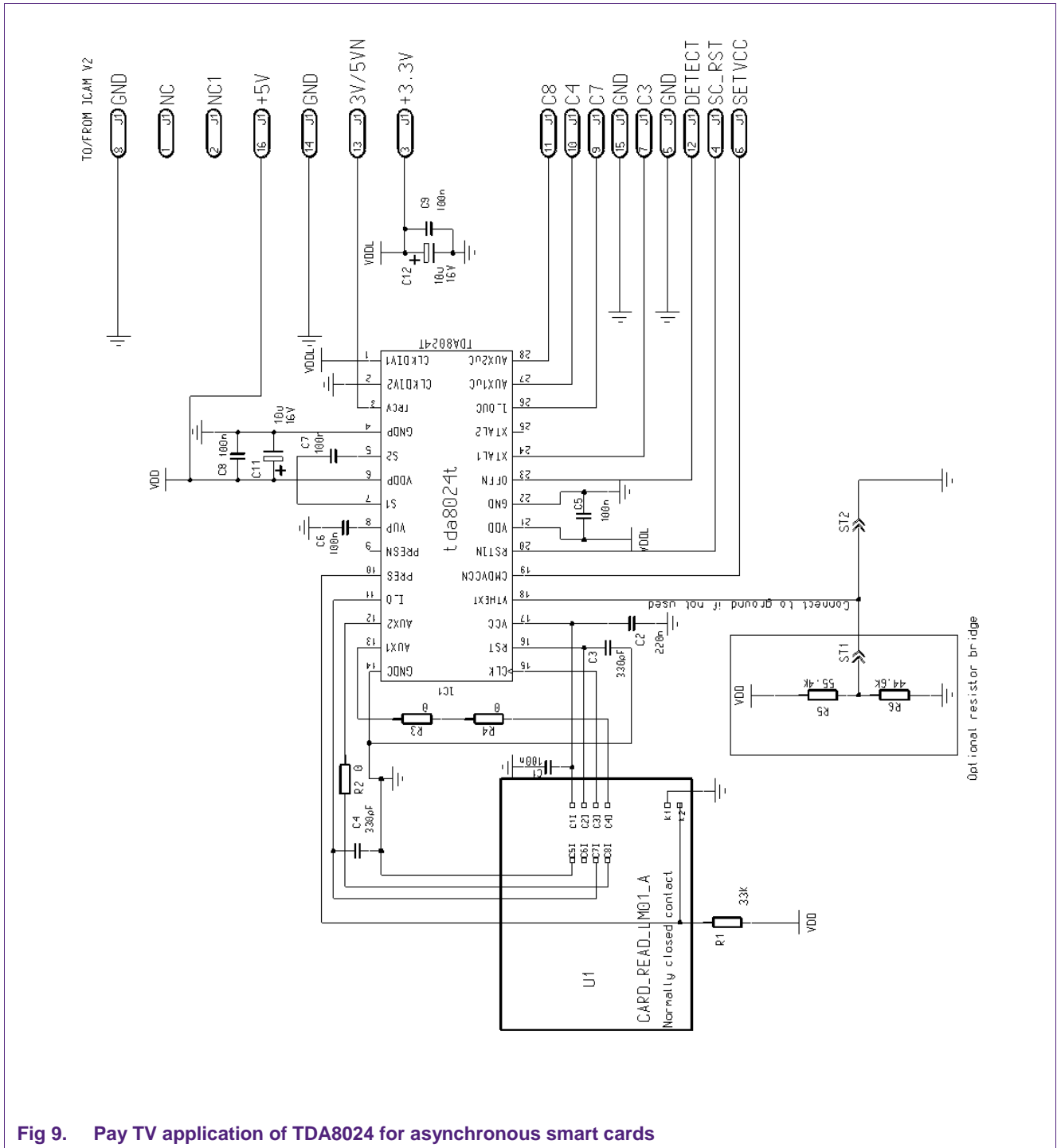
Fig 9.   Pay TV application of TDA8024 for asynchronous smart cards

In this case the clock signal is coming from the NDS device and so the CLK frequency has been programmed as XTAL/1.

4.3.3 Standard asynchronous application
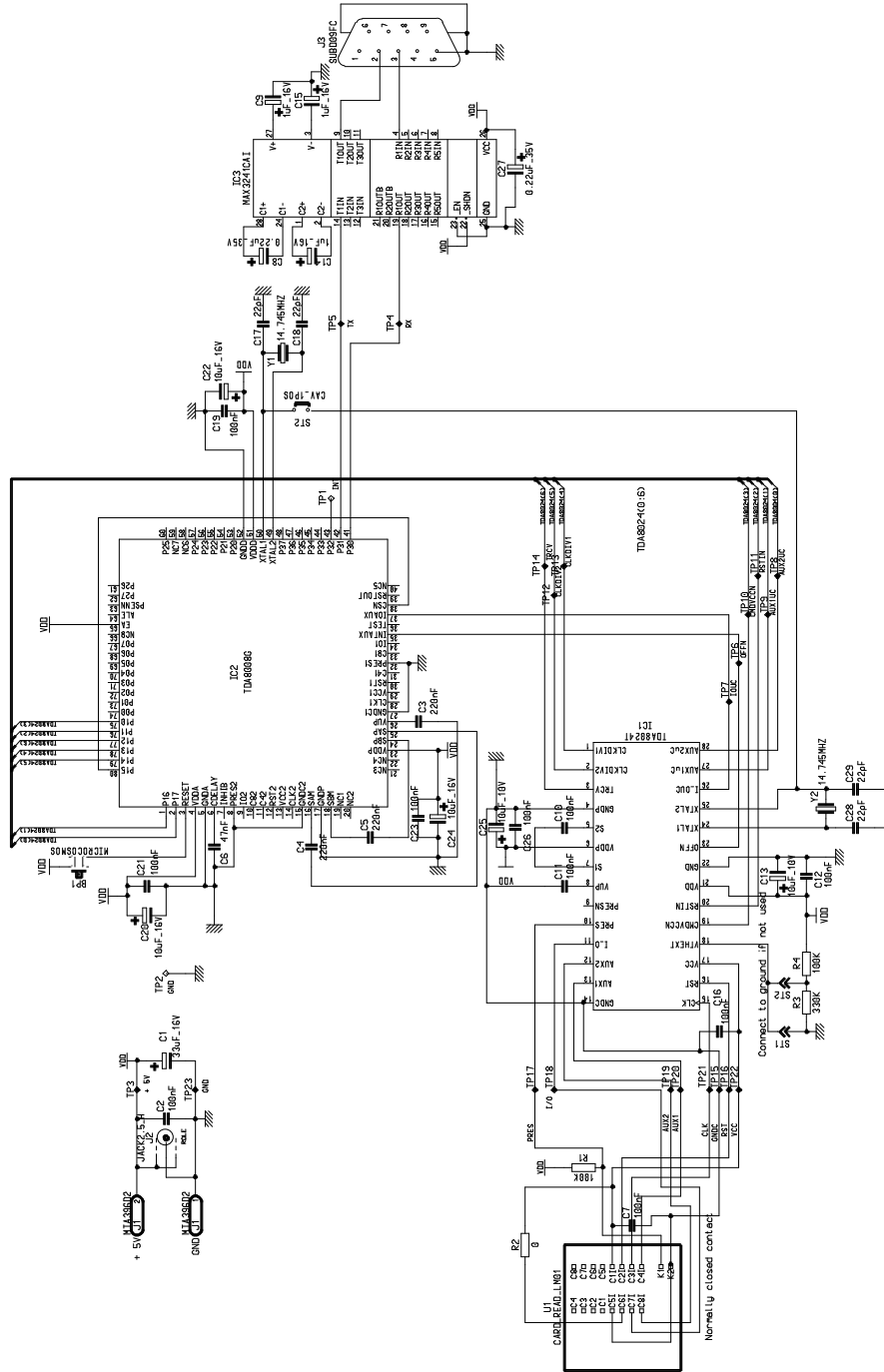
Fig 10. Standard asynchronous application example

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4.3.4 Application with security modules

Some applications such as banking applications require that a smart card having some security features concerning the application is permanently inserted in the smart card reader. These Security Access Modules are characterising the application and the terminal, and depending of the number of applications that is supported by the terminal, there can be more than one in the terminal.

For an application with a single SAM, it is possible to use a single TDA8024 if the customer card is asynchronous only. TDA8024 is supervising only the presence of the customer card, the SAM card being supposed to be ever present. The communication with the customer card is made via the standard I/O line and the communication with the SAM is made via the AUX1 line that can be considered as a second standard I/O line. The controller can switch from one to the other by the means of the multiplexer. Both cards are activated at the same time, and in order to get the different ATRs, a cold reset can be done with the first card and then a second warm reset is made with the SAM after having switched the I/O line.

Fig 11 displays an application where there are 2 security modules and one customer card. For that 1TDA8007B and 1TDA8024 are necessary; the TDA8007B is driving the 2 SAMs via the I/O1, I/O2, and the TDA8024 is driving the customer card via the 3rd slot of the TDA8007B. This is a very safe solution and a few number of external components are necessary (i.e. one single crystal oscillator).

In all these applications any asynchronous protocol (T=0, T=1) can be used because TDA8024 is protocol transparent on the I/O lines. The protocol management is made by software in the remote controller.

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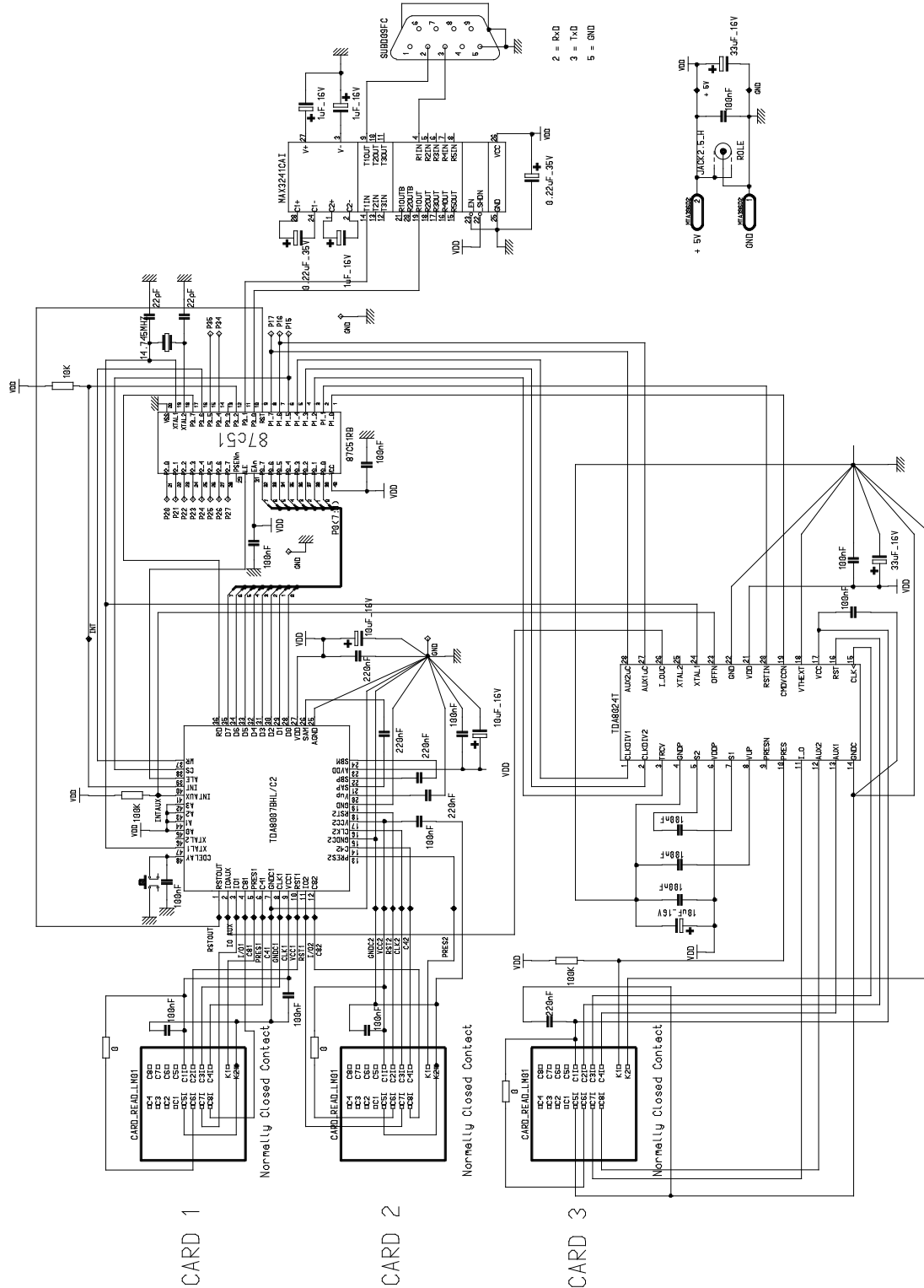
Fig 11. Application where there are 2 security modules and one customer card with a TDA8007B

5. Conclusion

TDA8024 is a complete low power smart card interface that complies with ISO7816-3 and E.M.V. requirements. It is very suitable for many applications (pay-TV, banking, P.O.S., PC applications).

This device is recommended by News Digital Systems for any pay TV application using their conditional access system.

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6. Appendixes

The following annex refers to the TDA8004 but is still valid for the TDA8024 (except that PORadj pin should be connected to GND.
Pin RFU1 becomes 3V/5VN and there is no possibility to modify the supervisor threshold.

Appendix 1: TDA8024TT reference layout (CAKE8024_12_D)
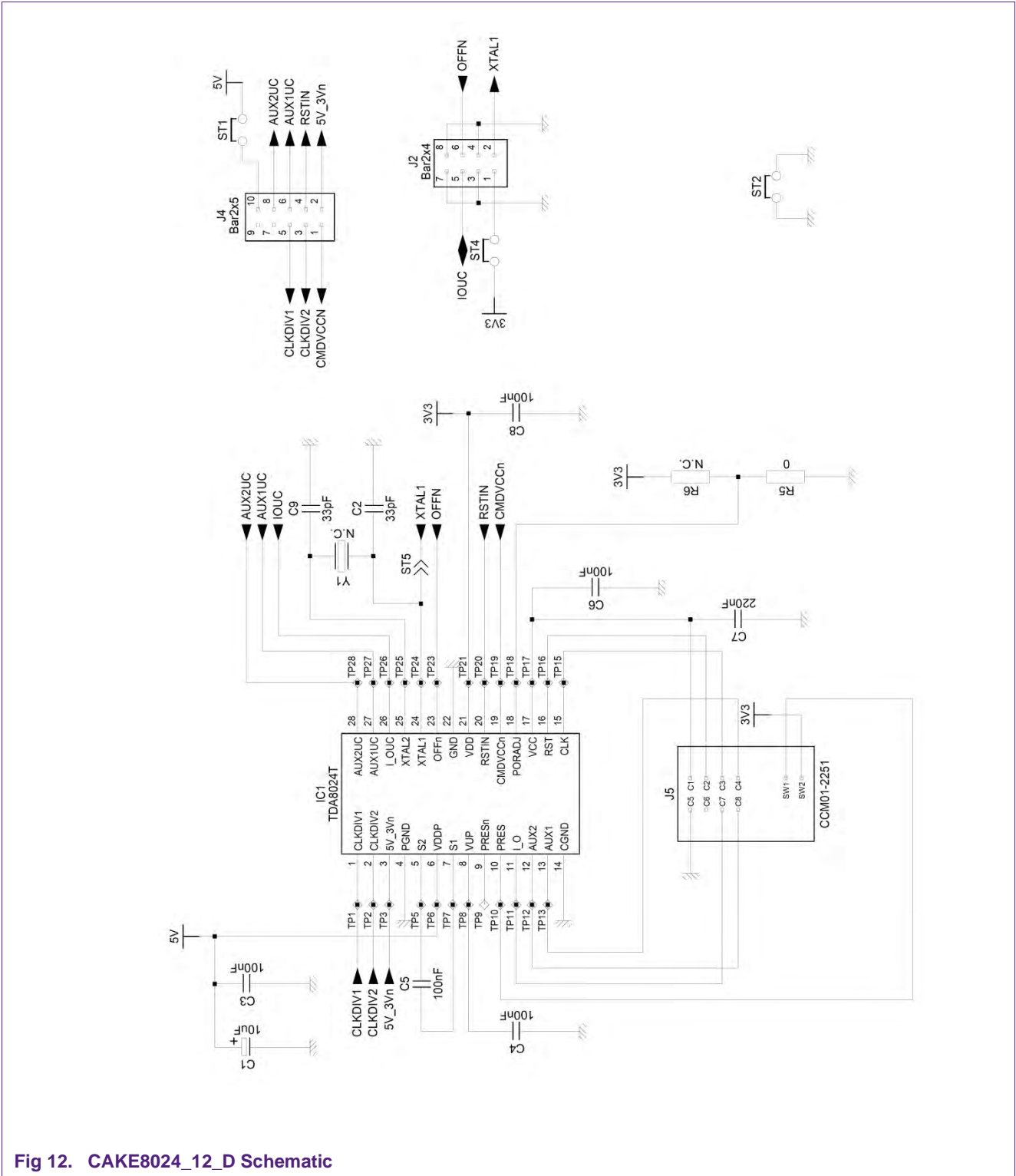
Fig 12. CAKE8024_12_D Schematic

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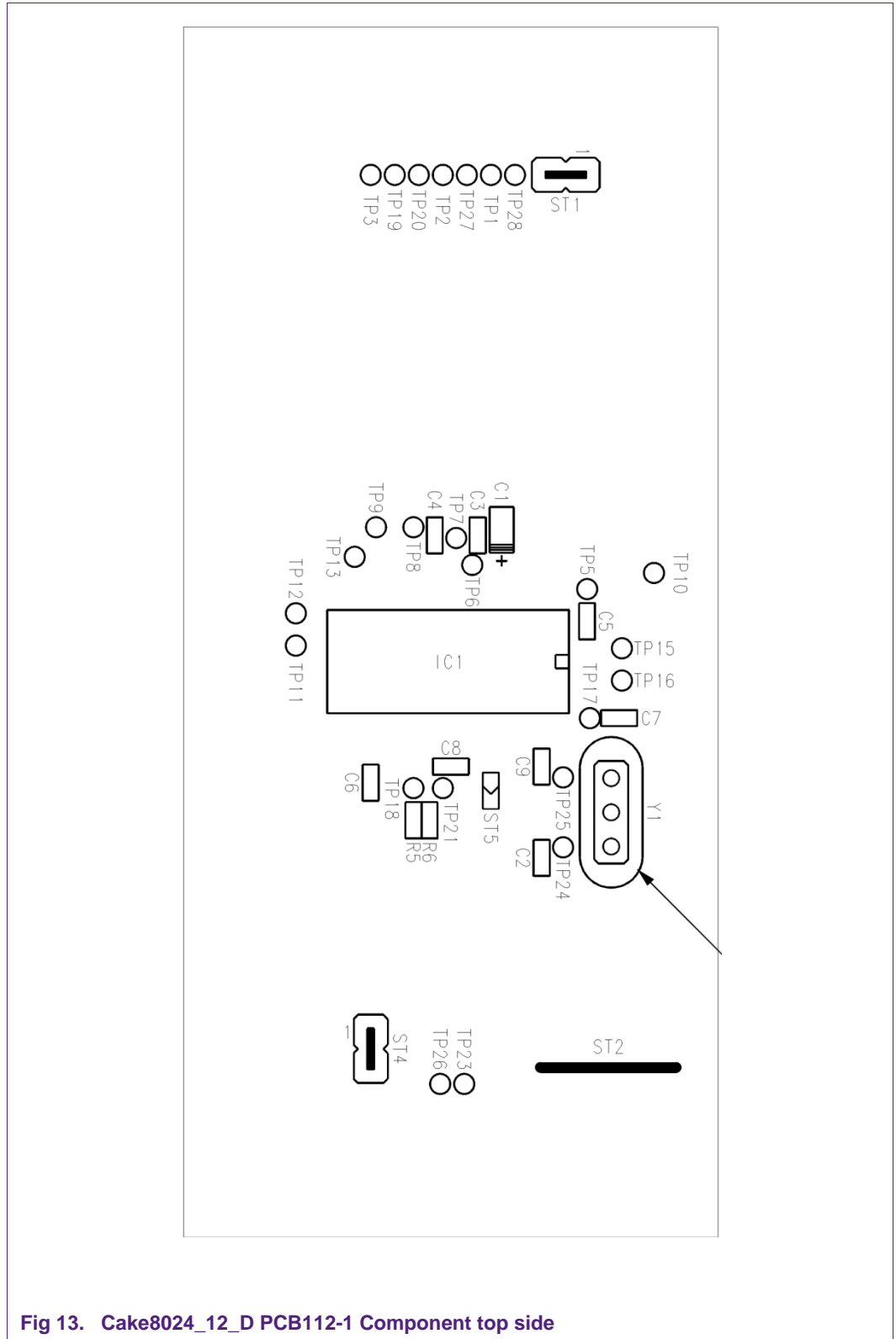
Fig 13. Cake8024_12_D PCB112-1 Component top side

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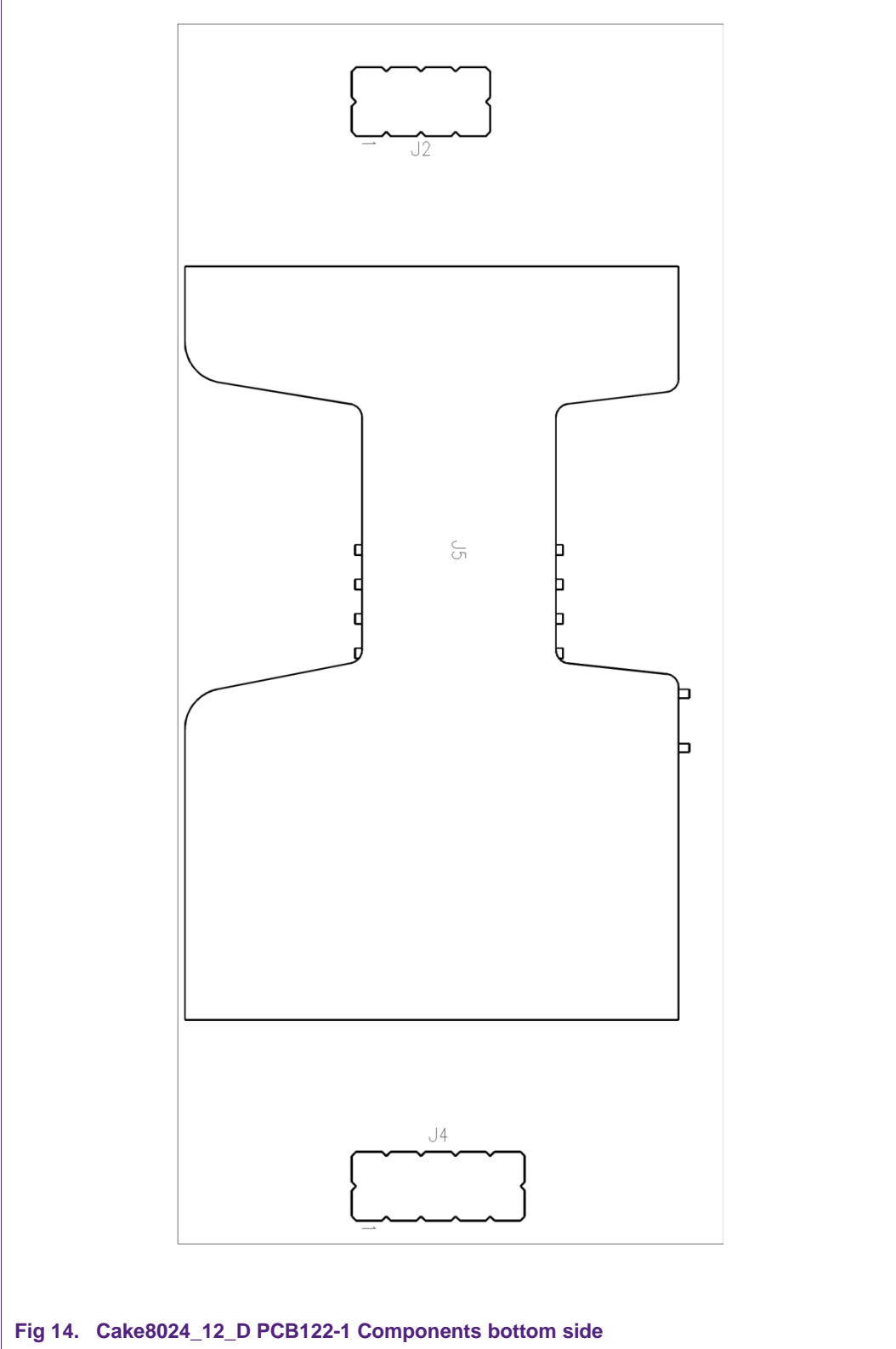
Fig 14. Cake8024_12_D PCB122-1 Components bottom side

Fig 15. Cake8024_12_D PCB1122-1 TOP LAYER

Fig 16.   Cake8024_12_D PCB1122-1 BOTTOM LAYER
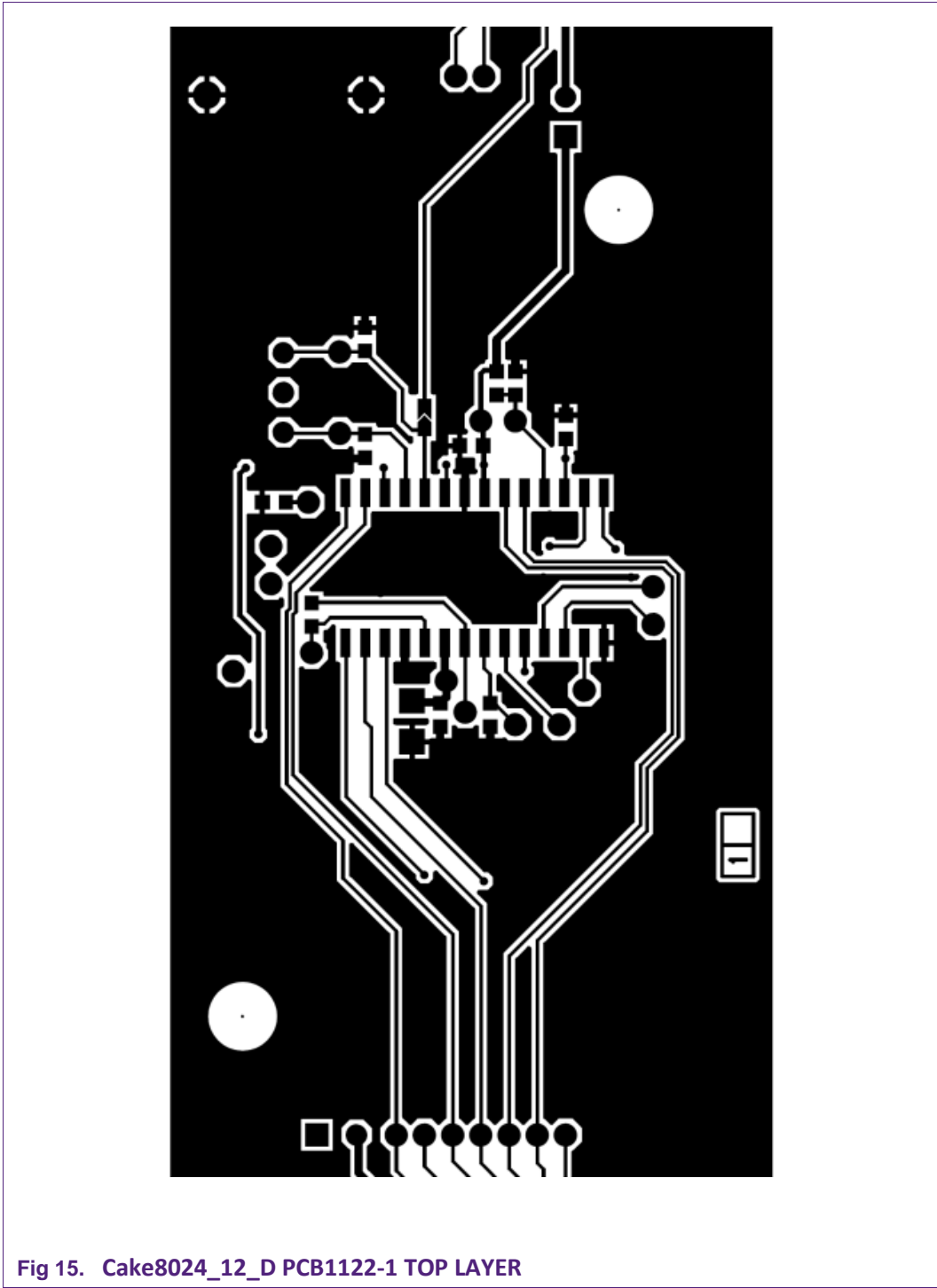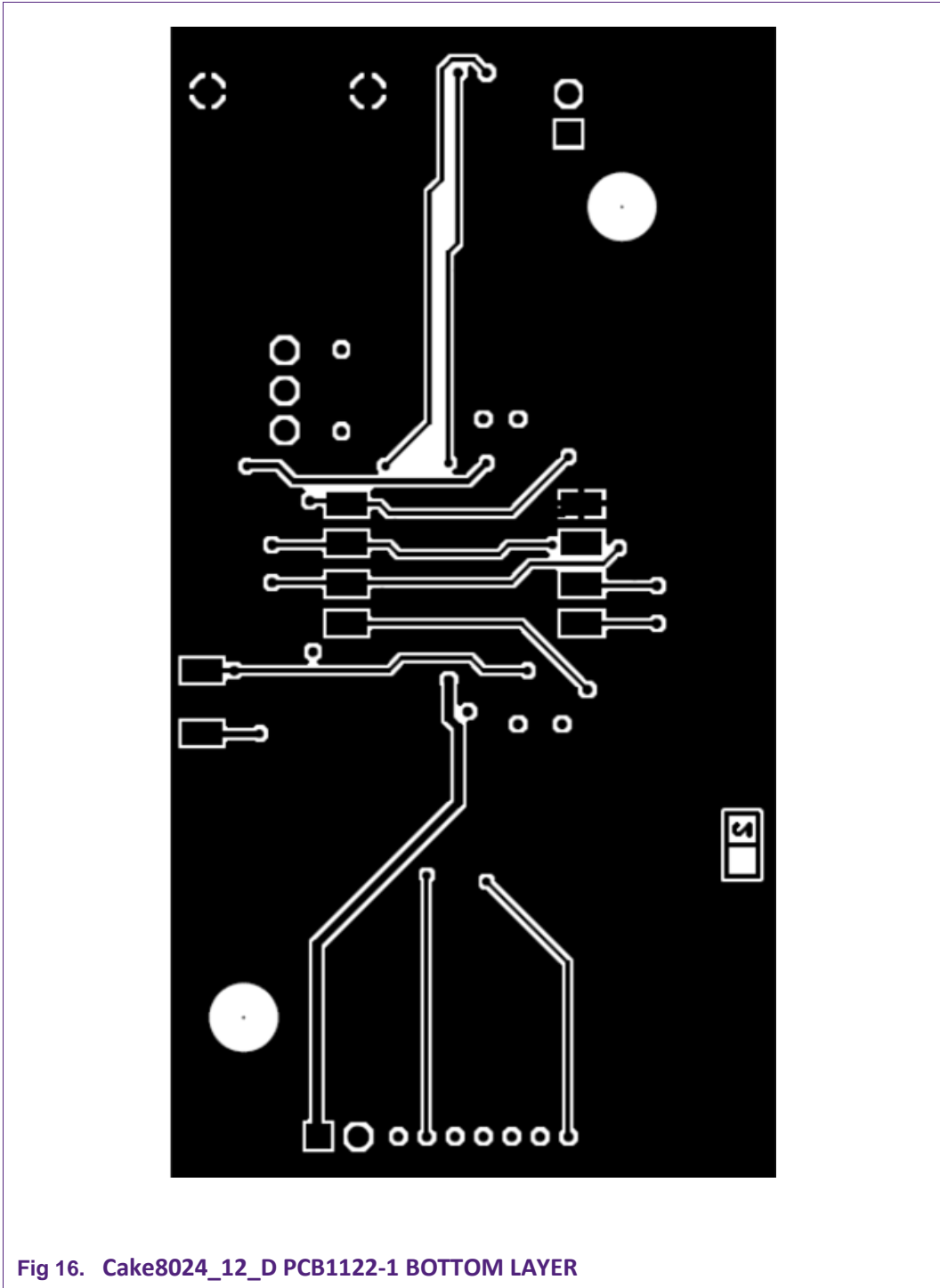
Table 4. **Bill of Materials for Cake8024_12_D**

Count	Reference	Geometry	Description
5	C3, C4, C5, C6, C8	c0603	100nF Capacitor X7R 0603 16V, 5%
1	C7	c0603	200nF Capacitor X7R 0603 16V, 10%
2	C2, C9	c0603	33pF Capacitor COG 0603 50V, 5%
1	C1	cap_320x160x160_a	10uF, Tantalum capacitor
2	ST1, ST4	cav_254_bar2md	Wire to board + Jumper
1	J2	con_bar_254_2x4_md	Bar2x4, Wire to board
1	J4	con_bar_254_2x5_md	Bar2x5, Wire to board
1	J5	con_itt_ccm01_2251	CCM01-2251, Card reader
1	ST2	cav_1016	CAV_10.16, Jumper, 10.16mm
1	R5	r0603	Resistor Package CMS 603 1% 0,1W
1	Y1	xtal_hc49s_plot	Quartz, package HC49/S, N.C.
1	R6	r0603	Resistor Package CMS 603 1% 0,1W, N.C.
1	IC1	so28_sot136_1	TDA8024T, package:so28
1			Circuit_imprime:BSX0190-1
2			Jumper_2.54mm:SAMTEC:SNT-100-BK-G
1			BULLE06:Jumper socket

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