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TECHNICAL DATA

MC6805R3
MC68HC05SR3

Technical Comparison

MC6805R3 and MC68HC05SR3

Introduction

This Technical Note will document the differences between the HCMOS MC68HC05SR3 and the NMOS MC6805R3. The MC68HC05SR3 is an enhanced HCMOS version of 6805R3. The device is pin compatible with the NMOS part. Due the differences in memory offset and instruction cycles, minor modification to existing R3 software is required.

Why use SR3?

The HCMOS SR3 has many advantages over the NMOS R3. These are listed below.

- The SR3 has a wider operating voltage range, from 3.0V to 5.5V; while the R3's operating voltage range is from 4.75V to 5.75V. The lower operating voltage also means a saving in power consumption.
- The CMOS SR3 has power saving modes. In the Stop mode, power consumption is only a few microamps. This is significantly less than the R3.
- The outputs of SR3 are TTL/CMOS compatible without mask option. The NMOS part requires mask option pull-ups for CMOS compatible outputs.
- Keyboard interrupts and pull-ups on SR3 is particularly suitable for hand-held products with keyboard inputs.
- The A/D on the SR3 can be switched off for power saving.
- The SR3 runs at a maximum bus speed of 2MHz, while the R3 is 1MHz.

The following sections will describe SR3 and R3 differences in more detail.

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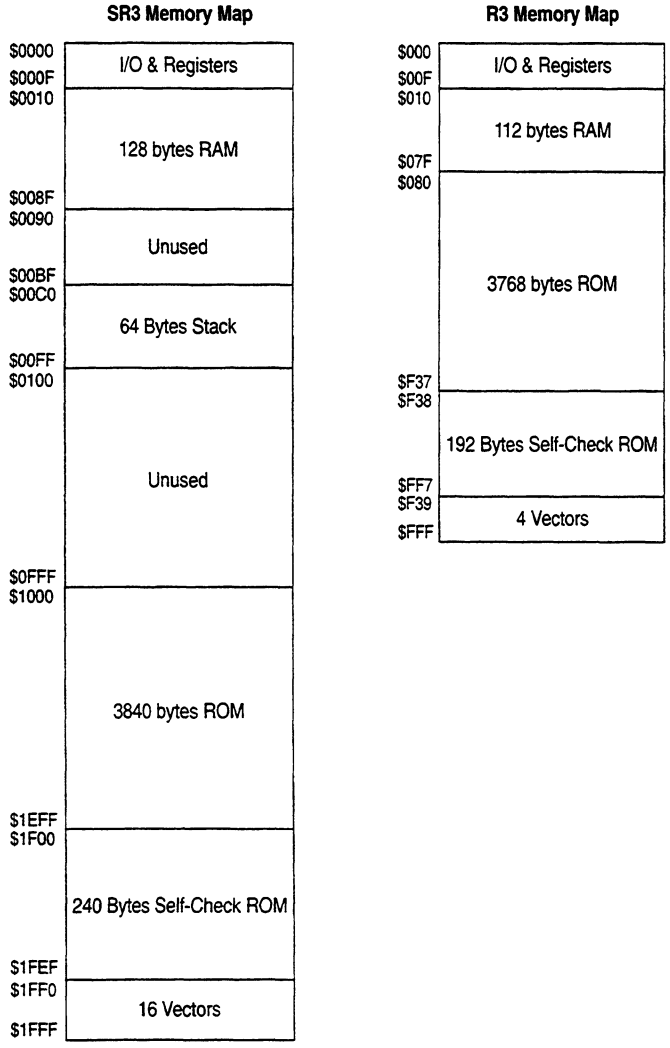
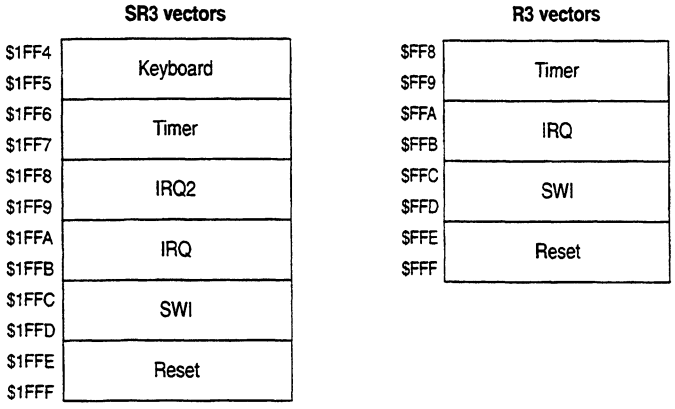
Memory Map

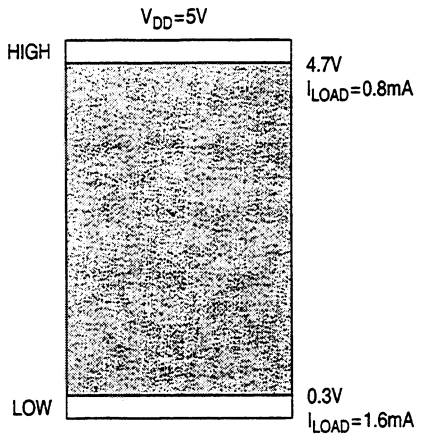


The RAM size of the SR3 is larger than R3. The start address of the ROM of the SR3 is $1000. The start address of the R3 ROM is $80. A relocation of the source code is required. The ROM size of the SR3 is slightly larger than the R3. The vector is also at different locations, therefore, a relocation is also required. Notice that an IRQ2 vector is added. In the R3, the IRQ2 and the timer shares the same interrupt vector. The user need to check the interrupt request bit of the Miscellaneous register (bit 7 of MR) and timer interrupt request bit (TIR) of the Timer Control register (bit 7 of TCR) to determine the source of interrupt. On the SR3, a negative edge on the $\overline{\text{IRQ2}}$ interrupt pin will generate a valid interrupt, the IRQ2 interrupt vector is then fetched.

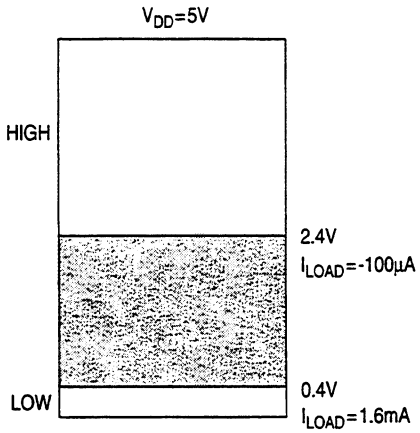


Input/Output

The input/output levels on the SR3 follows CMOS characteristics. Note that the output levels of the SR3 is higher than the R3. Both the driving capability and noise margin is enhanced. SR3 outputs can directly drive CMOS and TTL logic.

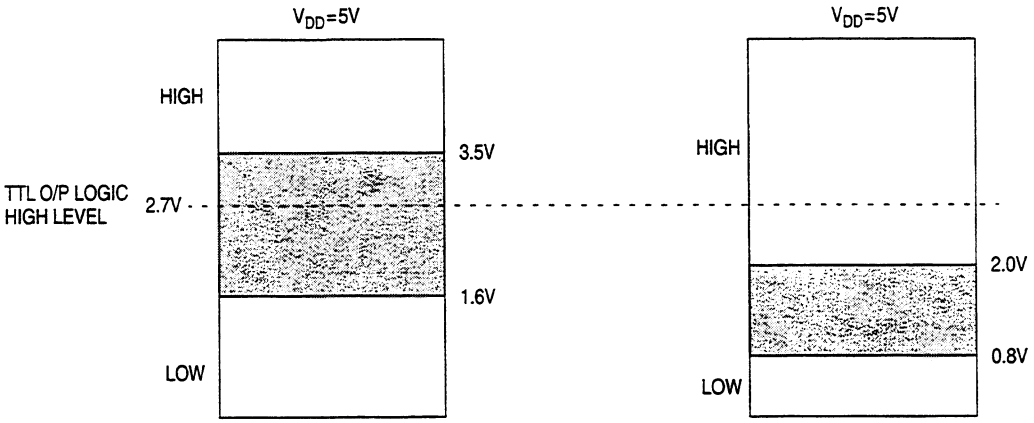


SR3 Output Characteristics



R3 Output Characteristics

The input level also has better noise margin. However, the input HIGH voltage is $0.7V_{DD}$ and this is 3.5V for a 5V supply. The minimum value of output HIGH for TTL logic is about 2.7V, therefore pull-ups are required for TTL outputs to drive SR3 inputs.



SR3 Input Characteristics

R3 Input Characteristics

In addition, port B has high current driving capability, therefore it can drive LEDs directly. The setting of the PIL bit of the Port Option Control register (bit 5 of address $000A) can configure PB5-7 to become 10mA drive port. This option is not selected at power-on.

Programmable Pull-ups and Keyboard Interrupts

A pull-up is available on each of the port pins at port A, B, C and D. A 20K pull-up on port B, port C and port D is activated by setting the PxP bit of the Port Option Control register. At power on, this option is turn off. In addition, a smaller pull up resistance on the PB1 and PB0 is available. Setting PB1, PB0 of Port Option Control register POPR will connect a 1.8K pull-up to PB1 and PB0.

Port Option Control Register	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	$000A	0	0	PIL	PDP	PCP	PBP	PB1	PB0

Port A pull-up and Interrupt

20KΩ internal pull-ups and interrupts are available on port A.

The following table summarizes the programmable pull-up options:

Pull-up and interrupt on Port A	Software programmable on KBIE and MCR
Pull-up on Port B	Software programmable on POPR
High current drive on Port B	Software programmable on POPR
Pull-up on Port C	Software programmable on POPR
Pull-up on Port D	Software programmable on POPR
Pull-up on $\overline{\text{RESET}}$ and $\overline{\text{IRQ}}$	Built-in

$\overline{\text{IRQ}}$ and $\overline{\text{IRQ2}}$

In SR3, IRQ is software programmable for either edge trigger only, or edge & level trigger by the INTO bit of the MCR and enabled/disabled by INTE of MCR. The IRQ of the NMOS R3 is edge trigger only. The IRQ2 of SR3 is enabled/disabled by setting the IRQ2E bit of MC. The interrupt status of IRQ2 is reflected by IRQ2F in the MCR. In the NMOS R3, the IRQ2 is controlled by the Miscellaneous register. The IRQ2 interrupt has an interrupt request bit (bit 7) and a mask bit (bit 6) in MR. Bits 5 to 0 in the MR are unused. The Miscellaneous register is located at $00A.

Low Voltage Reset

A low voltage reset is available on SR3, which can be enabled/disabled by software. This can be activated by setting the LVRE bit of the MCR. In R3, the low voltage reset/inhibit is set by mask option. The low voltage reset range for SR3 is 2.8V to 4.2V while the range for NMOS is 2.7V to 4.7V.

A/D Converter

The conversion time for the HCMOS SR3 is 32 machine cycles, while for NMOS R3 is 30 machine cycles. All the A/D channels on the NMOS R3 are input only. On SR3, when the A/D ports can be set as inputs or outputs when configured as general purpose I/O ports. Port D pins that are not selected by the A/D are controlled by the port I/O logic and thus used as general I/O. The DDR corresponding to an A/D channel used by the application must be cleared.

An ADRC bit in the A/D Status and Control register is available on the SR3. The RC oscillator should be selected when CPU bus frequency is below 1MHz. The A/D can also be turned on or off by ADON bit of the A/D Status and Control register. Setting this bit will enable the A/D, while and clearing this bit will turn off the A/D for power saving.

		Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SR3	A/D Control Register	$000E	COCO	ADRC	ADON	–	–	CH2	CH1	CH0

		Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
R3	A/D Control Register	$009	COCO	–	–	–	–	CH2	CH1	CH0

Timer

The prescaler on both the SR3 and R3 timers are programmable. But in R3, mask option is used to set the timer prescaler. On reset, the prescaler will be set to divide by128 for NMOS R3. On SR3 the default is divide by 16 at power on.

Power-up Delay

On the SR3, a power up delay is used to allow the oscillator to stabilize before the first instruction is executed. The delay can be selected by mask option. In the EPROM 705SR3, the delay is set by TMR2, TMR1, TMR0 bit of the MOR.

TIMR2	TIMR1	TIMR0	Delay (instruction cycles)
0	0	0	256
0	0	1	512
0	1	0	1024
0	1	1	2048
1	0	0	4096
1	0	1	8192
1	1	0	16384
1	1	1	32768

Bus Frequency

The bus frequency prescalers are different on the two devices. The bus frequency for R3 is crystal frequency divided by 4. The bus frequency for SR3 is crystal frequency divided by 2. Also note that the instruction execution cycle time is different between the SR3 and R3. Hence, routines used for timing purposes will have to be modified.

Read-modified Write on DDR

In the NMOS R3, the DDRs are write-only registers. A read operation on these registers are undefined. Since BSET and BCLR are read-modify write instructions, they cannot be used to set a data direction register bit. However, on the HCMOS SR3, the DDRs are read/write registers, therefore BSET and BCLR can be used.

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How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

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