



# 24-Bit UFm 5 MHz I<sup>2</sup>C-Bus 100 mA 40 V LED Driver

## PCU9656B

### Archived

このページには、製造中止（生産終了）となった製品の情報が記載されています。本ページに記載されている仕様および情報は、過去の参考情報です。

Last Updated: Sep 11, 2024

The PCU9656 is a UFm I<sup>2</sup>C-bus controlled 24-bit LED driver optimized for voltage switch dimming and blinking 100 mA Red/Green/Blue/Amber (RGBA) LEDs. Each LEDn output has its own 8-bit resolution (256 steps) fixed frequency individual PWM controller that operates at 97 kHz (typical) with a duty cycle that is adjustable from 0 % to 99.6 % to allow the LED to be set to a specific brightness value. An additional 8-bit resolution (256 steps) group PWM controller has both a frequency of 190 Hz and an adjustable frequency between 24 Hz to once every 10.73 seconds with a duty cycle that is adjustable from 0 % to 99.6 % that is used to either dim or blink all LEDs with the same value.

Each LEDn output can be off, on (no PWM control), set at its individual PWM controller value or at both individual and group PWM controller values. The PCU9656 operates with a supply voltage range of 2.3 V to 5.5 V and the 100 mA open-drain outputs allow voltages up to 40 V for the LED supply.

The PCU9656 is one of the first LED controller devices in a new Ultra Fast-mode (UFm) family. UFm devices offer higher frequency (up to 5 MHz).

The active LOW Output Enable input pin (OE) blinks all the LEDs outputs and can be used to externally PWM the outputs, which is useful when multiple devices need to be dimmed or blinked together without using software control.

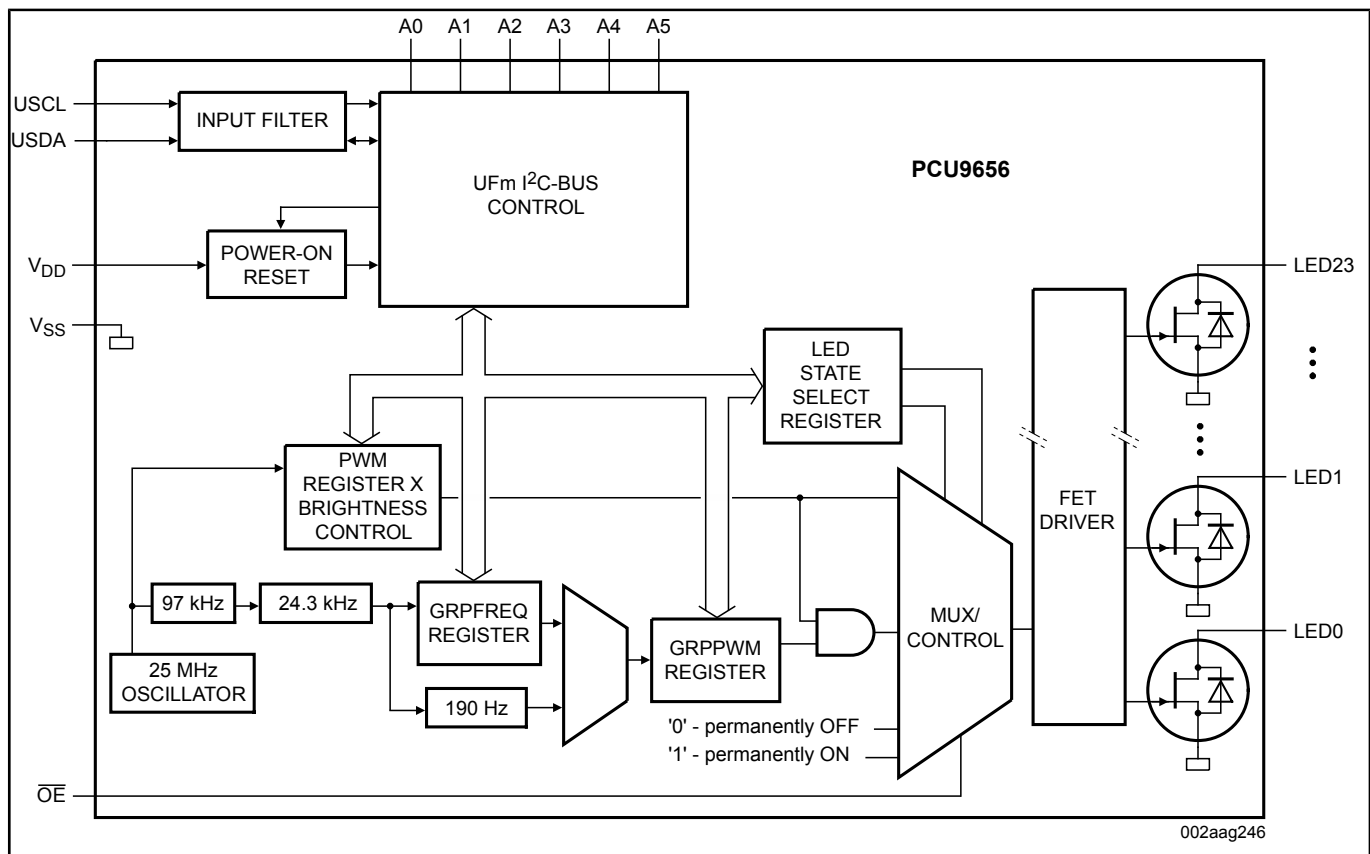
Software programmable LED Group and three Sub Call I<sup>2</sup>C-bus addresses allow all or defined groups of PCU9656 devices to respond to a common I<sup>2</sup>C-bus address, allowing, for example, all

red LEDs to be turned on or off at the same time or marquee chasing effect, thus minimizing I<sup>2</sup>C-bus commands. Six hardware address pins allow up to 64 devices on the same bus.

The Software Reset (SWRST) Call allows the controller to perform a reset of the PCU9656 through the I<sup>2</sup>C-bus, identical to the Power-On Reset (POR) that initializes the registers to their default state causing the output NAND FETs to be OFF (LED off). This allows an easy and quick way to reconfigure all device registers to the same condition.

A new feature to control LEDn output pattern is incorporated in the PCU9656. A new control byte called 'Chase Byte' allows enabling or disabling of selective LEDn outputs depending on the value of the Chase Byte. This feature greatly reduces the number of bytes to be sent to the PCU9656 when repetitive patterns need to be displayed as in creating a marquee chasing effect.

## 24-Bit U<sup>F</sup>m 5 MHz I<sup>2</sup>C-Bus 100 MA 40 V LED Driver Block Diagram



View additional information for [24-Bit U<sup>F</sup>m 5 MHz I<sup>2</sup>C-Bus 100 MA 40 V LED Driver](#).

**Note:** The information on this document is subject to change without notice.

---

**[www.nxp.com](http://www.nxp.com)**

NXP and the NXP logo are trademarks of NXP B.V. All other product or service names are the property of their respective owners. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. © 2025 NXP B.V.