

4-Bit I²C-Bus and SMBus Low-Power I/O Port with Interrupt and Reset

PCA9537DP

Last Updated: Mar 2, 2023

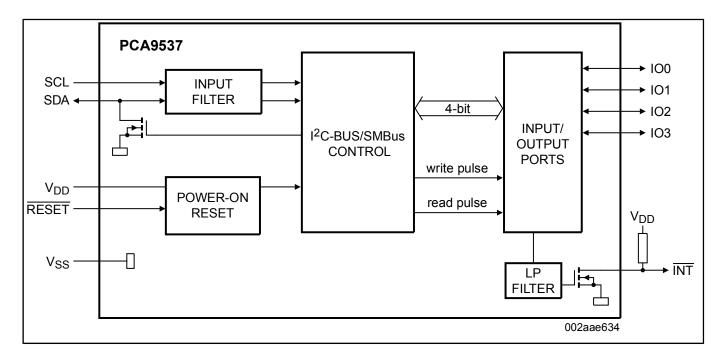
The PCA9537 is a 10-pin CMOS device that provides 4 bits of General Purpose parallel Input/ Output (GPIO) expansion with interrupt and reset for I²C-bus/SMBus applications and was developed to enhance the NXP Semiconductors family of I²C-bus I/O expanders. I/O expanders provide a simple solution when additional I/O is needed for ACPI power switches, sensors, push-buttons, LEDs, fans, etc.

The PCA9537 consists of a 4-bit Configuration register (input or output selection), 4-bit Input Port register, 4-bit Output Port register and a 4-bit Polarity Inversion register (active HIGH or active LOW operation). The system controller can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input Port or Output Port register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system controller.

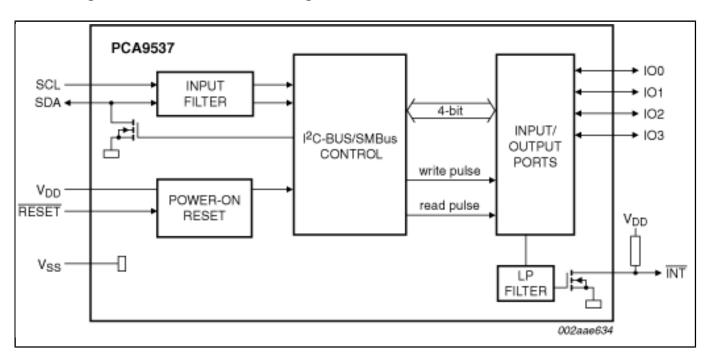
The PCA9537 open-drain interrupt output (INT) is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system controller that an input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine. The RESET pin causes the same reset/initialization to occur without de-powering the device.

The I²C-bus address is fixed and allows only one device on the same I²C-bus/SMBus.

PCA9537 Block Diagram Block Diagram



Block diagram: PCA9537DP Block Diagram



View additional information for 4-Bit I²C-Bus and SMBus Low-Power I/O Port with Interrupt and Reset.

Note: The information on this document is subject to change without notice.

www.nxp.comNXP and the NXP logo are trademarks of NXP B.V. All other product or service names are the property of their respective owners. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. © 2024 NXP B.V.