Simple Two-Wire Bus Buffer

PCA9525

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The PCA9525 is a monolithic CMOS integrated circuit for bus buffering in applications including I²C-bus, SMBus, DDC, PMBus, and other systems based on similar principles.

The buffer extends the bus load limit by buffering both the SCL and SDA lines, allowing the maximum permissible bus capacitance on both sides of the buffer.

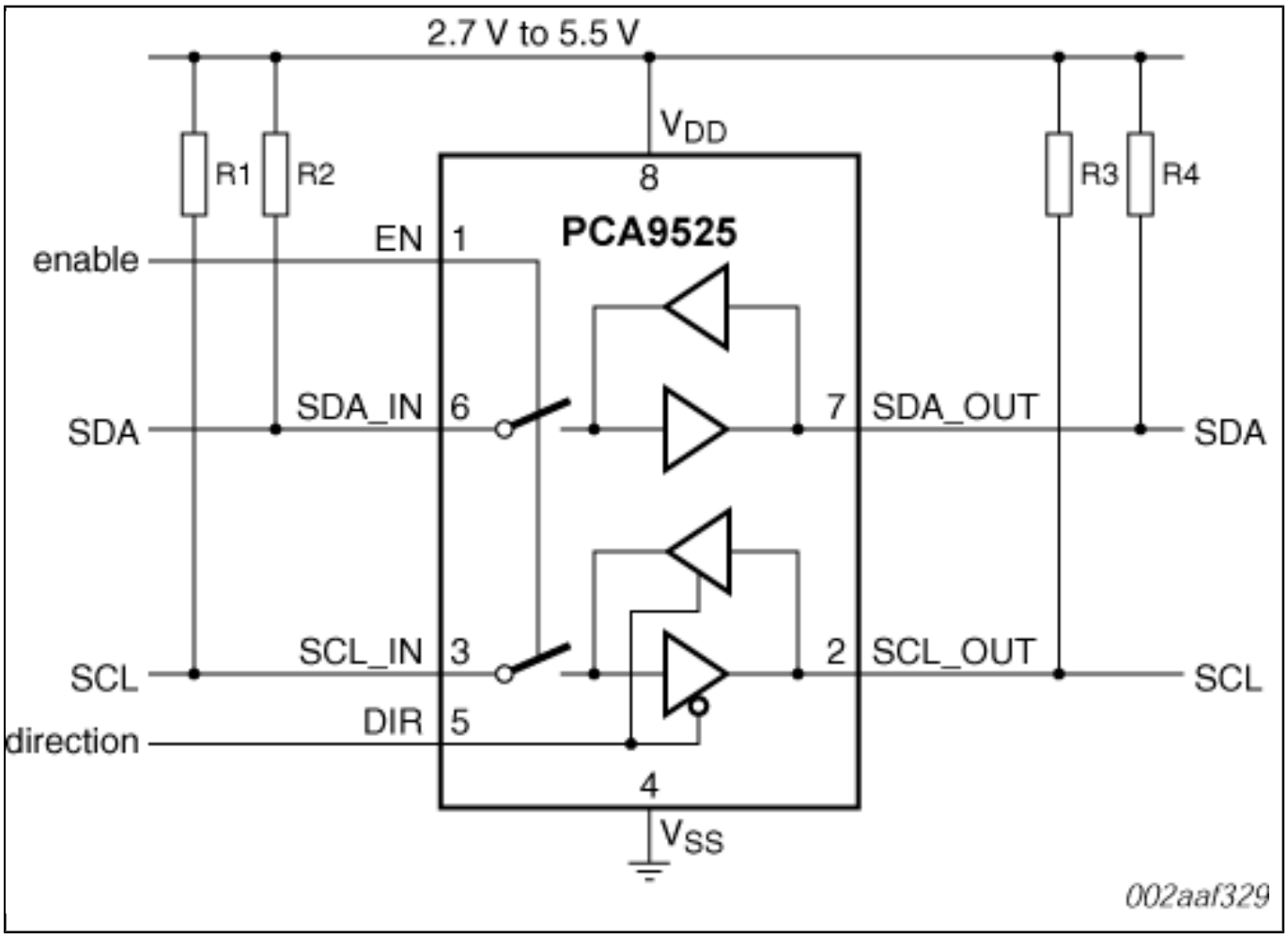
The PCA9525 includes a unidirectional buffer for the clock signal, and a bidirectional buffer for the data signal. Target devices which employ clock stretching are therefore not supported.

In its most basic implementation, the buffer will allow an extended number of target devices to be attached to one (or more) controller devices. In this case, all controller devices would be positioned on the Sxx_IN side of the PCA9525.

The direction pin (DIR) further enhances this function by allowing the unidirectional clock signal to be reversed, thus allowing controller devices on both sides of the buffer.

The enable (EN) function allows sections of the bus to be isolated. Individual parts of the system can be brought on-line successively. This means a controlled start-up using a diverse range of components, operating speeds and loads is easily achieved.

PCA9525 Block Diagram



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Note: The information on this document is subject to change without notice.