5-Channel I²C-Bus Hub

PCA9516A

Last Updated: Mar 15, 2024

The PCA9516A is a CMOS integrated circuit intended for application in I²C-bus and SMBus systems.

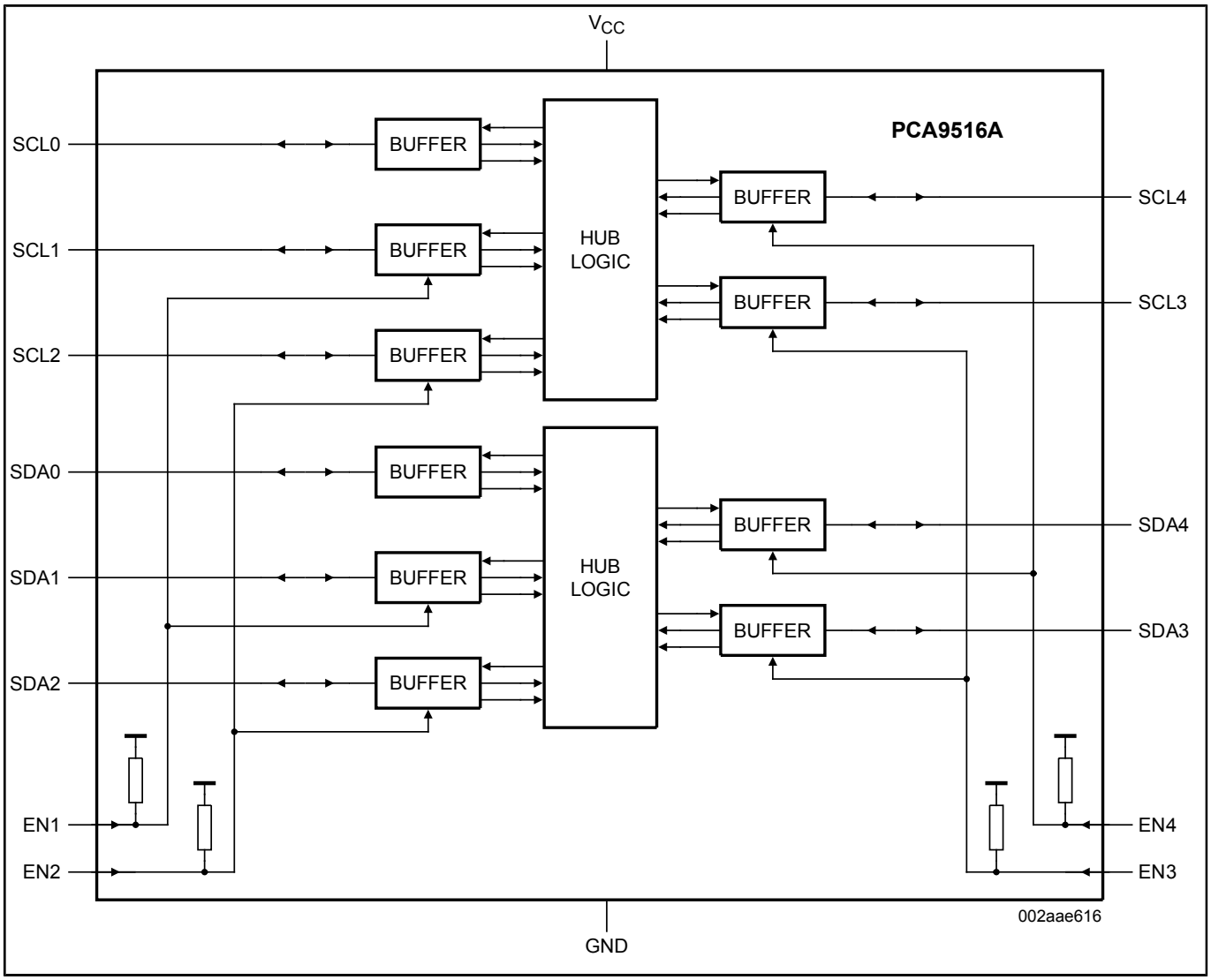
While retaining all the operating modes and features of the I²C-bus system, it permits extension of the I²C-bus by buffering both the data (SDAn) and the clock (SCLn) lines, thus enabling five buses of 400 pF.

The I²C-bus capacitance limit of 400 pF restricts the number of devices and bus length. Using the PCA9516A enables the system designer to divide the bus into five segments off of a hub where any segment-to-segment transition sees only one repeater delay.

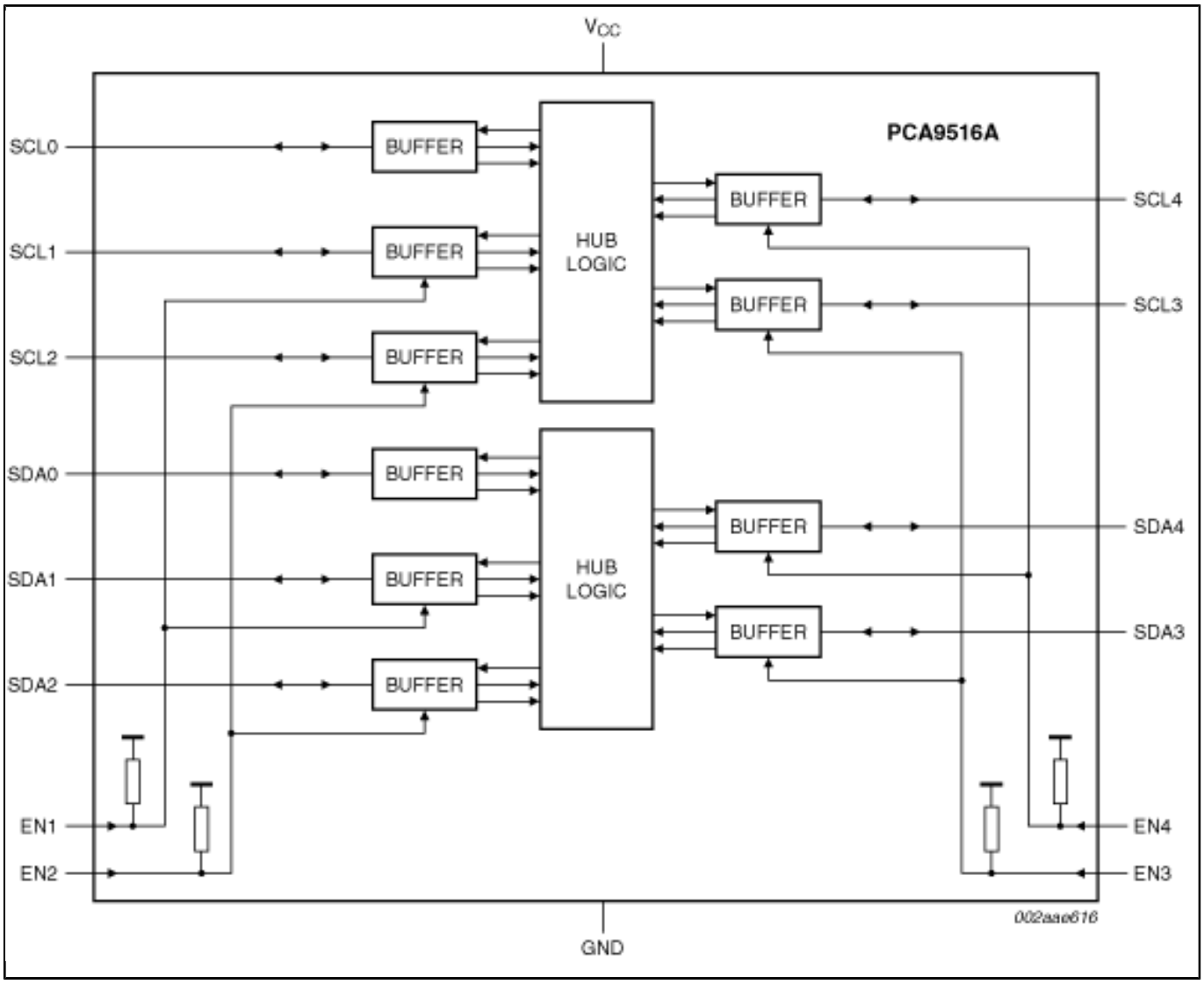
It can also be used to run different buses at 5 V and 3.3 V or 400 kHz and 100 kHz buses where the 100 kHz bus is isolated when 400 kHz operation of the other bus is required.

Two or more PCA9516A's cannot be put in series. The PCA9516A design does not allow this configuration. Since there is no direction pin, slightly different 'legal' low voltage levels are used to avoid lock-up conditions between the input and the output of each repeater in the hub. A 'regular LOW' applied at the input of a PCA9516A will be propagated as a 'buffered LOW' with a slightly higher value on all the enabled outputs. When this 'buffered LOW' is applied to another PCA9515A, PCA9516A, or PCA9518A in series, the second PCA9515A, PCA9516A, or PCA9518A will not recognize it as a 'regular LOW' and will not propagate it as a 'buffered LOW' again. The PCA9510A/9511A/9513A/9514A and PCA9512A cannot be used in series with the PCA9515A, PCA9516A, or PCA9518A, but can be used in series with themselves since they use shifting instead of static offsets to avoid lock-up conditions.

PCA9516A Block Diagram Block Diagram



Block diagram: PCA9516AD, PCA9516APW Block Diagram



View additional information for 5-Channel I²C-Bus Hub.

Note: The information on this document is subject to change without notice.