I²C-Bus Repeater

PCA9515

Archived

このページには、製造中止（生産終了）となった製品の情報が記載されています。本ページに記載されている仕様および情報は、過去の参考情報です。

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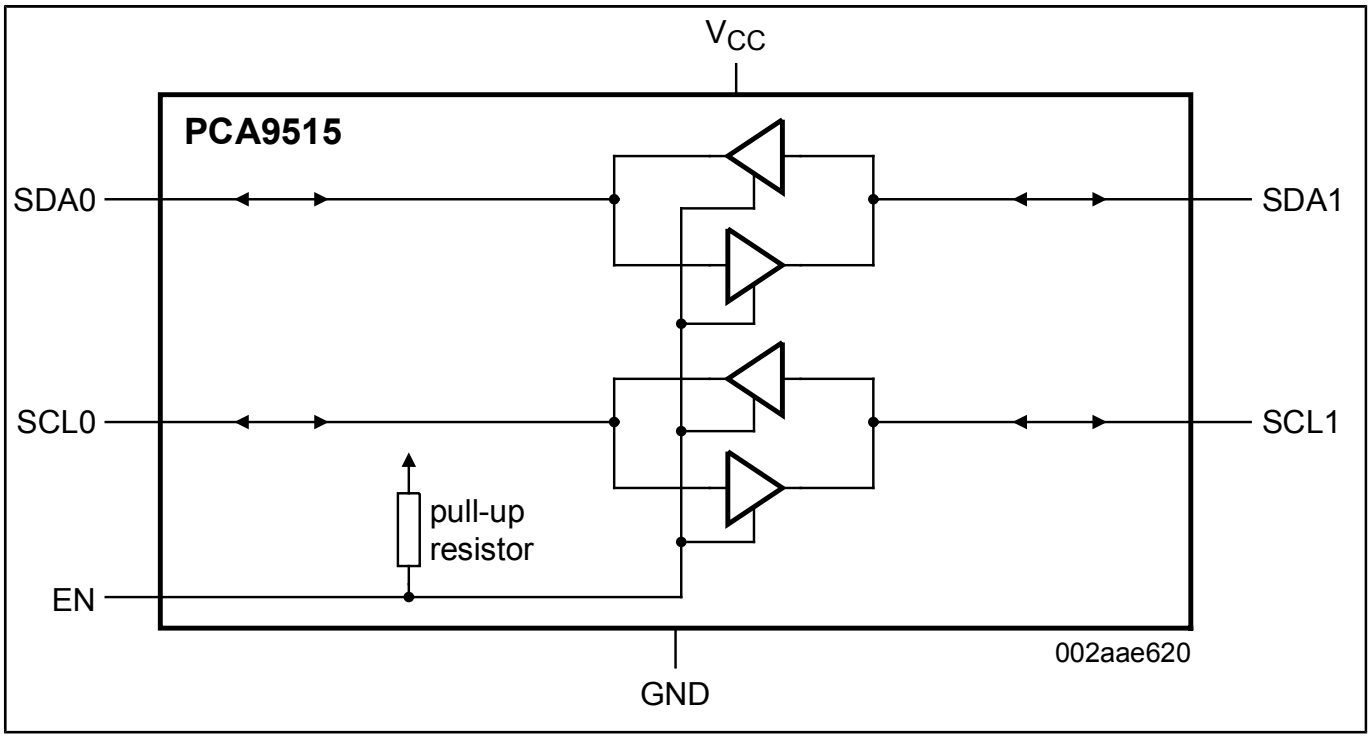
The PCA9515 is a BiCMOS integrated circuit intended for application in I²C-bus and SMBus systems.

While retaining all the operating modes and features of the I²C-bus system, it permits extension of the I²C-bus by buffering both the data (SDAn) and the clock (SCLn) lines, thus enabling two buses of 400 pF.

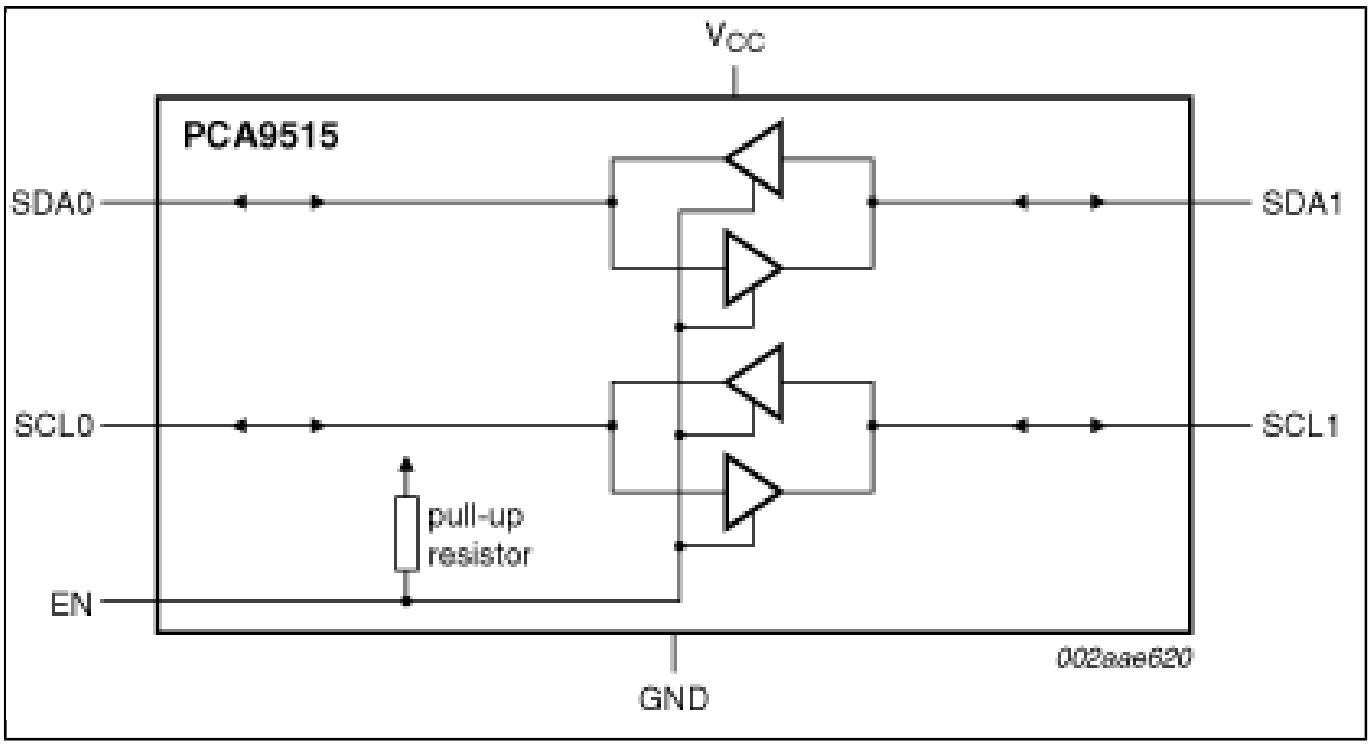
The I²C-bus capacitance limit of 400 pF restricts the number of devices and bus length. Using the PCA9515 enables the system designer to isolate two halves of a bus, thus more devices or longer length can be accommodated. It can also be used to run two buses, one at 5 V and the other at 3.3 V or a 400 kHz and 100 kHz bus, where the 100 kHz bus is isolated when 400 kHz operation of the other is required.

Two or more PCA9515's cannot be put in series. The PCA9515 design does not allow this configuration. Since there is no direction pin, slightly different 'legal' low voltage levels are used to avoid lock-up conditions between the input and the output. A 'regular low' applied at the input of a PCA9515 will be propagated as a 'buffered low' with a slightly higher value. When this 'buffered low' is applied to another PCA9515, PCA9516A, or PCA9518A in series, the second PCA9515, PCA9516A, or PCA9518A will not recognize it as a 'regular low' and will not propagate it as a 'buffered low' again. The PCA9510A/9511A/9513A/9514A and PCA9512A cannot be used in series with the PCA9515, PCA9516A, or PCA9518A but can be used in series with themselves since they use shifting instead of static offsets to avoid lock-up conditions.

PCA9515 Block Diagram Block Diagram



PCA9515D, PCA9515DP Block Diagram Block Diagram



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Note: The information on this document is subject to change without notice.

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