Hot Swappable Level Translating I²C-Bus Repeater

PCA9508

Last Updated: Jun 17, 2025

The PCA9508 is a CMOS integrated circuit that supports hot-swap with zero offset and provides level shifting between low voltage (down to 0.9 V) and higher voltage (2.7 V to 5.5 V) for I²C-bus or SMBus applications. While retaining all the operating modes and features of the I²C-bus system during the level shifts, it also permits extension of the I²C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, thus enabling two buses of 400 pF. Using the PCA9508 enables the system designer to isolate two halves of a bus for both voltage and capacitance, and perform hot-swap and voltage level translation. Furthermore, the dual supply pins can be powered up in any sequence; when any of the supply pins are unpowered, the 5 V tolerant I/O are high-impedance.

The hot swap feature allows an I/O card to be inserted into a live backplane without corrupting the data and clock buses. Control circuitry prevents the backplane from being connected to the card until a stop command or bus idle occurs on the backplane without bus contention on the card. Zero offset output voltage allows multiple PCA9508s to be put in series and still maintains an excellent noise margin.

PCA9508 has B side and A side bus drivers. The 2.7 V to 5.5 V bus B side drivers behave much like the drivers on the PCA9515A device, while the adjustable voltage bus A side drivers drive more current and incur no static offset voltage. This results in a LOW on the B side translating into a nearly 0 V LOW on the A side.

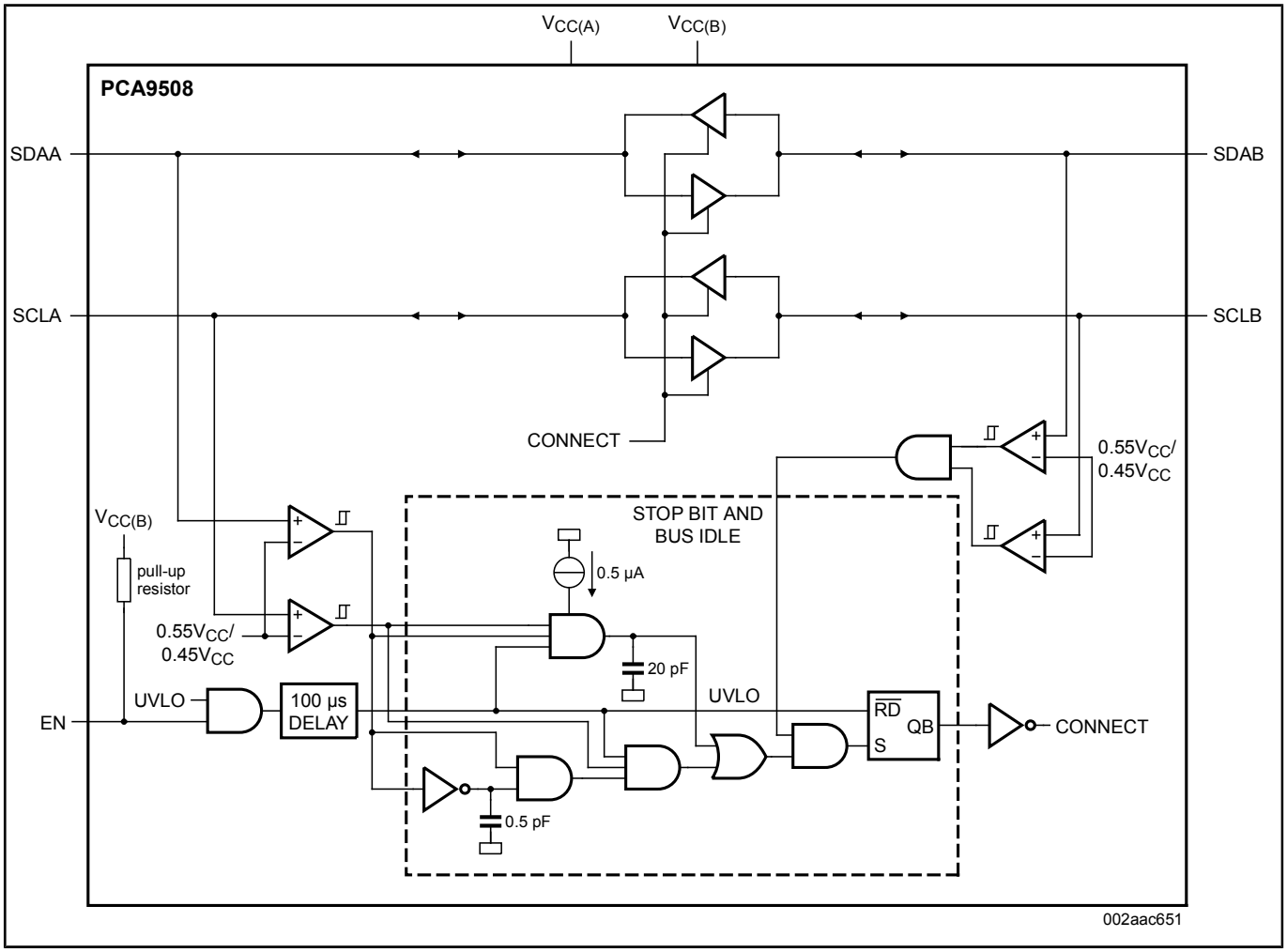
The static offset design of the B side PCA9508 I/O drivers prevents them from being connected to another device that has a rise time accelerator including the PCA9510/A, PCA9511/A, PCA9512/A, PCA9513/A, or PCA9514/A or a static offset voltage including the PCA9507 (B side), PCA9508 (B side), PCA9509 (A side), PCA9515/A, PCA9516A, PCA9517/A (B side), PCA9518, PCA9519 (A side), or P82B96/PCA9600 (Sx/Sy side). The A side of two or more PCA9508s can be connected together, however, to allow a star topology with the A side on the common bus, and the A side can be connected directly to any other buffer with static or dynamic

offset voltage. Multiple PCA9508s can be connected in series, A side to B side, with no build-up in offset voltage with only time-of-flight delays to consider.

The PCA9508 drivers are not enabled unless the bus is idle, VCC(A) is above 0.8 V and VCC(B) is above 2.5 V. The EN pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the enable pin when the bus is idle.

The output pull-down on the B side internal buffer LOW is set for approximately 0.5 V, while the input threshold of the internal buffer is set about 70 mV lower (0.43 V). When the B side I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring. The output pull-down on the A side drives a hard LOW and the input level is set at 0.5VCC(A) to accommodate the need for a lower LOW level in systems where the low voltage side supply voltage is as low as 0.9 V.

PCA9508 Block Diagram



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