2-bit I3C Bus Buffer with Voltage Level Translation Evaluation Board

P3B1602-EVB NEW

Preproduction

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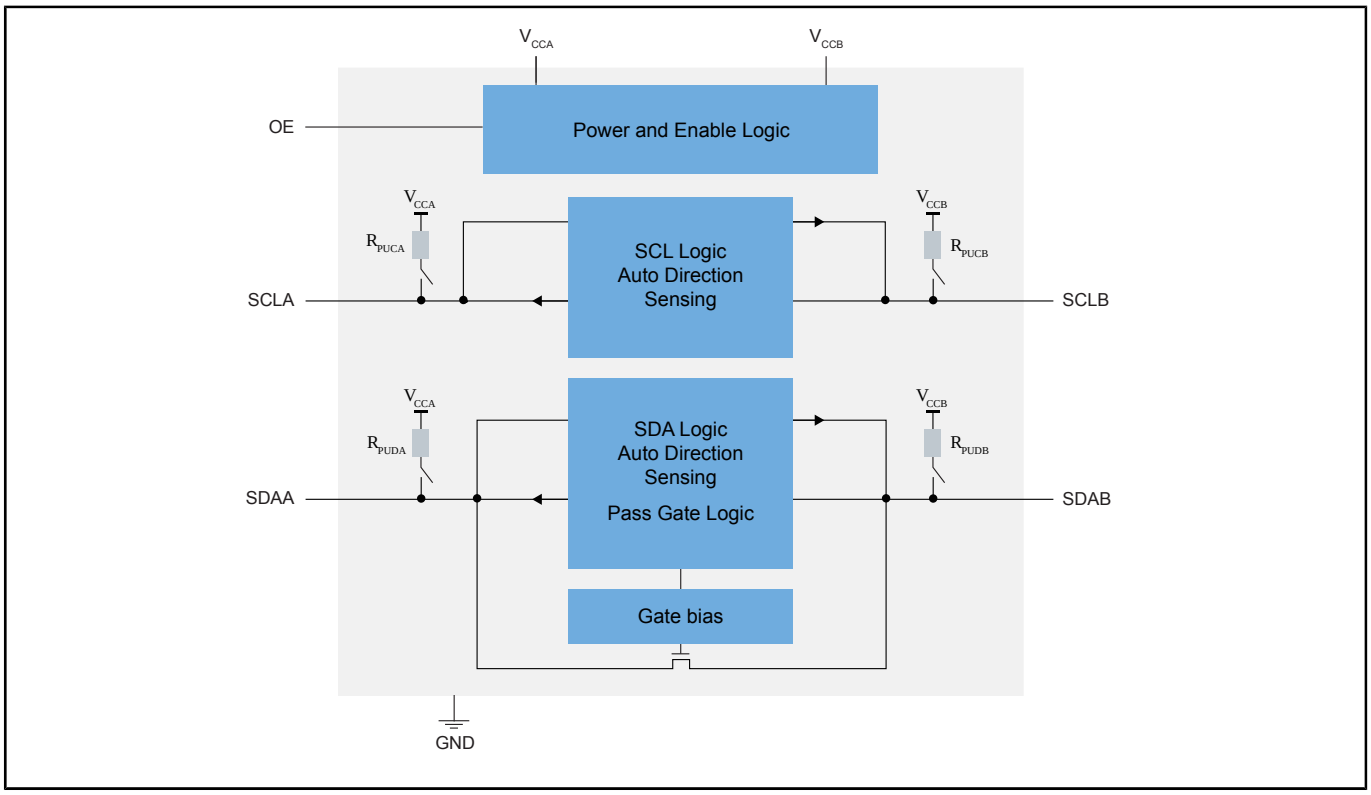
The P3B1602DP-EVB evaluation board is designed to enable easy testing, validation, and design-in of the P3B1602DP, a 2-bit I3C buffer with integrated auto-direction sensing and bidirectional voltage-level translation.

The standalone evaluation board is populated with series resistors that can be reworked during evaluation. It also supports the selection of different capacitive loads, allowing performance evaluation under various bus-loading conditions.

Evaluation Board Circuit Block Diagram



View additional information for 2-bit I3C Bus Buffer with Voltage Level Translation Evaluation Board.

Note: The information on this document is subject to change without notice.