Low-Power PowerQUICC® II Pro Processor with DDR2, TDM, PCI, Security, USB, QUICC Engine®

MPC8321

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The MPC8321 PowerQUICC® II Pro is part of the MPC8323E family of cost-effective network communication processors that meet the requirements of several small office/home office (SOHO), broadband access, routers and industrial control applications. It provides better CPU performance, additional functionality and faster interfaces than current PowerQUICC processors while addressing important time to market, price, power consumption and board real estate requirements.

Core Complex The MPC8321 incorporates a unique configuration of the e300c2 (MPC603e-based) core. While this version of e300 core does not have a floating point unit (FPU), it has been designed to include dual integer units as well as a modified multiply instruction. These architectural enhancements enable more efficient operations to be executed in parallel, resulting in significant performance improvement. The core also includes 16 KB of L1 instruction and data caches and on-chip memory management units (MMUs). The MPC8321 includes a 32-bit PCI controller, four DMA channels, a flexible local bus and a 32-bit DDR-1/DDR-2 SDRAM memory controller.

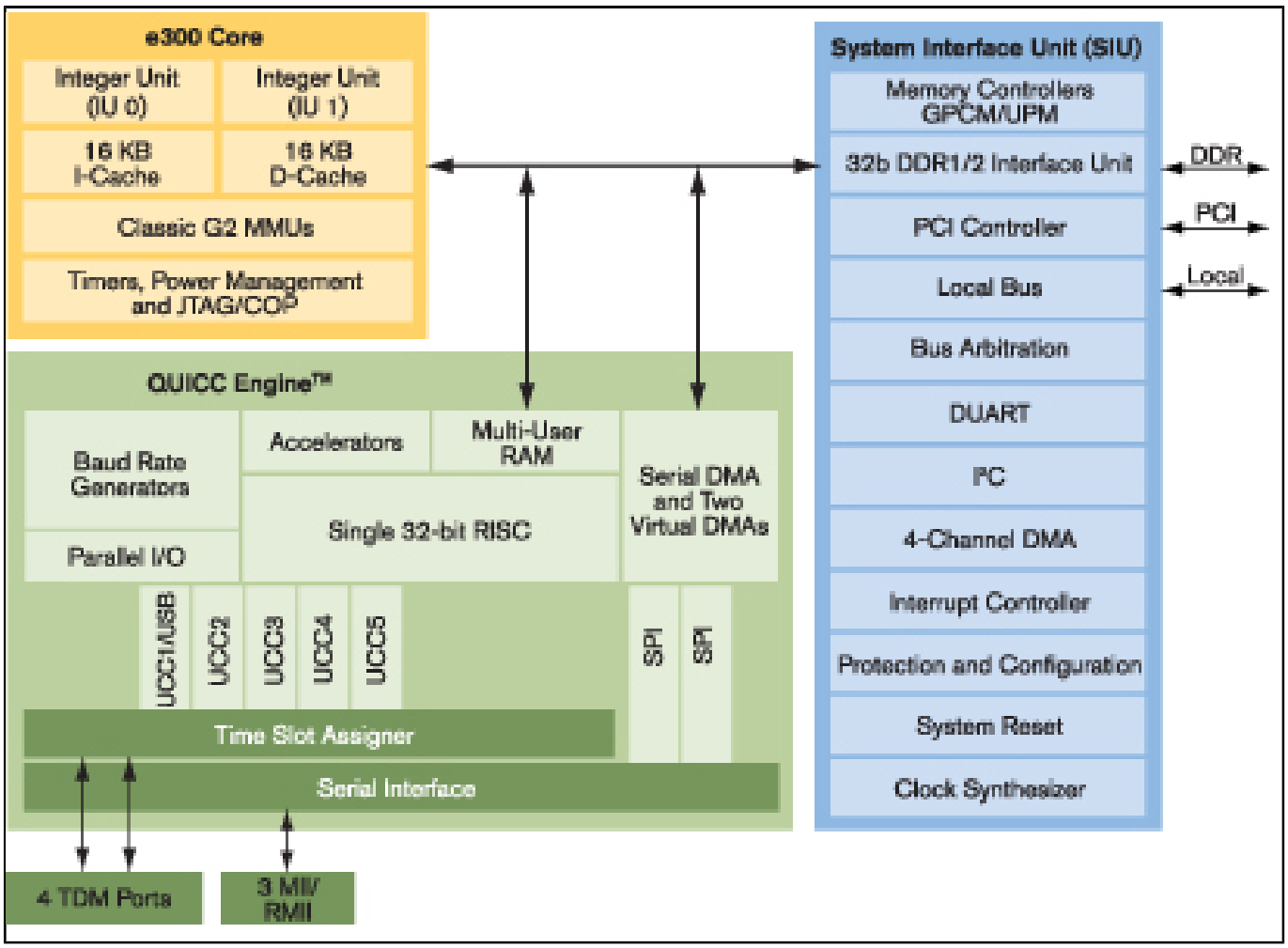
QUICC Engine® Technology A new single-reduced instruction set computing (RISC) version of the QUICC Engine communications engine forms the heart of the networking capability of the MPC8321. The QUICC Engine block contains several peripheral controllers and a single 32-bit RISC controller. Unique microcode packages provide support for network address port translation (NAPT), firewall, IPsec and advanced quality of service (QoS). Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs). Each of the five UCCs can support a variety of communication protocols:

- Up to three 10/100 Mbps Ethernet
- High-level data link control (HDLC)

- Up to four time division multiplexing (TDM)
- Binary synchronous communications protocol (BISYNC)
- UCC can also support USB 2.0 (full/low-speed)

System Interface Unit The MPC8321 family also includes a 32-bit double data rate (DDR)-1/ DDR/2 memory controller, a 32-bit peripheral component interconnect (PCI) controller, a 16-bit local bus and four direct memory access (DMA) channels.

MPC8321 Block Diagram Block Diagram



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Note: The information on this document is subject to change without notice.

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