Layerscape® 1020A and 1022A Dual-Core Processors

LS1020A
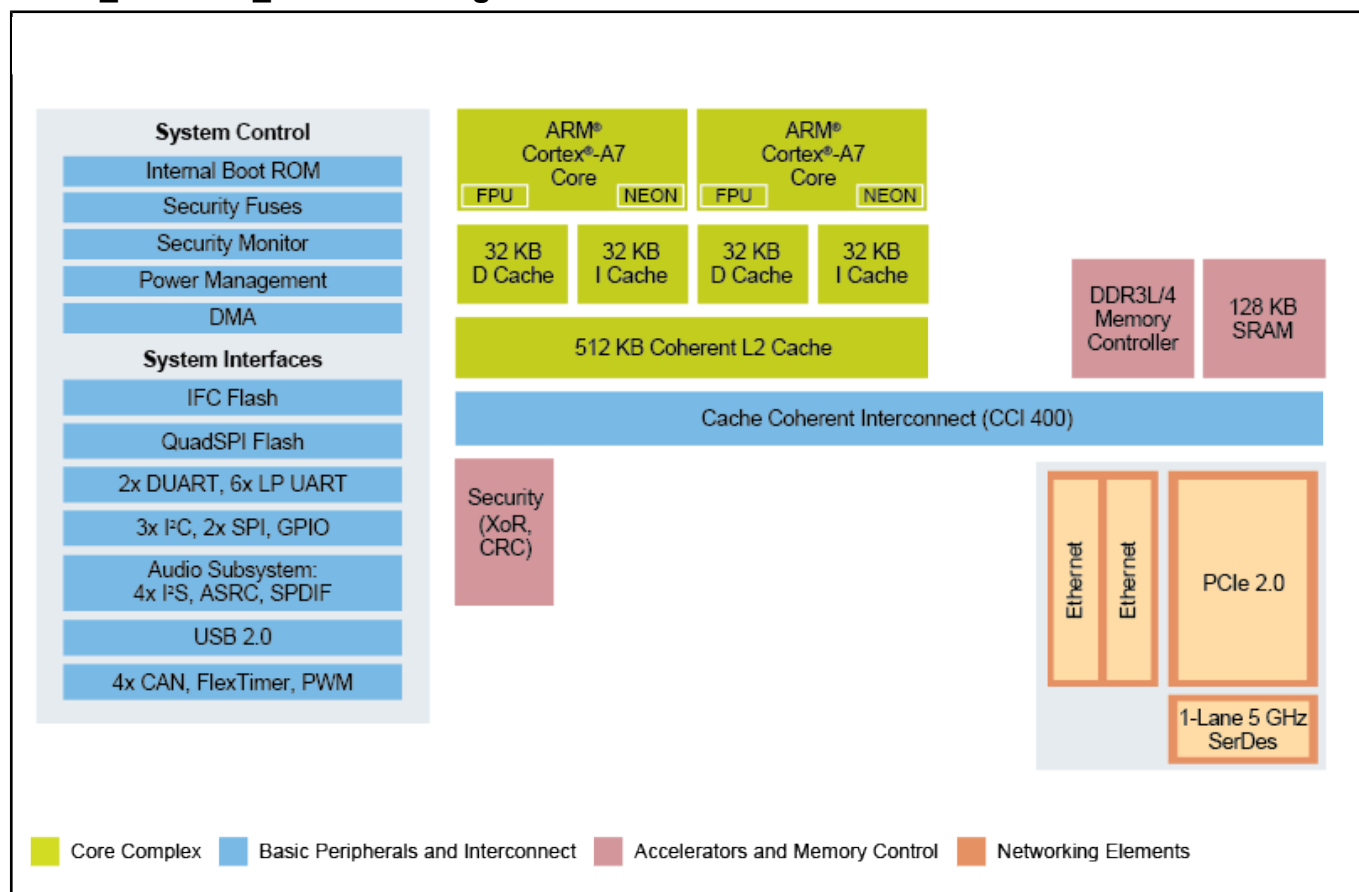
Last Updated: Sep 5, 2025

The LS1 family, which includes the LS1020A and LS1022A communications processors, is built on Layerscape architecture, the industry's first software-aware, core-agnostic networking architecture to offer unprecedented efficiency and scale.

Members of the value-performance tier, the LS1020A and LS1022A processors provide extensive integration and power efficiency for fanless, small form factor enterprise and consumer networking applications. Incorporating dual Arm® Cortex®-A7 cores running up to 1.2 GHz, the LS1020A and LS1022A processors deliver pre-silicon CoreMark® performance of over 7,000, as well as virtualization support, advanced security features and broadest array of high-speed interconnects and optimized peripheral features ever offered in a sub-3 W processor (LS1022A processor is sub-2W typical).
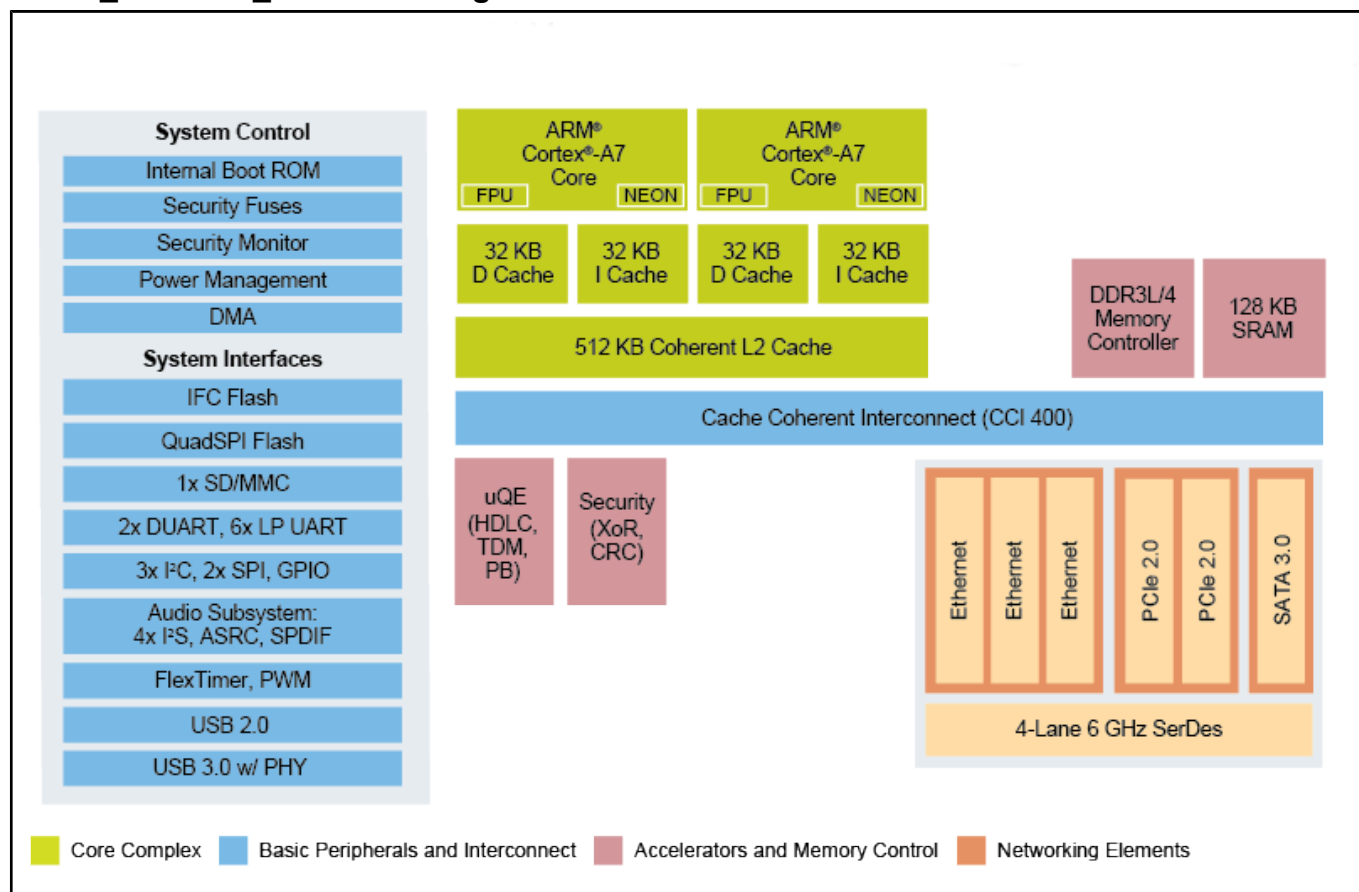
The LS1020A and LS1022A processors features support for multiple industrial protocols, DDR3L/4 running up to 1600 MHz, integrated hardware-based security engine and QUICC Engine®. and ECC protection on both L1 and L2 caches. The LS1020 and LS1022A processors are pin- and software-compatible with the LS1021A processor.

Layerscape processors are part of NXP's EdgeVerse™ edge computing platform.

29841_LS1022A_BD Block Diagram

System Control
- Internal Boot ROM
- Security Fuses
- Security Monitor
- Power Management
- DMA

System Interfaces
- IFC Flash
- QuadSPI Flash
- 2x DUART, 6x LP UART
- 3x I²C, 2x SPI, GPIO
- Audio Subsystem: 4x I²S, ASRC, SPDIF
- USB 2.0
- 4x CAN, FlexTimer, PWM

ARM® Cortex®-A7 Core — FPU, NEON
ARM® Cortex®-A7 Core — FPU, NEON

32 KB D Cache | 32 KB I Cache | 32 KB D Cache | 32 KB I Cache

512 KB Coherent L2 Cache

DDR3L/4 Memory Controller
128 KB SRAM

Cache Coherent Interconnect (CCI 400)

Security (XoR, CRC)

Ethernet | Ethernet | PCIe 2.0

1-Lane 5 GHz SerDes

Legend:
- Core Complex
- Basic Peripherals and Interconnect
- Accelerators and Memory Control
- Networking Elements

29841_LS1020A_BD Block Diagram

System Control
- Internal Boot ROM
- Security Fuses
- Security Monitor
- Power Management
- DMA

System Interfaces
- IFC Flash
- QuadSPI Flash
- 1x SD/MMC
- 2x DUART, 6x LP UART
- 3x I²C, 2x SPI, GPIO
- Audio Subsystem: 4x I²S, ASRC, SPDIF
- FlexTimer, PWM
- USB 2.0
- USB 3.0 w/ PHY

ARM® Cortex®-A7 Core — FPU, NEON
ARM® Cortex®-A7 Core — FPU, NEON

32 KB D Cache | 32 KB I Cache | 32 KB D Cache | 32 KB I Cache

512 KB Coherent L2 Cache

DDR3L/4 Memory Controller
128 KB SRAM

Cache Coherent Interconnect (CCI 400)

uQE (HDLC, TDM, PB)
Security (XoR, CRC)

Ethernet | Ethernet | Ethernet | PCIe 2.0 | PCIe 2.0 | SATA 3.0

4-Lane 6 GHz SerDes

Legend:
- Core Complex
- Basic Peripherals and Interconnect
- Accelerators and Memory Control
- Networking Elements

View additional information for Layerscape® 1020A and 1022A Dual-Core Processors.

Note: The information on this document is subject to change without notice.