



Arm926EJ-S™ with 256 kB SRAM, USB High-speed OTG, SD/MMC, NAND flash controller, Ethernet

LPC3240FET296

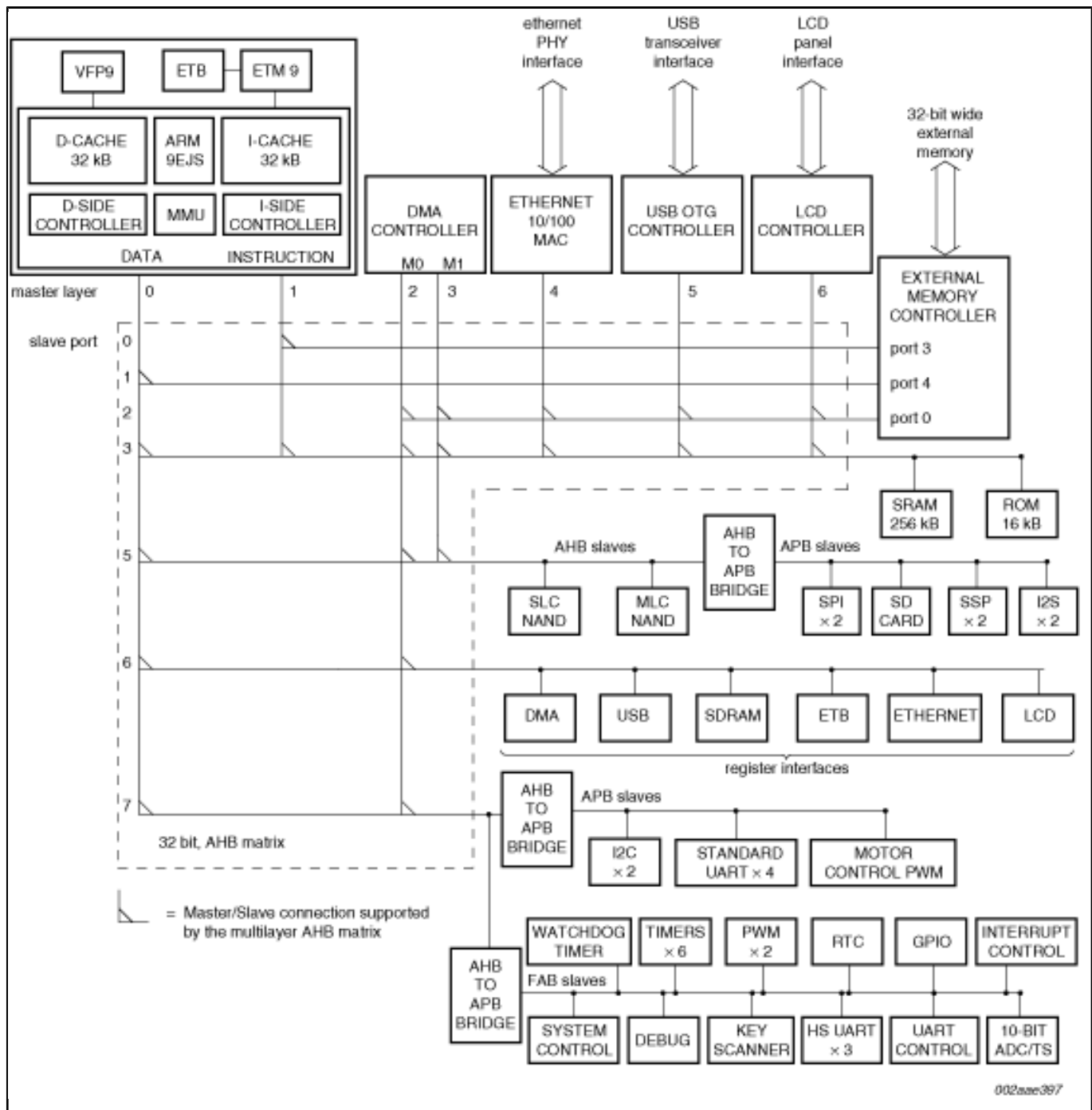
Not Recommended for New Designs

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The LPC3240 operates at CPU frequencies of up to 266 MHz. The NXP® implementation uses an ARM926EJ-S CPU core with a Harvard architecture, 5-stage pipeline, and an integral Memory Management Unit (MMU). The LPC3240 also includes 256 kB of on-chip static RAM, a NAND flash interface, an Ethernet MAC, and an external bus interface that supports SDR and DDR SDRAM, as well as static devices. In addition, the LPC3240 includes a USB 2.0 full-speed interface, seven UARTs, two I2C-bus interfaces, two SPI/SSP ports, two I2S-bus interfaces, two single output PWMs, a motor control PWM, six general purpose timers with capture inputs and compare outputs, a Secure Digital (SD) interface, and a 10-bit Analog-to-Digital Converter (ADC) with a touch screen sense option.

Block diagram: LPC3220FET296, LPC3230FET296, LPC3240FET296, LPC3250FET296
Block Diagram



View additional information for [Arm926EJ-S™ with 256 kB SRAM, USB High-speed OTG, SD/MMC, NAND flash controller, Ethernet.](#)

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