8-Bit LVTTL-to-GTL Transceiver

GTL2018PW

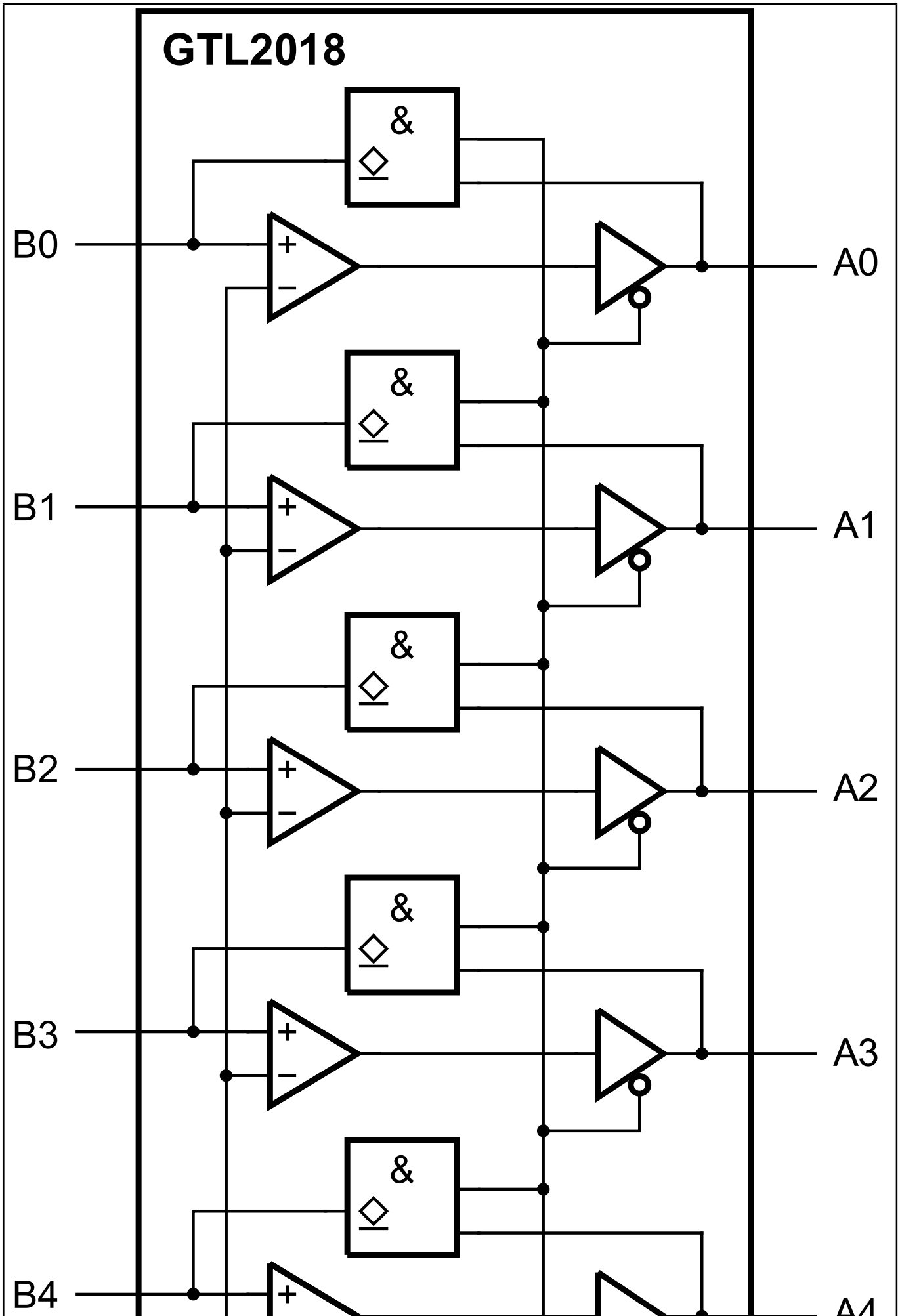
Last Updated: Mar 15, 2024

The GTL2018 is an octal translating transceiver designed for 3.3 V LVTTL system interface with a GTL-/GTL/GTL+ bus.

The direction pin (DIR) allows the part to function as either a GTL-to-LVTTL sampling receiver or as an LVTTL-to-GTL interface.

The GTL2018 LVTTL inputs (only) are tolerant up to 5.5 V, allowing direct access to TTL or 5 V CMOS inputs.

GTL2018 Block Diagram Block Diagram


GTL2018
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B0
A0
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View additional information for 8-Bit LVTTL-to-GTL Transceiver.

Note: The information on this document is subject to change without notice.