



# 8-Bit LVTTTL-to-GTL Transceiver

## GTL2018PW

Last Updated: Dec 15, 2024

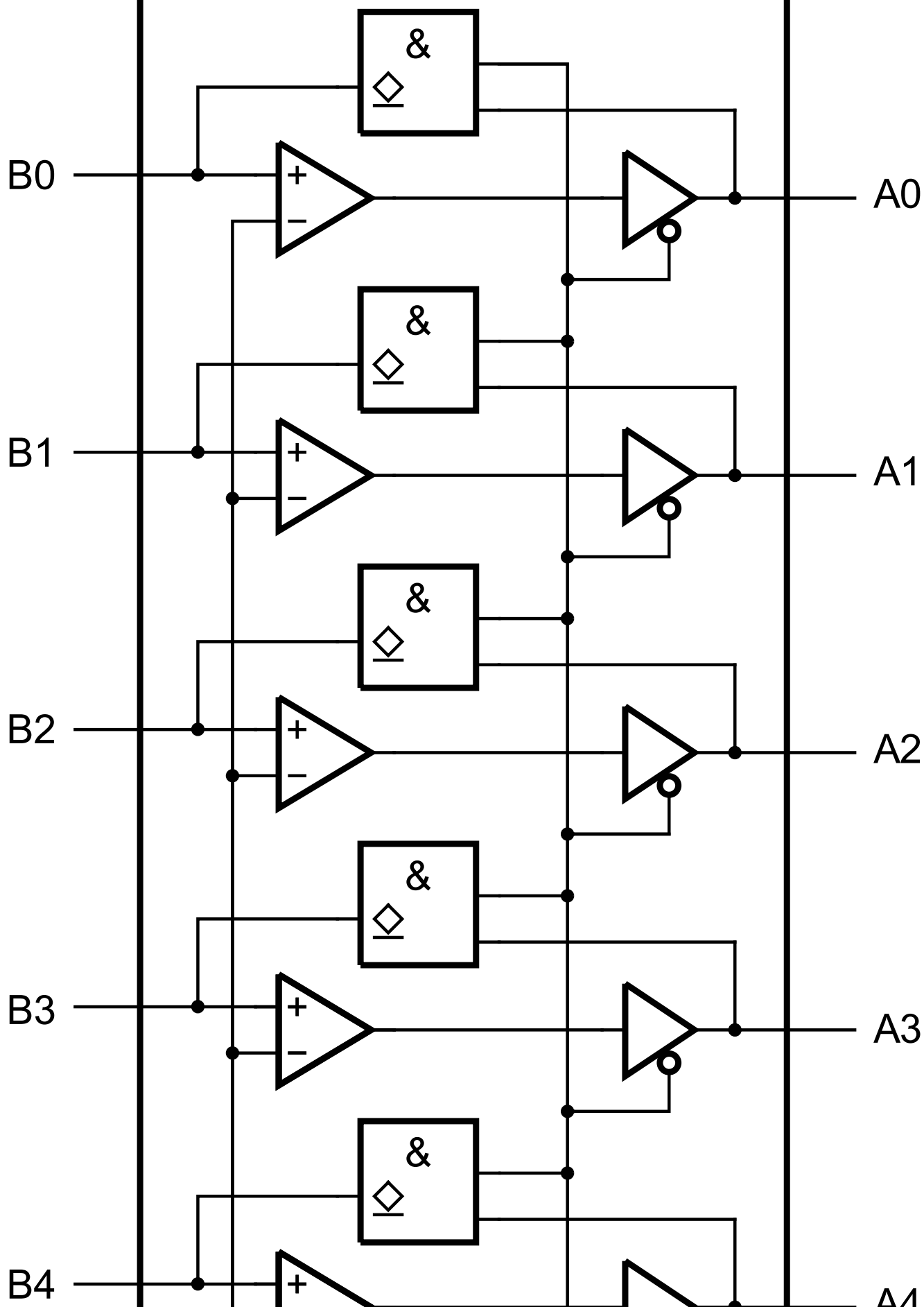
The GTL2018 is an octal translating transceiver designed for 3.3 V LVTTTL system interface with a GTL-/GTL/GTL+ bus.

The direction pin (DIR) allows the part to function as either a GTL-to-LVTTTL sampling receiver or as an LVTTTL-to-GTL interface.

The GTL2018 LVTTTL inputs (only) are tolerant up to 5.5 V, allowing direct access to TTL or 5 V CMOS inputs.

## **GTL2018 Block Diagram Block Diagram**

# GTL2018



View additional information for [8-Bit LVTTTL-to-GTL Transceiver](#).

**Note:** The information on this document is subject to change without notice.

---

**[www.nxp.com](http://www.nxp.com)**

NXP and the NXP logo are trademarks of NXP B.V. All other product or service names are the property of their respective owners. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. © 2025 NXP B.V.