4-Bit LVTTL-to-GTL Transceiver

GTL2014PW

Last Updated: Mar 15, 2024

The GTL2014 is a 4-bit translating transceiver designed for 3.3 V LVTTL system interface with a GTL-/GTL/GTL+ bus, where GTL-/GTL/GTL+ refers to the reference voltage of the GTL bus and the input/output voltage thresholds associated with it.

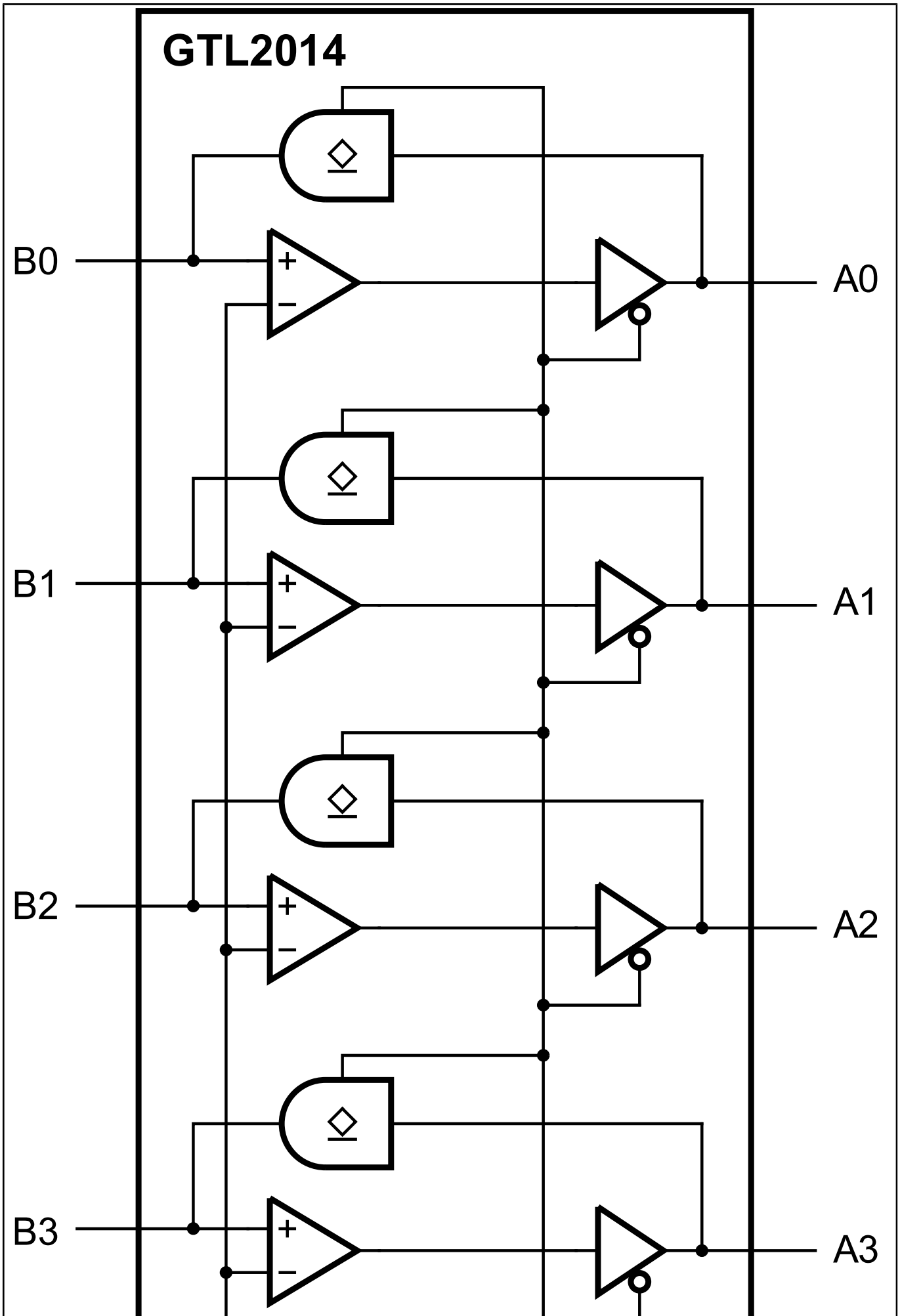
The direction pin allows the part to function as either a GTL to LVTTL sampling receiver or as a LVTTL to GTL interface.

The GTL2014 LVTTL inputs (only) are tolerant up to 5.5 V allowing direct access to TTL or 5 V CMOS inputs. The LVTTL outputs are not 5.5 V tolerant.

The GTL2014 GTL inputs and outputs operate up to 3.6 V, allowing the device to be used in higher voltage open-drain output applications.

GTL2014 is pin-to-pin backward compatible to the GTL2005 (labels for A port and B port are interchanged). GTL2014's Vref tracks down to 0.5 V for low voltage CPU, propagation delays are slightly longer, while GTL2005's Vref linearity degrades below 0.8 V and has shorter propagation delay.

GTL2014 Block Diagram Block Diagram


GTL2014
B0
B1
B2
B3
A0
A1
A2
A3

View additional information for 4-Bit LVTTL-to-GTL Transceiver.

Note: The information on this document is subject to change without notice.